

Boomer[®]Audio Power Amplifier Series

Class G Headphone Amplifier with I²C Volume Control

General Description

The LM48824 is a Class G, ground-referenced stereo headphone amplifier designed for portable devices. The LM48824 features National's ground-referenced architecture, which eliminates the large DC blocking capacitors required by traditional headphone amplifiers, saving board space and minimizing system cost.

The LM48824 takes advantage of National's patent-pending Class G architecture offering power savings compared to a traditional Class AB headphone amplifier. Additionally, output noise is improved by common-mode sensing that corrects for any differences between the amplifier ground and the potential at the headphone return terminal, minimizing noise created by any ground mismatches.

A high output impedance mode allows the LM48824's outputs to be driven by an external source without degrading the signal. Other features include flexible power supply requirements, differential inputs for improved noise rejection, a low power (2.5µA) shutdown mode, and a 32-step I²C volume control with mute function.

The LM48824's superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48824 is available in an ultra-small 16-bump, 0.4mm pitch micro SMD package (1.69mm x 1.69mm)

Key Specifications

Quiescent Power Supply Current at 3.6V	0.9mA	(typ)
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Output Power/channel at V _{DD} = 3.6V	
R _L = 16Ω, THD+N ≤ 1%	37mW (typ)

- Output I ower/chamier at v _{DD} - 0.0V	
R _L = 32Ω, THD+N ≤ 1%	29mW (typ)
PSRR at 217Hz	100dB (typ)
Shutdown current	2.5µA (typ)

Features

- Class G Power Savings
- Ground Referenced Headphone Outputs Eliminates **Output Coupling Capacitors**
- Common-Mode Sense
- I²C Volume and Mode Control
- High Output Impedance in Shutdown
- **Differential Inputs**
- Advanced Click-and-Pop Suppression
- Low Supply Current
- Low THD mode option

Applications

- Mobile Phones, PDAs, MP3 Players
- Portable Electronic Devices, Notebook PCs



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Typical Application 查询"LM48824"供应商



FIGURE 1. Typical Audio Amplifier Application Circuit

Con查爾tiona & Dag 共和国 TM Package 1.7mm x 1.7mm x 0.6mm 16–Bump micro SMD Marking XYTT Α sw OUTL INL- V_{DD} GL6 Pin 1 В GND C1P HPVDD INL+ 30089217 Top View XY = Date code TT = Die traceability G = Boomer Family L6 = LM48824TM С C1N сом INR+ HPVSS D SCL SDA OUTR INR-1 2 3 4 30089220 **Top View** Order Number LM48824TM See NS Package Number TMD16DDA

Ordering Information

Order Number	Package	Package DWG #	Transport Media	MSL Level	Green Status
LM48824TM	16 Bump micro SMD	TMD16DDA	250 units on tape and reel	1	NOPB
LM48824TMX	16 Bump micro SMD	TMD16DDA	3000 units on tape and reel	1	NOPB

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Bump	Name	Pin Descriptions
A1	SW	Regulator Switching Node
A2	V _{DD}	Power Supply
A3	OUTL	Left Channel Output
A4	INL-	Left Channel Inverting Input
B1	GND	Ground
B2	C1P	Charge Pump Flying Capacitor Positive Terminal
B3	HPV _{DD}	Amplifier Power Supply/Regulator Output
B4	INL+	Left Channel Non-Inverting Input
C1	C1N	Charge Pump Flying Capacitor Negative Terminal
C2	HPV _{SS}	Charge Pump Output
C3	СОМ	Common-mode Sense Input. Connect to headphone jack return
C4	INR+	Right Channel Non-Inverting Input
D1	SDA	I2C Serial Data Input
D2	SCL	I2C Serial Clock Input
D3	OUTR	Right Channel Output
D4	INR-	Right Channel Inverting Input

Absolute Maximum Ratings (Note 1, Note 查询"LM48824"供应商 <u>2</u>)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 1)	6\
Storage Temperature	–65°C to +150°C
Input Voltage	-0.3V to V _{DD} + 0.3V
Power Dissipation (<i>Note 3</i>)	Internally Limited
ESD Rating (<i>Note 4</i>)	2000\
ESD Rating (<i>Note 5</i>)	200\
ESD Rating (<i>Note 6</i>)	500\
Junction Temperature	150°C

Soldering Information Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Thermal Resistance	
θ _{JA} (TMA16DDA)	60°C/W
Soldering Information	

See AN-1112 "Micro SMD Wafer Level Chip Scale package"

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40^{\circ}C \le T_A \le +85^{\circ}C$
Supply Voltage (V _{DD})	$2.4V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 3.6V (*Note 1, Note 2*) The following specifications apply for A_V = 0dB, R_L = 32 Ω , f = 1kHz, unless otherwise specified. Limits apply to T_A = 25°C.

			LM48824		Units
Symbol	Parameter	Conditions	Typical (<i>Note 7</i>)	Limit (<i>Note 8</i>)	(Limits)
I _{DD}	Quiescent Power Supply Current	$V_{IN} = 0V$, both channels active $R_L = \infty$	0.9	1.3	mA (max)
55		$R_{L} = \infty$, Low THD mode	1.55		mA
		$P_{O} = 100\mu$ W, two channels in phase, 3dB Crest Factor, $R_{L} = 32\Omega + 15\Omega$	1.8	2.5	mA (max)
		$P_O = 100\mu$ W, two channels in phase, 3dB Crest Factor, $R_L = 32\Omega + 15\Omega$, Low THD mode	2.2		mA
		$P_{O} = 500\mu$ W, two channels in phase, 3dB Crest Factor R _L = 32 Ω + 15 Ω	3.1	3.8	mA (max)
I _{DD(OP)}	Operating Power Supply Current	$P_O = 500\mu$ W, two channels in phase, 3dB Crest Factor R _L = $32\Omega + 15\Omega$, Low THD mode	3.4		mA
		P_{O} = 1mW, two channels in phase, 3dB Crest Factor, R_{L} = 32 Ω + 15 Ω	4.1	4.9	mA (max)
		$P_O = 1$ mW, two channels in phase, 3dB Crest Factor, $R_L = 32\Omega + 15\Omega$, Low THD mode	4.4		mA
I _{SD}	Shutdown Current	Shutdown Enabled V _{SCL} = V _{SDA} = 1.8V	2.5	3.9	µA (max)
V _{os}	Output Offset Voltage	V _{IN} = 0V	0.15	0.65	mV (max)
T _{WU}	Wake Up Time	From Shutdown	2		ms
	Coin	Minimum Gain Setting	-59	-58 -60	dB (max) dB (min)
A _V		Maximum Gain Setting	4	4.5 3.5	dB (max) dB (min)
A _{V(MUTE)}	Mute Attenuation		-110		dB
R _{IN}	Input Resistance	$A_V = 4dB$ $A_V = -59dB$	24 64	20 80	$k\Omega$ (min) $k\Omega$ (max)

LM48824

			LM48824		Units	
syin 0.6 48	824"供应商 Parameter	Conditions	Typical (<i>Note 7</i>)	Limit (<i>Note 8</i>)] (Limit	
		f = 1kHz, THD+N = 1%				
		Two channels in phase	37	30	mW (r	
Þ	Output Power	R _L = 16Ω				
0		f = 1kHz, THD+N = 1%				
		Two channels in phase	29	23	mW (r	
		$R_L = 32\Omega$,				
		THD+N = 1%, Two Channels in Phase	1	1	1	
		R _L = 16Ω	0.77	0.7	V _{RN} (mir	
Vo	Output Swing	R _L = 32Ω	0.96	0.86	V _{RN} (mir	
		$R_L = 32\Omega + 15\Omega$	1.05		V _{RN}	
		$R_L = 10k\Omega$	1.3	1.1	V _{RN} (mir	
		f = 1kHz, Single Channel		•		
		$V_{\Omega} = 600 \text{mV}_{\text{BMS}}, R_{1} = 16\Omega$	0.05	1	%	
		$V_0 = 600 \text{mV}_{\text{RMS}}, \text{ R}_1 = 16\Omega,$ Low THD Mode	0.03		%	
	Total Harmonic Distortion + Noise	$V_{-} = 800 \text{mV}_{} \text{B}_{-} = 320$	0.035		%	
THD+N		$V_0 = 800 \text{mV}_{\text{RMS}}, H_1 = 6252,$	0.000		//	
		$V_{O} = 800 \text{mV}_{RMS}, \text{H}_{L} = 32\Omega,$ Low THD Mode	0.02		%	
		$V_0 = 900 \text{mV}_{\text{RMS}}, \text{R}_{\text{L}} = 32\Omega + 15\Omega$	0.027	0.04	%(m	
		$V_{O} = 900 \text{mV}_{\text{RMS}}, \text{ R}_{L} = 32\Omega + 15\Omega,$ Low THD Mode	0.015		%	
		$V_{RIPPLE} = 200 m V_{P-P}$, Inputs AC GND				
	Power Supply Dejection Datio	$C_{IN} = 1\mu F$, input referred,				
ronn		f _{RIPPLE} = 217Hz	100	94	dB (n	
		f _{RIPPLE} = 1kHz	100		dE	
CMRR	Common Mode Rejection Ratio	$V_{RIPPLE} = 1V_{P-P}, f_{RIPPLE} = 217Hz$	60		dE	
		$R_1 \ge 16\Omega, P_0 = 5mW, f = 1kHz$	80	70	dB (n	
X _{TALK}	Crosstalk	$B_{\mu} \ge 10 \text{kg}$, $V_{\text{out}} = 1V_{\text{out}}$, $f = 1 \text{kHz}$	110	95	dB (n	
		$V_{\text{CUT}} = 1V_{\text{EVE}}, f = 1kHz$	102	98	dB (n	
SNR	Signal-to-Noise Ratio	$V_{\text{OUT}} = 1V_{\text{PMO}}, f = 1kHz.$				
		Low THD Mode	105		dE	
		$A_{\rm V} = 4$ dB, A-Weighted Filter	8	12	μV(m	
€os	Output Noise	$A_{V} = 4$ dB, A-weighted Filter,	_			
		Low THD Mode	7		μ\	
		Charge pump-only mode enabled		•	•	
-		f < 40kHz	43	30	kΩ (r	
R _{OUT}	Output Impedance	f = 6MHz		500	Ω (m	
		f = 36MHz		75	Ω (m	
		No Sustained Oscillations				
CL	Maximum Capacitive Load	with 5 Ω series resistance	100		nF	
-		with no series resistance	100		pF	
VOUT	Maximum Voltage Swing	Voltage applied to amplifier outputs in	1.1	1.0	V _{RN}	

I C Interface Characteristics $V_{DD} = 3.6V$ (*Note 1, Note 2*) The following specifications apply for $A_V = 0$ dB, $B_L = 16\Omega$, f = 1kHz, unless otherwise specified. Limits apply to $T_A = 25^{\circ}$ C.

			LM	Units	
Symbol	Parameter	Conditions	Typical	Limit	(Limits)
			(Note 7)	(<i>Note 8</i>)	
t ₁	SCL Period			2.5	µs (min)
t ₂	SDA Setup Time			250	ns (min)
t ₃	SDA Stable Time			250	ns (min)
t ₄	Start Condition Time			250	ns (min)
t ₅	Stop Condition Time			250	ns (min)
V _{IH}	Input High Voltage			1.2	V (min)
V _{IL}	Input Low Voltage			0.6	V (max)

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T, IMAX, θ, IA, and the ambient temperature, TA. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Charged Device Model, applicable std. JESD22-C101-C.

Note 7: Typical values represent most likely parametric norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Datasheet min/max specification limits are guaranteed by test or statistical analysis.



Typical Performance Characteristics 适询"LM48824"供应商













10

1

0.1

0.01

100

10

1

0.1

0.01

10

1

0.1

0.01

THD + N (%)

THD + N (%)

THD + N (%)

LM48824











10000

100000

300892h9

Application Information 查询"LM48824"供应商 I²C COMPATIBLE INTERFACE

The LM48824 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48824 and the master can communicate at clock rates up to 400kHz. Figure 2 shows the I2C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48824 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 3). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 4). The LM48824 device address is 1100000.

I²C BUS FORMAT

The I²C bus format is shown in Figure 4. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/\overline{W} bit ($R/\overline{W} = 0$ indicates the master is writing to the LM48824, $R/\overline{W} = 1$ indicates the master wants to read data from the LM48824). Data is latched into the device on the rising clock edge. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48824 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register address word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register address is sent, the LM48824 sends another ACK bit. Following the acknowledgment of the register address, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data is sent, the LM48824 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.



FIGURE 2. I²C Timing Diagram



FIGURE 3. Start and Stop Diagram



	B7	B6	B5	B4	B3	B2	B1	B0 (R/W)
Device Address	1	1	0	0	0	0	0	х

TABLE 2. I²C Control Registers (Note 9) 查询"LM48824"供应商 Register Register **B**7 **B6 B**5 Β4 **B**3 **B2 B1 B**0 Address Name MODE 0x01h HPL_EN HPR_EN 0 0 0 0 THRM SHDN CONTROL VOLUME 0x02h MUTE_L* MUTE_R* VOL4 VOL3 VOL2 VOL1 VOL0 0 CONTROL OUTPUT 0x03h 0 0 0 0 LOW_THD 0 HiZ_L HiZ_R CONTROL DEVICE INFORMATI 0x04h 0 0 0 0 0 0 0 1 ON (Read-Only)

Note 9: * All registers default to 0 on initial power-up except SHDN, MUTE_L, MUTE_R bits default to 1 at power-up.

TABLE 3. Mode Control Register

Bit	Name	Value	Description	
PO		0	Device enabled	
DU	SHUN	1	Device disabled	
D1	THRM	0	Thermal-protection inactive	
ВІ	(Read Only)	1	Thermal-protection active	
DC	HPR_EN	0	Right channel amplifier disabled	
Во		1	Right channel amplifier enabled	
B7	HPL_EN -	0	Left channel amplifier disabled	
		1	Left channel amplifier enabled	

TABLE 4. Volume Control Register

Bit	Name	Value Description		
B5:B1	VOL4:VOL0	These bits set the volume level. (Volume Control).		
Re	MUTE_R	0	Right Channel Mute Disabled	
DO		1	Right Channel Mute Enabled	
DZ	MUTE_L	0	Left Channel Mute Disabled	
В/		1	Left Channel Mute Enabled	

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$\boldsymbol{\omega}$	
$\boldsymbol{\omega}$	
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olume Step	VOL4	VOL3	VOL2	VOL1	VOL0	HP Gain (dB)
0	0	0	0	0	0	-59
1	0	0	0	0	1	-55
2	0	0	0	1	0	-51
3	0	0	0	1	1	-47
4	0	0	1	0	0	-43
5	0	0	1	0	1	-39
6	0	0	1	1	0	-35
7	0	0	1	1	1	-31
8	0	1	0	0	0	-27
9	0	1	0	0	1	-25
10	0	1	0	1	0	-23
11	0	1	0	1	1	-21
12	0	1	1	0	0	-19
13	0	1	1	0	1	-17
14	0	1	1	1	0	-15
15	0	1	1	1	1	-13
16	1	0	0	0	0	-11
17	1	0	0	0	1	-10
18	1	0	0	1	0	-9
19	1	0	0	1	1	-8
20	1	0	1	0	0	-7
21	1	0	1	0	1	-6
22	1	0	1	1	0	-5
23	1	0	1	1	1	-4
24	1	1	0	0	0	-3
25	1	1	0	0	1	-2
26	1	1	0	1	0	-1
27	1	1	0	1	1	0
28	1	1	1	0	0	1
29	1	1	1	0	1	2
30	1	1	1	1	0	3
31	1	1	1	1	1	4
			1		•	·

TABLE 6. Output Control Register

Bit	Name	Value	Description	
Bo	HiZ_R	0	Right channel high impedance mode disabled	
во		1	Right channel high impedance mode enabled	
B1	HiZ_L	0	Left channel high impedance mode disabled	
		1	Left channel high impedance mode enabled	
В3	LOW_THD	0	LOW_THD mode disabled	
		1	LOW_THD mode enabled, improves overall THD	

GENERAL DEVICE FUNCTION

The LM29334 integeo 4 to 5.5V. The switching regulator with a ground reference headphone amplifier. The switching regulator delivers a constant voltage from an input voltage ranging from 2.4V to 5.5V. The switching regulator uses a voltage-mode architecture with synchronous rectification, improving efficiency and reducing component count.

The LM48824 headphone amplifier features National's ground referenced architecture that eliminates the large DCblocking capacitors required at the outputs of traditional single-ended headphone amplifiers. A low-noise inverting charge pump creates a negative supply (HPV_{SS}) from the positive supply voltage (V_{DD}). The headphone amplifiers operate from these bipolar supplies, with the amplifier outputs biased about GND. Because there is no DC component on the output signals, the large DC-blocking, AC coupling capacitors (typically 220µF) are not necessary, conserving board space, reducing system cost, and improving frequency response.

CLASS G OPERATION

Class G is a modification of some other class of amplifier (normally Class B or Class AB) to increase efficiency and reduce power dissipation. Class G works off the fact that musical and voice signals have a high peak to mean ratio with most of the signal content at low levels. To decrease power dissipation, Class G has multiple voltage supplies. The LM48824 has two discrete voltage supplies at the output of the buck, 1.1V and 1.8V. When the output reached the threshold to switch to the higher voltage rails, the rails will switch from 1.1V to 1.8V. When the output falls below the required voltage rails for a set period of time, it will switch back to the lower rail until the next time the threshold is reached. Power dissipation is greatly reduced for typical musical or voice sources. The drawing below shows how a musical output may look. The green lines are the supply voltages at the output of the buck converter.



LM48824

DIFFERENTIAL AMPLIFIER EXPLANATION

间些LW4882矩曲 供 应 通道fferential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled.

SYNCHRONOUS RECTIFIER

The buck converter in the LM48824 uses an internal NFET synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relative low compared to the voltage drop across an ordinary rectifier diode and eliminating the need for the diode.

CURRENT LIMITING

A current limit of the buck converter in the LM48824 allows the device to protect itself and external components during overload conditions.

PFM OPERATION

During PFM(Pulse-Frequency Modulation) operation, if the output voltage of the buck converter is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is I_{PFM} = 112mA + V_{DD}/27\Omega.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold, the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode.





SOFT START

The buck converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if global SHDN goes from 1 to 0 after V_{DD} reaches 2.7V. Soft start is implemented by increasing switch current limit in steps of 70-mA, 140mA, 280mA, and 750mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current of the buck converter. Typical start-up times with a 10uF output capacitor and 150mA load is 280us and with 5mA load is 240us.

COMMON-MODE SENSE

The LM48824 features a ground (common mode) sensing feature. In noisy applications, or where the headphone jack is

used as a line out to other devices, noise pick up and ground imbalance can degrade audio quality. The LM48824 COM input senses and corrects any noise at the headphone return, or any ground imbalance between the headphone return and device ground, improving audio reproduction. Connect COM directly to the headphone return terminal of the headphone jack (*Figure 8*). No additional external components are required. Connect COM to GND if the common-mode sense feature is not in use.





SHUTDOWN FUNCTION

The LM48824 features individual amplifier shutdown control and a global device shutdown control.

Bit B0 (SHDN) of the MODE CONTROL register controls the global shutdown for the entire device. Set SHDN = 1 to put the device into current-saving shutdown mode, and set SHDN = 0 for normal operation. SHDN defaults to 1 at power-up.

Bit B7 (HPL_EN) and Bit B6 (HPR_EN) of the MODE CON-TROL register (register address 0x01h) controls the left and right headphone amplifier shutdown respectively. Set HPL_EN = 0 to set the left channel headphone amplifier to shutdown and set HPL_EN = 1 to enable left channel operation. Set HPR_EN = 0 to set the right channel headphone amplifier to shutdown and set HPR_EN = 1 to enable right channel operation. The left and right channel amplifier shutdowns operate individually.

The LM48824 has a shutdown time of 3ms to complete the internal shutdown sequence. After SHDN is set to 1, any new I²C commands should only be sent after the 3ms shutdown time to ensure proper operation of the device.

MUTE FUNCTION

The LM48824 features independent left and right channel mute functions.

Bit B7 (MUTE_L) and Bit B6 (MUTE_R) of the VOLUME CONTROL register (register address 0x02h) controls the mute function of the left and right channels respectively. Set $MUTE_L = 1$ to mute the left channel and set the $MUTE_R =$ 1 to mute the right channel. Set $MUTE_L = 0$ and $MUTE_R =$ 0 to disable mute on the respective channels. $MUTE_L$ and $MUTE_R$ defaults to 1 at power-up.

LOW THD+N MODE

The LM48824 features a Low THD mode that reduces THD +N to improve audio qaulity. Set B3 (Low_THD) of the OUT-PUT CONTROL register (register address 0x03h) to 1 to enable the Low THD mode. There is a quiescent and operating current increase in Low THD mode. See Electrical Characteristics table and Typical Performance Characteristics for reference.

PROPER SELECTION OF EXTERNAL COMPONENTS

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor saturation current and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded capacitors are preferred since these capacitors radiate less noise. Inductors with low DCR should also be considered to minimize the efficiency.

Inductor value involves trade-offs in performance. Larger inductors reduce inductor triple current, which typically means less output voltage ripple (for a given size of output capacitor).

REGULATOR INPUT CAPACITOR SELECTION (C3)

A ceramic input capacitor of 1μ F, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{DD} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603.

REGULATOR OUTPUT CAPACITOR SELECTION (C4)

A low ESR ceramic output capacitor of 10μ F, 6.3V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

CHARGE PUMP CAPACITOR SELECTION

Use low ESR ceramic capacitors (less than 100m $\!\Omega\!)$ for optimum performance.

CHARGE PUMP FLYING CAPACITOR (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2μ F, the R_{DS(ON)} of the charge pump switches and the ESR of C1 and C2 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

CHARGE PUMP HOLD CAPACITOR (C2)

Amplifier Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48824. The input capacitors create a highpass filter with the input resistors RIN. The -3dB point of the high-pass filter is found using Equation (1) below.

$$f = 1 / 2\pi R_{IN}C_{IN} \quad (Hz) \tag{1}$$

Where the value of R_{IN} is given in the Electrical Characteristics Table.

High-pass filtering the audio signal can be beneficial for some applications. When the LM48824 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

SINGLE-ENDED AUDIO AMPLIFIER CONFIGURATION

The LM48824 is compatible with single-ended sources. Figure 9 shows the typical single-ended applications circuit. Input coupling capacitors are required for single-ended configuration.



PCB LAYOUT CONFIGURATION 查询"LM48824"供应商 TABLE 7. LM48824TM Demoboard Bill of Materials

Designator	Quantity	Description		
C1	1	10μ F ±10% 16V 500 Ω Tantalum Capacitor (B Case) AVX TPSB106K016R0500		
C2	1	1µF ±10% 16V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1C105K		
C3, C8, C9	3	2.2µF ±10% 10V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1A225K		
C4 – C7	4	1µF ±10% 16V X7R Ceramic Capacitor (1206) Panasonic ECJ-3YB1C105K		
R1, R2	2	5kΩ ±5% 1/10W Thick Film Resistor (603) Vishay CRCW06035R1KJNEA		
L1	1	3.3µH ± 30% 1.2A Inductor Murata LQM2MPN3R3NG0L		
J1	1	Stereo Headphone Jack		
J2	1	16-Pin Boardmount Socket 3M 8516-4500JL		
JU1	1	3 Pin Header		
JU2	1	2 Pin Header		
LM4822TM	1	LM48824TM (16-Bump microSMD)		

Demoboard Schematic 查询"LM48824"供应商





FIGURE 11. Top Silkscreen



FIGURE 12. Top Layer

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FIGURE 13. Layer 2 (GND)









	Rev Date		Description	
	1.0	08/06/09	Initial released of the full datasheet.	
	1.01	08/31/09	Text edits.	



§询"LM48824"供应商

Notes

Pro	oducts	Design Support		
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench	
Audio	www.national.com/audio	App Notes	www.national.com/appnotes	
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns	
Data Converters	www.national.com/adc	Samples	www.national.com/samples	
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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging	
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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts	
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality	
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback	
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy	
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