

Preliminary Data

Features

- Gold metallization
- Excellent thermal stability
- Common source push-pull configuration
- $P_{OUT} = 350 \text{ W min.}$
with 26.8 dB gain @ 123 MHz
- In compliance with the 2002/95/EC
european directive

Description

The SD3932 is a gold metallized N-channel MOS field-effect RF power transistor. It is intended for use in 100V DC large signal applications up to 250MHz.

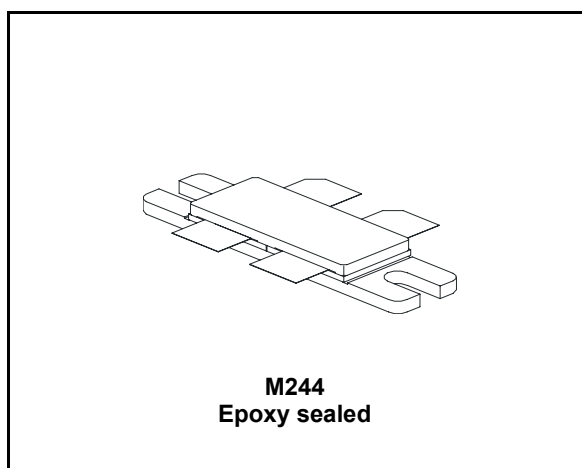
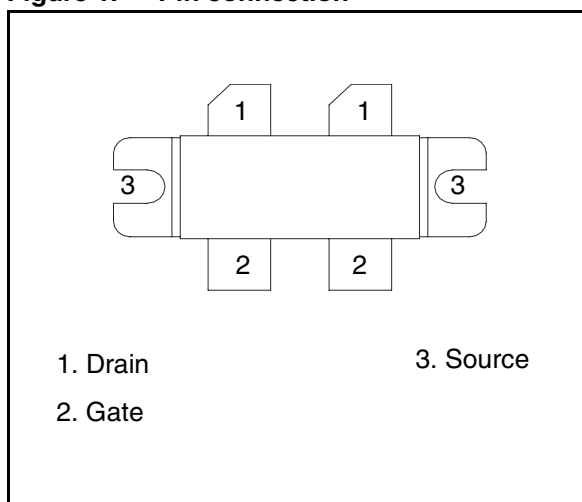


Figure 1. Pin connection

**Table 1. Device summary**

Order code	Marking	Package	Packaging
SD3932	SD3932	M244	Plastic tray

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1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings ($T_{CASE} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}^{(1)}$	Drain source voltage	250	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 1M\Omega$)	250	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current	20	A
P_{DISS}	Power dissipation	500	W
T_j	Max. operating junction temperature	200	$^{\circ}C$
T_{STG}	Storage temperature	-65 to +150	$^{\circ}C$

1. $T_j = 150^{\circ}C$

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.35	$^{\circ}C/W$

2 Electrical characteristics

$$T_{\text{CASE}} = +25\text{ }^{\circ}\text{C}$$

2.1 Static

Table 4. Static (per side)

Symbol	Test conditions			Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}^{(1)}$	$V_{\text{GS}} = 0\text{ V}$	$I_{\text{DS}} = 100\text{ mA}$		250			V
I_{DSS}	$V_{\text{GS}} = 0\text{ V}$	$V_{\text{DS}} = 100\text{ V}$				1	mA
I_{GSS}	$V_{\text{GS}} = 20\text{ V}$	$V_{\text{DS}} = 0\text{ V}$				250	nA
$V_{\text{GS(Q)}}$	$V_{\text{DS}} = 10\text{ V}$	$I_{\text{D}} = 250\text{ mA}$		1.5	2.5	4.0	V
$V_{\text{DS(ON)}}$	$V_{\text{GS}} = 10\text{ V}$	$I_{\text{D}} = 5\text{ A}$			2.5	3.5	V
G_{FS}	$V_{\text{DS}} = 10\text{ V}$	$I_{\text{D}} = 2.5\text{ A}$		3			S
C_{ISS}	$V_{\text{GS}} = 0\text{ V}$	$V_{\text{DS}} = 100\text{ V}$	$f = 1\text{ MHz}$		500		pF
C_{OSS}	$V_{\text{GS}} = 0\text{ V}$	$V_{\text{DS}} = 100\text{ V}$	$f = 1\text{ MHz}$		134		pF
C_{RSS}	$V_{\text{GS}} = 0\text{ V}$	$V_{\text{DS}} = 100\text{ V}$	$f = 1\text{ MHz}$		6		pF

1. $T_{\text{J}} = 150^{\circ}\text{C}$

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions			Min.	Typ.	Max.	Unit
$P_{1\text{dB}}$	$V_{\text{DD}} = 100\text{ V}$	$I_{\text{DQ}} = 2 \times 250\text{ mA}$	$f = 123\text{ MHz}$	350	425		W
G_{PS}	$V_{\text{DD}} = 100\text{ V}, I_{\text{DQ}} = 2 \times 250\text{ mA}, P_{\text{OUT}} = 350\text{ W}, f = 123\text{ MHz}$				26.8		dB
h_{D}	$V_{\text{DD}} = 100\text{ V}, I_{\text{DQ}} = 2 \times 250\text{ mA}, P_{\text{OUT}} = 350\text{ W}, f = 123\text{ MHz}$				66		%
Load mismatch	$V_{\text{DD}} = 100\text{ V}, I_{\text{DQ}} = 2 \times 250\text{ mA}, P_{\text{OUT}} = 300\text{ W}, f = 123\text{ MHz}$ All phase angles			3:1			VSWR

3 Impedance data

Figure 2. Impedance data

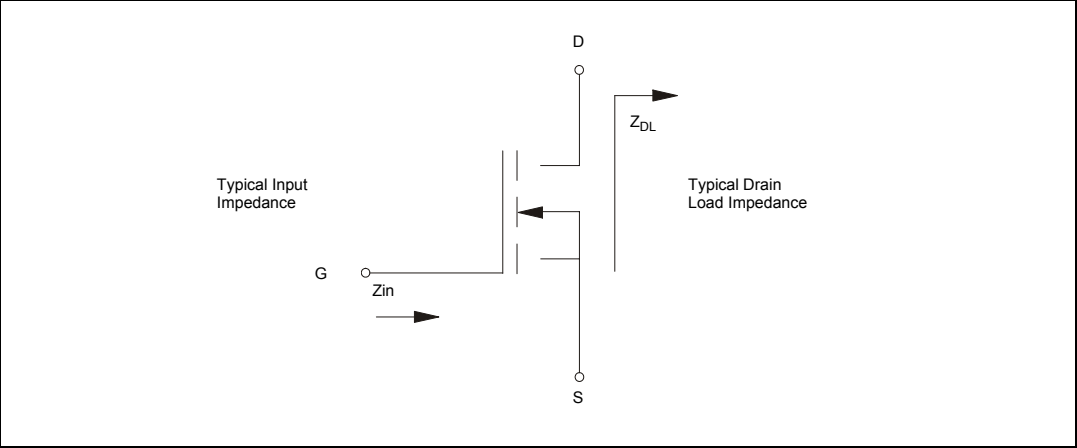


Table 6. Impedance data

Freq	$Z_{IN} (\Omega)$	$Z_{DL} (\Omega)$
123 MHz (800W Peak)	1.4 - j 5.5	6.4 + j 10.2
123 MHz (350W CW)	0.7 - j 3.9	3.2 + j 15

4 Typical performance

Figure 3. Capacitances vs voltage

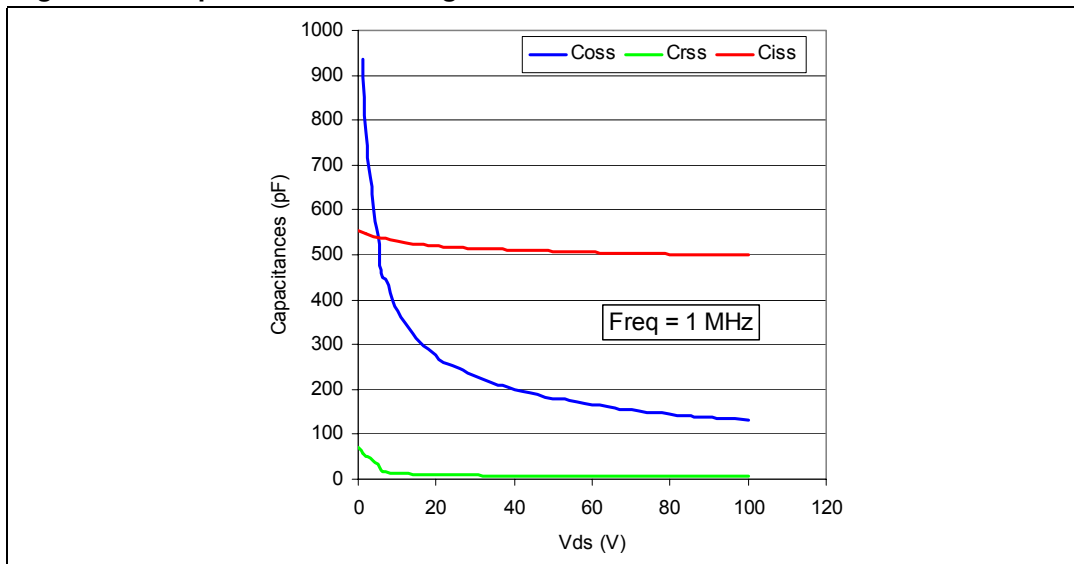


Figure 4. Transient thermal impedance

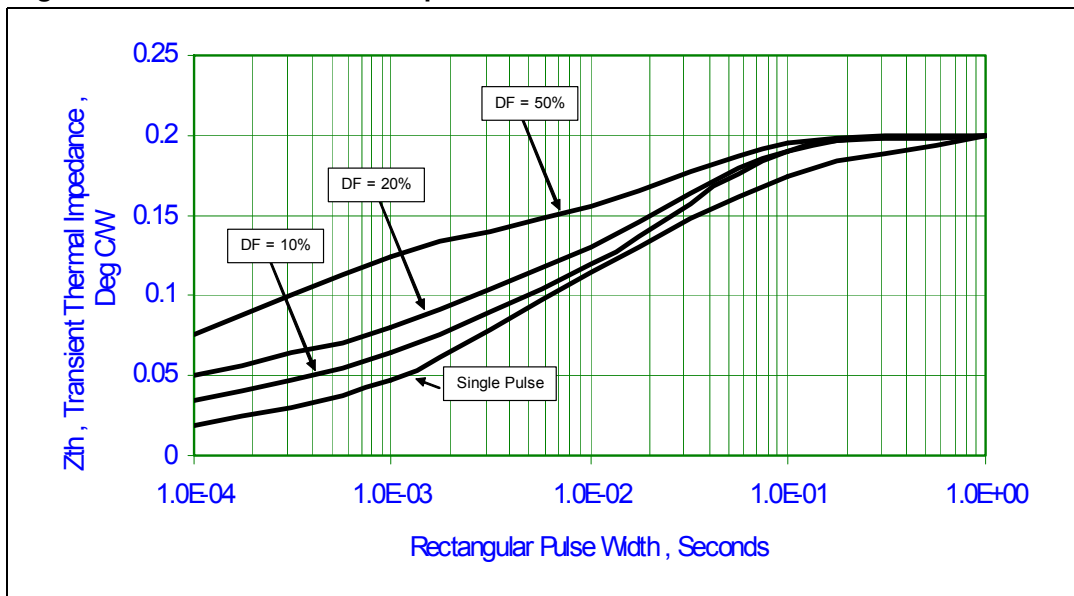


Figure 5. Maximum safe operating area

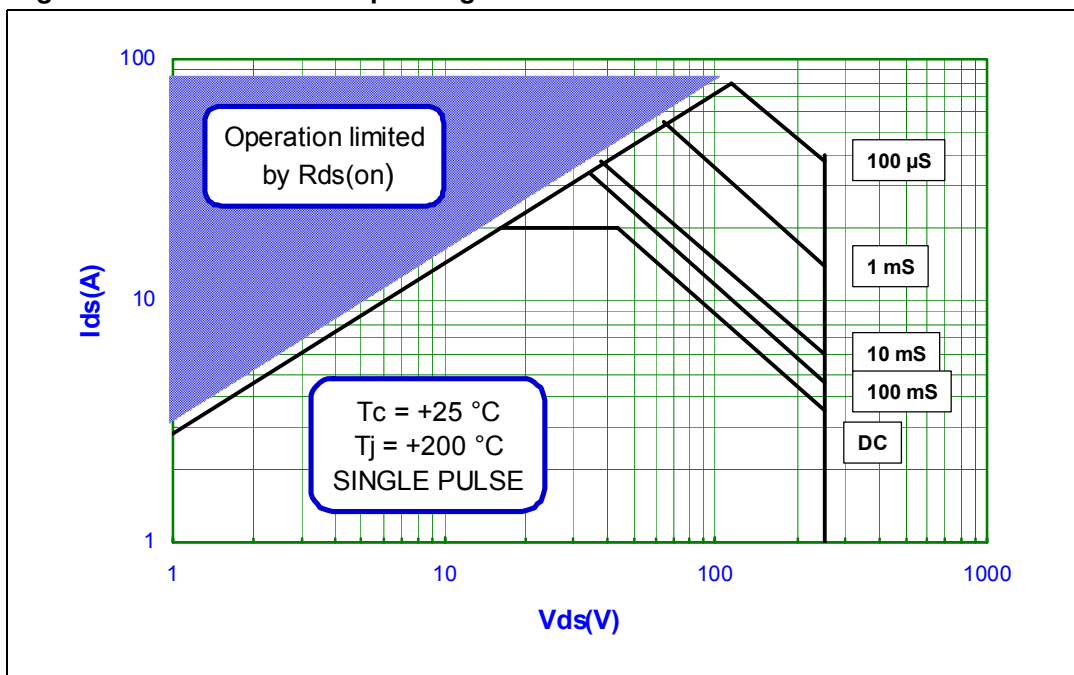


Figure 6. Zero temperature coefficient point

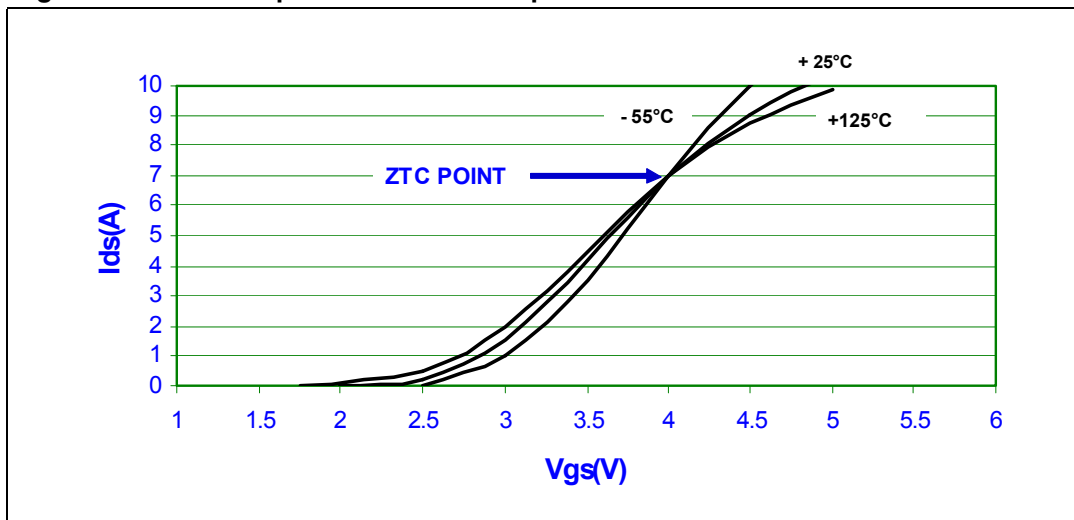


Figure 7. Pout & efficiency vs pin - CW

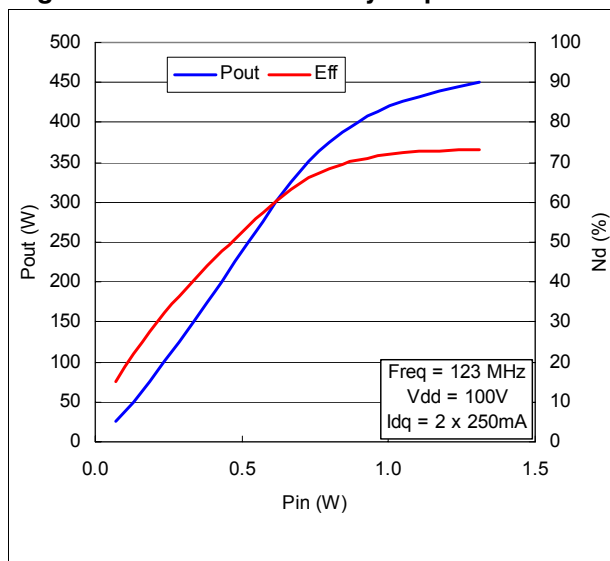


Figure 8. Gain vs output power - CW -

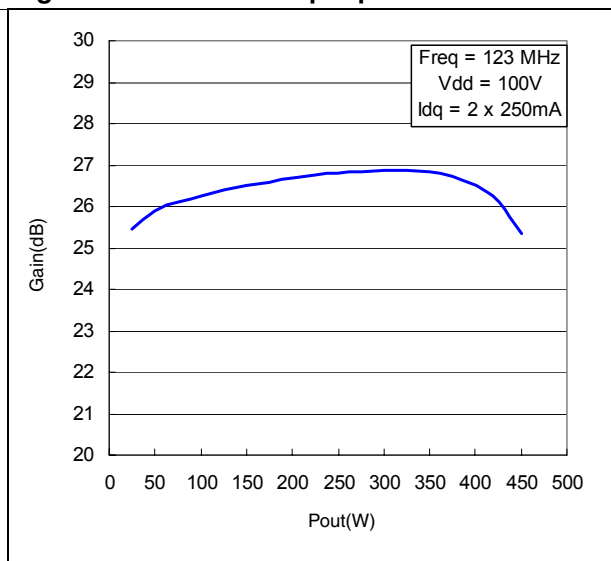


Figure 9. Pout & efficiency vs pin power
1 msec - 10%

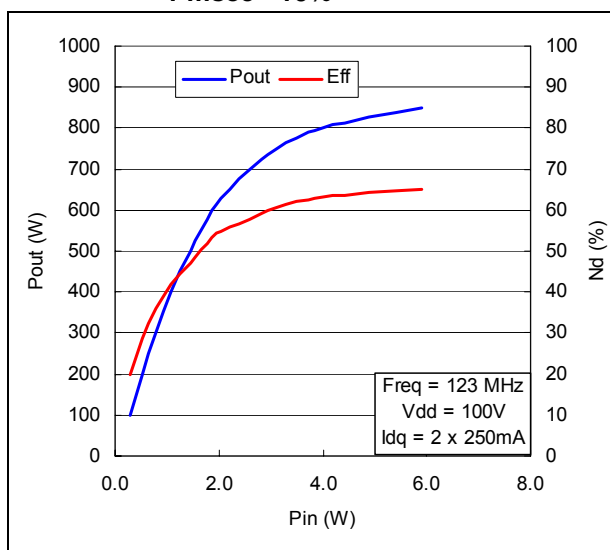
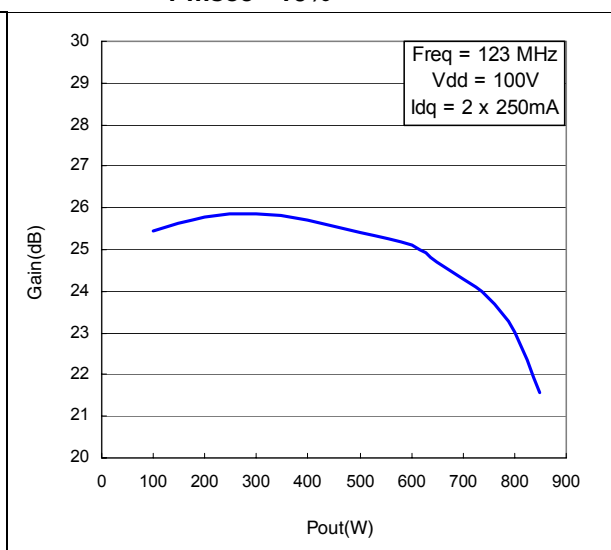


Figure 10. Gain vs output power
1 msec - 10%



5 Test circuit

Figure 11. Test circuit

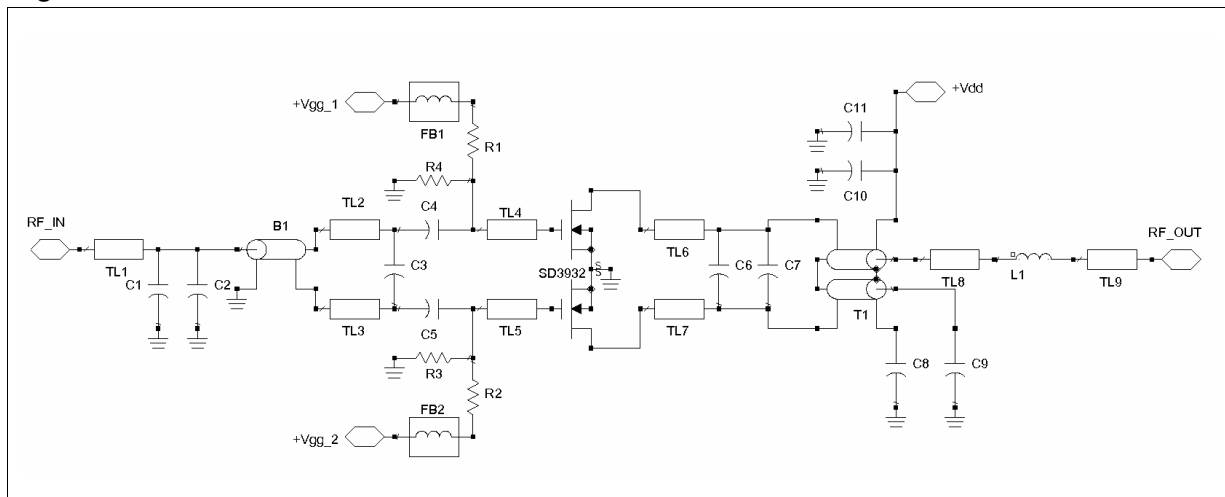


Table 7. Bill of materials

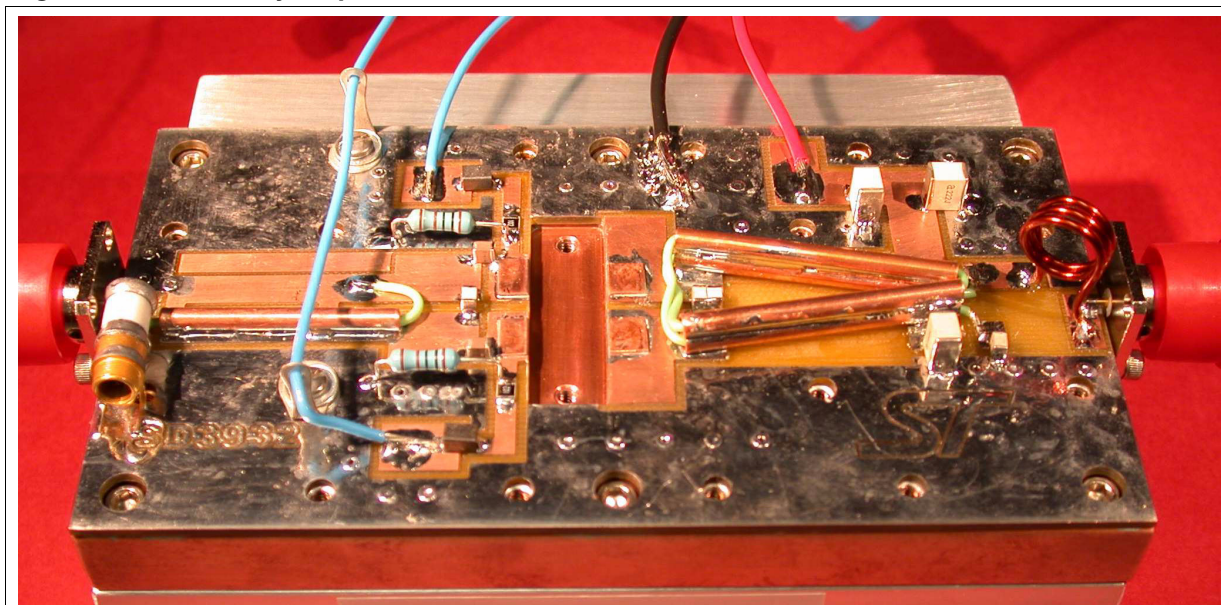
Component	Description
C1	120 pF ATC 100B chip capacitor
C2	1-20 pf Johanson variable capacitor
C3	51 pF ATC 100B chip capacitor
C4, C5	750 pF ATC 700B chip capacitor
C6	43 pF ATC 100B chip capacitor
C7	20 pF ATC 100B chip capacitor
C8	1000 pF ATC 100C chip capacitor
C9	43 pF ATC 100B chip capacitor
C10	2200 pF ATC 100C chip capacitor
C11	1200 pF ATC 100C chip capacitor
R1, R2	1K ohm 1/4 watt chip resistor
R3, R4	1K ohm 1/2 watt axial lead resistor
L1	3 turns, 16 ga magnet wire, Id 3/8", 95 nH
FB1, FB2	Fair-Rite # 2743019447
B1	20 ga teflon coated wire thru copper tube OD 1/8"x 1.3"
T1	20 ga teflon coated wire thru 4 copper tubes OD 1/8"x 1.5"
TL1	.135" x .155" microstrip
TL2, TL3	.420" x .350" microstrip

Table 7. Bill of materials (continued)

Component	Description
TL4, TL5	.220" x .350" microstrip
TL6, TL7	.350" x .660" microstrip
TL8	.225" x .200" microstrip
TL9	.175" x .250" microstrip
Board	.062" FR-4

6 Circuit layout

Figure 12. Circuit layout photo

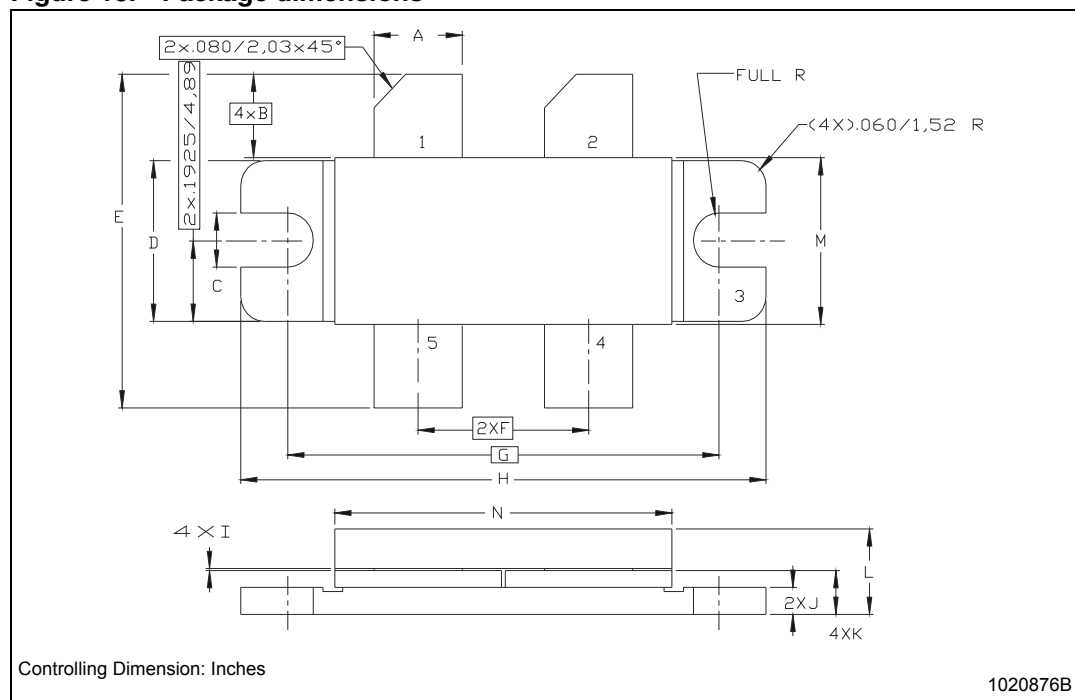


7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 8. M244 (.400 x .860 4/L BAL N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.59		5.84	0.220		0.230
B		5.08			0.200	
C	3.02		3.28	0.119		0.129
D	9.65		9.91	0.380		0.390
E	19.81		20.82	0.780		0.820
F	10.92		11.18	0.430		0.440
G		27.94			1.100	
H	33.91		34.16	1.335		1.345
I	0.10		0.15	0.004		0.006
J	1.52		1.78	0.060		0.070
K	2.59		2.84	0.102		0.112
L	4.83		5.84	0.190		0.230
M	10.03		10.34	0.395		0.407
N	21.59		22.10	0.850		0.870

Figure 13. Package dimensions


8 Revision history

Table 9. Document revision history

Date	Revision	Changes
09-Sep-2003	1	First release
03-Jul-2007	2	Specification upgrade
07-Aug-2007	3	Updated: Cover page, Figure 7, 8, 9, 10 on page 8
31-Oct-2007	4	Updated: Table 4: Static (per side) on page 4 Added Section 5: Test circuit on page 8 , Section 6: Circuit layout on page 10

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