High Voltage Fractional-N / Integer-N PLL Synthesizer

Preliminary Technical Data

ADF4150HV

FEATURES

Fractional-N synthesizer and integer-N synthesizer
High voltage charge pump: 6 V to 30 V
RF bandwidth to 4.4 GHz
Programmable divide-by-1/2/4/8 or 16 outputs
3.0 V to 3.6 V synthesizer power supply
Programmable dual-modulus prescaler of 4/5 or 8/9
Programmable output power level
Programmable charge pump currents
RF output mute function
3-wire serial interface
Analog and digital lock detect

APPLICATIONS

Wireless infrastructure
Microwave Point to Point / Multi-Point Radios
VSAT Radios
Test equipment
Military & Radar applications
Private/Land Mobile Radio

GENERAL DESCRIPTION

The ADF4150HV is a 4.4 GHz fractional-N or integer-N frequency synthesizer with an integrated high voltage charge pump. The synthesizer can be used to drive external wide band VCOs directly, removing the need for operational amplifiers to achieve higher tuning voltages. This simplifies design and reduces cost while improving phase noise, as active filter topologies tend to degrade phase noise when compared to passive filters.

The VCO frequency can be divided-by 1/2/4/8 or 16 to allow the user to generate RF output frequencies as low as 31.25 MHz. For applications that require isolation the RF output stage can be muted. The mute function is both pin and software controllable.

Control of all the on-chip registers is through a simple 3-wire interface. The charge pump operates off a supply ranging from 6V to 30V, while the rest of the device operates from 3.0 V to 3.6 V. The ADF4150HV can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

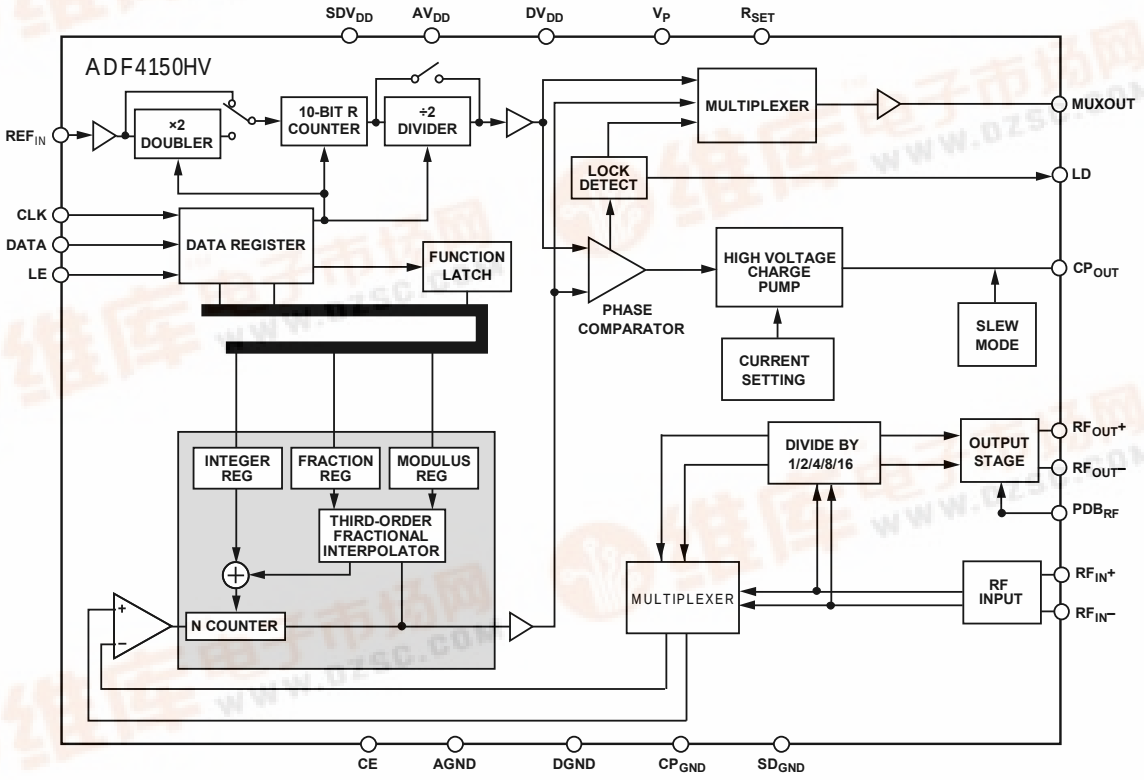

Figure 1.

Rev. PrI

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TABLE OF CONTENTS

REVISION HISTORY

SPECIFICATIONS

AV_{DD} = DV_{DD} = SD_{VDD} = 3.3 V ± 10%; V_P = 6.0 to 30 V; AGND = DGND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range is −40°C to +85°C.

Table 1.

REF_{IN} CHARACTERISTICS			
Input Frequency	10 to 250	MHz min to MHz max	For f < 10 MHz ensure slew rate > 21 V/µs
Input Sensitivity	0.7 to AV_{DD}	V p-p min to V p-p max	Biased at $AV_{DD}/2$[1]
Input Capacitance	5.0	pF max	
Input Current	±60	µA max	
RF INPUT CHARACTERISTICS			
RF Input Frequency (RF_{IN})	0.5/4.4	GHz min/max	−10 dBm ≤ RF Input Power ≤ 0 dBm For lower frequencies, ensure slew rate > 400 V/µs
PHASE DETECTOR			
Phase Detector Frequency[2]	30	MHz max	
HIGH VOLTAGE CHARGE PUMP			
I_{CP} Sink/Source			
High Value	400	uA typ	With R_{SET} = 5.1 kΩ
Low Value	50	uA typ	With R_{SET} = 5.1 kΩ
R_{SET} Range	3.3/10	kΩ	
High value vs. R_{SET}	204/618	uA typ	With R_{SET} = 10 kΩ/3.3 kΩ
Sink and Source Current Matching	2.5%	% typ	1.5 V ≤ V_{CP} ≤ V_P − 1.5 V, Vp = 20V
Sink and Source Current Matching	6%	% typ	1.5 V ≤ V_{CP} ≤ V_P − 1.5 V, Vp = 30V
Absolute ICP Accuracy	4%	% typ	
I_{CP} vs. V_{CP}	3%	% typ	1.5 V ≤ V_{CP} ≤ V_P − 1.5 V
I_{CP} vs. Temperature	2%	% typ	V_{CP} = V_P /2
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.0	V min	
Input Low Voltage, V_{INL}	0.6	V max	
Input Current, I_{INH}/I_{INL}	±1	µA max	
Input Capacitance, C_{IN}	3.0	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	DV_{DD} − 0.4	V min	CMOS output chosen
Output High Current, I_{OH}	500	µA max	
Output Low Voltage, V_O	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES			
AV_{DD}	3.0 to 3.6	V min to V max	
DV_{DD}, SD_{VDD},	AV_{DD}		
V_P	6.0 to 30	V min to V max	
I_P	2	mA max	V_P = 30V
DI_{DD} + AI_{DD}[3]	25	mA typ	
Output Dividers	6-24	mA typ	Each output divide by two consumes 6 mA
I_{RFOUT}[3]	32	mA typ	RF output stage is programmable
Low Power Sleep Mode	7	µA typ	
RF OUTPUT CHARACTERISTICS			
Minimum output Frequency Using RF Output Dividers	31.25	MHz	500 MHz VCO input and divide by 16 selected
Maximum RF_{IN} Frequency Using RF Output Dividers	4400	MHz max	
Harmonic Content (Second)	−19	dBc typ	Fundamental VCO output
Harmonic Content (Third)	−13	dBc typ	Fundamental VCO output

Harmonic Content (Second)	−20	dBc typ	Divided VCO output
Harmonic Content (Third)	−10	dBc typ	Divided VCO output
Output Power[4]	−4 to +5	dBm typ min to dBm typ max	Programmable in 3 dB steps
Output Power Variation	±1	dB typ	
NOISE CHARACTERISTICS[5]			
Normalized In-Band Phase Noise Floor[6]	−213	dBc/Hz typ	
In-Band Phase Noise	−101	dBc/Hz typ	@ 1 kHz offset from 1800 MHz carrier
Spurious Signals Due to PFD Frequency	−70	dBc typ	
Level of Signal With RF Mute Enabled	-40	dBm typ	

[1] AC coupling ensures $AV_{DD}/2$ bias.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] T_A = 25°C; AV_{DD} = DV_{DD} = 3.3 V; prescaler = 8/9; f_{REFIN} = 100 MHz; f_{PFD} = 25 MHz; f_{RF} = 2.5 GHz.
[4] Using 50 Ω resistors to V_{VCO}, into a 50 Ω load.
[5] This figure can be used to calculate phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output use the following formula: −213 + 10log(f_{PFD}) + 20 logN . The value given is the lowest noise mode.
[6] This figure can be used to calculate phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output use the following formula: −213 + 10log(f_{PFD}) + 20 logN . The value given is the lowest noise mode.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = SD_{VDD} = 3.3 V ± 10%; V_P = 6.0 to 30 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range is −40°C to +85°C.

Table 2.

Parameter	Limit (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLOCK setup time
t_3	10	ns min	DATA to CLOCK hold time
t_4	25	ns min	CLOCK high duration
t_5	25	ns min	CLOCK low duration
t_6	10	ns min	CLOCK to LE setup time
t_7	20	ns min	LE pulse width

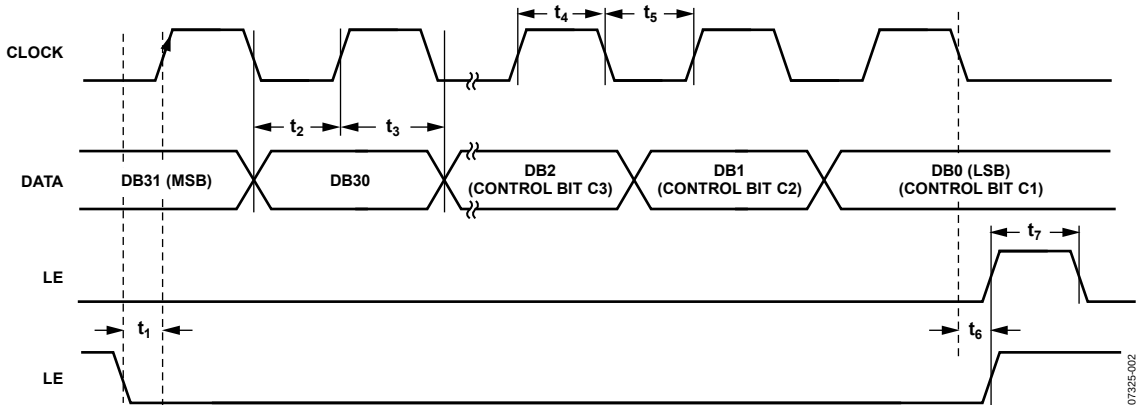


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to + 3.9 V
AV_{DD} to DV_{DD}	−0.3 V to + 0.3 V
V_P to GND[1]	−0.3 V to + 33 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance (Paddle-Soldered)	27.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] GND = AGND = DGND = 0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

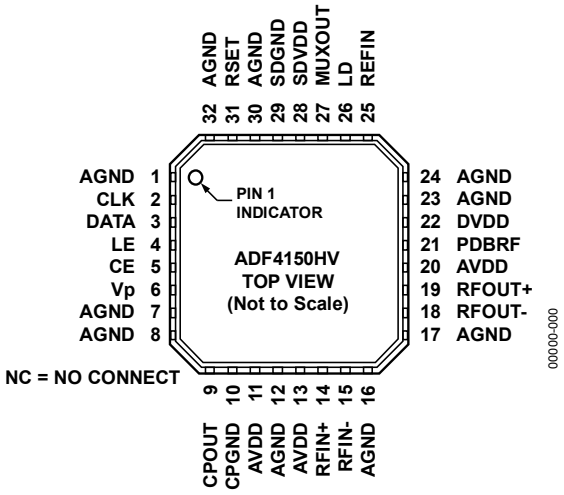
TRANSISTOR COUNT

23380 (CMOS) and 809 (bipolar)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Notes: The LFCSP package has an exposed paddle which must be connected to Ground.

Figure 3.

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7, 8, 12, 16, 17, 23, 24, 30, 32	AGND	Analog Ground. All ground pins should be tied together.
2	CLK	Serial clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
3	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSB's as control bits. This input is a high impedance CMOS input.
4	LE	Load Enable, CMOS input. When LE goes high, the data stored in the 32-bit shift register is loaded into the register that is selected by the three Control Bits.
5	CE	Chip Enable pin. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high on this pin powers up the device depending on the status of the power-down pins.
6	V_P	High Voltage Charge Pump Supply. Decoupling capacitors to the ground plane are to be placed as close as possible to the pin. The decoupling capacitor should have the appropriate voltage rating.
9	CPOUT	High Voltage Charge Pump Output. When enabled, this provides ± I_{CP} to the external passive loop filter. The output of the loop filter is connected to the voltage tuning port of your external VCO.
10	CPGND	High Voltage Charge Pump Ground. All ground pins should be tied together.
11, 13, 20	AVDD	Analog Power Supply. This pin ranges from 3.0V to 3.6V. Decoupling capacitors to the analog ground plane are to be placed as close as possible to this pin. AVDD must have the same value as DVDD.
14	RFIN+	Positive RF Input. The Output of the VCO or external prescaler should be ac-coupled into this pin.
15	RFIN -	Complementary RF Input. If only a single-ended input is required, this pin can be tied to Ground via a 100pF capacitor.
18	RFOUT-	Divided down output of RFIN-. This pin can be left unconnected if the divider functionality is not required.
19	RFOUT+	Divided down output of RFIN+. This pin can be left unconnected if the divider functionality is not required.
21	PDB_{RF}	RF Power Down. A logic low on this pin mutes the RF outputs. This function is also software controllable.
22	DVDD	Digital Power Supply. Decoupling capacitors to the ground plane are to be placed as close as possible to this pin. DVDD must have the same value as AVDD.
25	REFIN	Reference Input. This is a CMOS input with a nominal threshold of VDD/2 and a dc equivalent input resistance of 100 kΩ. This input can be driven from a crystal oscillator, TCXO or other reference.

26	LD	Lock Detect Output Pin. This pin outputs a logic high to indicate PLL lock. A logic low indicates loss of PLL lock.
27	MUXOUT	Multiplexer Output. This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference to be accessed externally.
28	SDVDD	Digital Sigma-Delta Modulator Power Supply. Decoupling capacitors to the ground plane are to be placed as close as possible to this pin. SDVDD must have the same value as AVDD.
29	SDGND	Digital Sigma-Delta Modulator Ground. All ground pins should be tied together.
31	R_{SET}	Connecting a resistor between this pin and GND sets the charge pump output current. The nominal voltage bias at the R_{SET} pin is 0.55V. the relationship between I_{CP} and R_{SET} is $I_{CP} = \frac{2.04}{R_{SET}}$ Where: R_{SET} = 5.1 kΩ I_{CP} = 400uA

TYPICAL PERFORMANCE CHARACTERISTICS

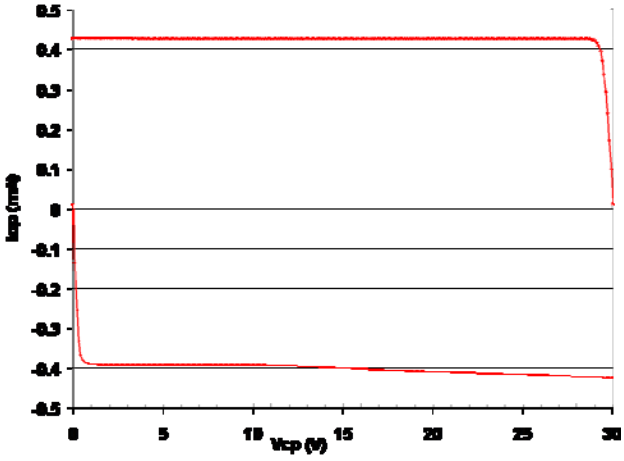


Figure 3. Charge Pump Output Characteristics, Vp = 30V, Icp = 400uA, Rset=5.1k

TBD

Figure 5.

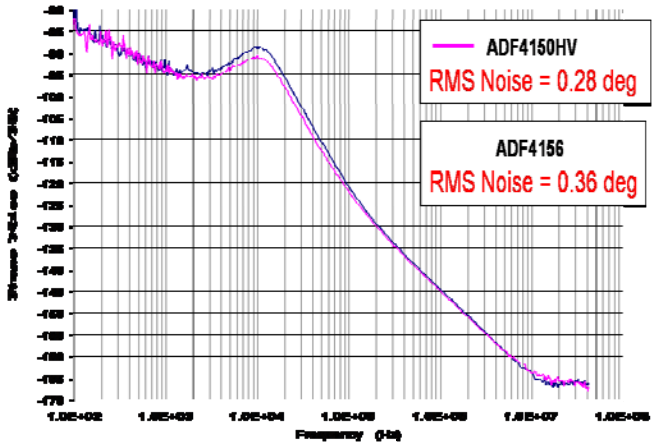


Figure 4. ADF4150HV vs. ADF4156 and active filter phase noise plot. Active filter implemented using OP27 op-amp. PFD = 20MHz, Loop Bandwidth = 10kHz, Icp = 300uA, Carrier Frequency = 1.7GHz, Vp = 28V

TBD

Figure 6.

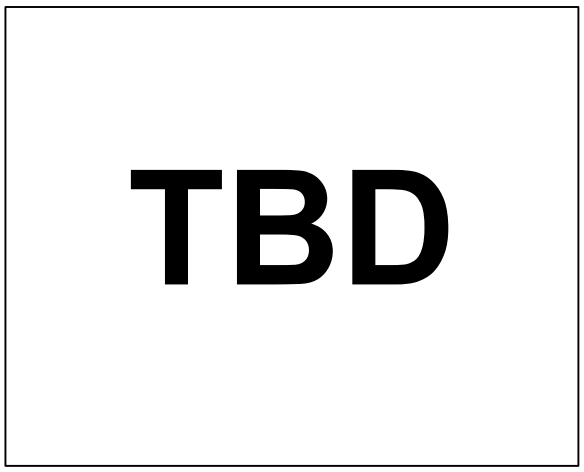


Figure 7.

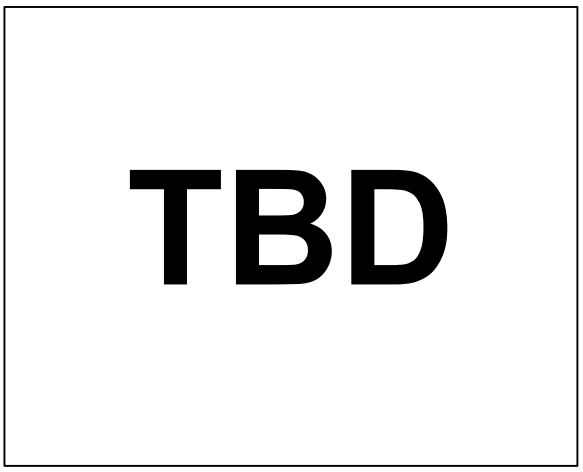


Figure 9.

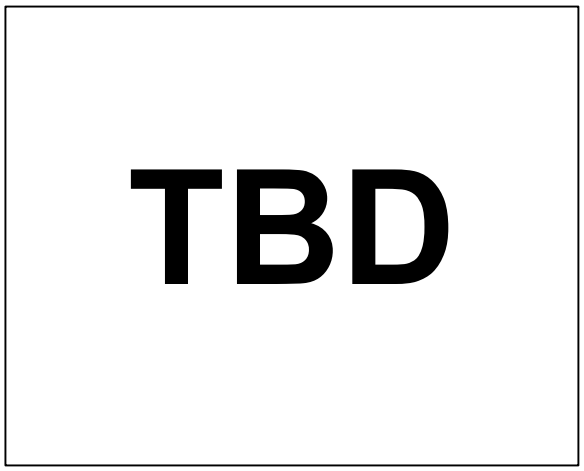


Figure 8.

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 10. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

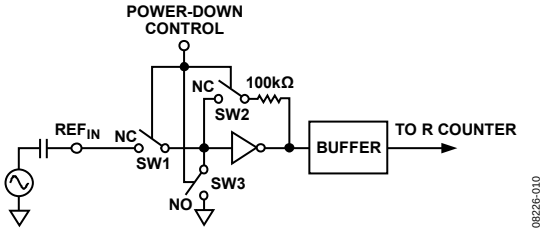


Figure 10. Reference Input Stage

RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. Division ratio is determined by INT, FRAC, and MOD values, which build up this divider.

INT, FRAC, MOD, AND R COUNTER RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency. See the RF Synthesizer—A Worked Example section for more information. The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

where:

RF_{OUT} is the output frequency of external voltage controlled oscillator (VCO).

INT is the preset divide ratio of the binary 16–bit counter (23 to 65535 for 4/5 prescaler, 75 to 65535 for 8/9 prescaler).

MOD is the preset fractional modulus (2 to 4095).

FRAC is the numerator of the fractional division (0 to MOD − 1).

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit.

T is the REF_{IN} divide-by-2 bit (0 or 1).

R is the preset divide ratio of the binary 10–bit programmable reference counter (1 to 1023).

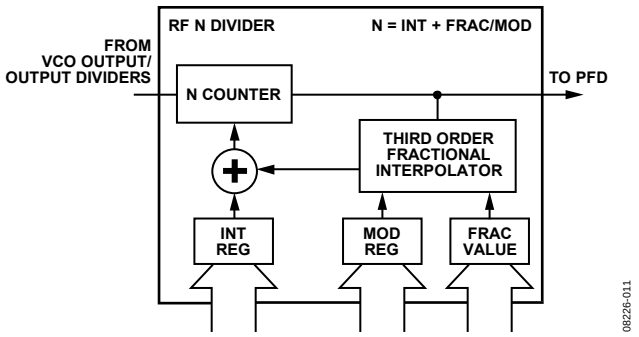


Figure 11. RF INT Divider

INT N MODE

If the FRAC = 0 and DB8 in Register 2 (LDF) is set to 1, the synthesizer operates in integer-N mode. The DB8 in Register 2 (LDF) should be set to 1 to get integer-N digital lock detect.

R COUNTER

The 10–bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND HIGH VOLTAGE CHARGE PUMP

The phase frequency detector (PFD) takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 12 is a simplified schematic of the phase frequency detector. The PFD includes a programmable delay element that sets the width of the antibacklash pulse, which can be set in Register5. This pulse ensures there is no dead zone in the PFD transfer function, and gives a consistent reference spur level. The high voltage charge pump is designed on an Analog Devices proprietary high voltage process and allows the charge pump to output voltages as high as 28.5V when run off a 30V supply. This removes the need for active filtering when interfacing to a high voltage VCO.

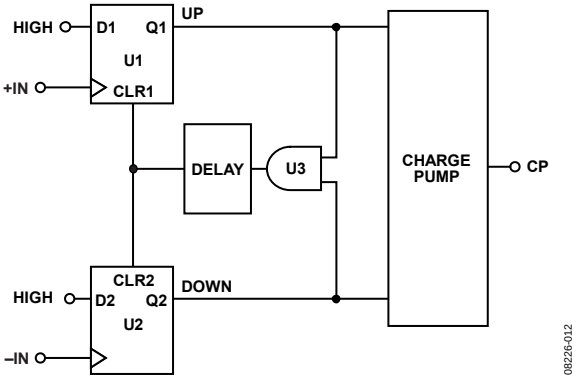


Figure 12. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4150HV allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 (for details, see Figure 18). Figure 13 shows the MUXOUT section in block diagram form.

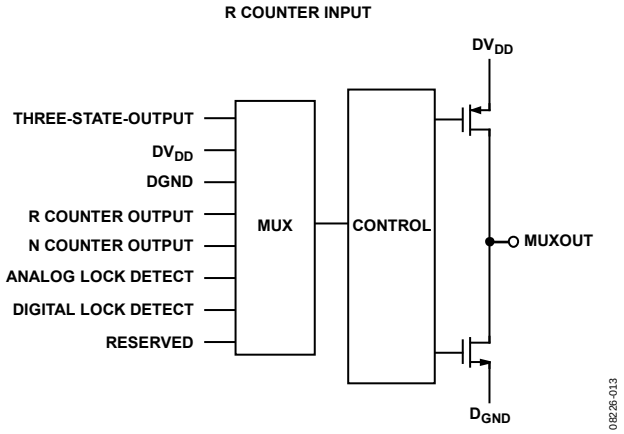


Figure 13. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4150HV digital section includes a 10-bit RF R counter, a 16–bit RF N counter, a 12-bit FRAC counter, and a 12-bit modulus counter. Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of six latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the shift register. These are the 3 LSBs, DB2, DB1, and DB0, as shown in Figure 2. The truth table for these bits is shown in Table . Figure 15 shows a summary of how the latches are programmed.

Table 5. C3, C2, and C1 Truth Table

Control Bits			
C3	**C2**	**C1**	**Register**
0	0	0	Register 0 (R0)
0	0	1	Register 1 (R1)
0	1	0	Register 2 (R2)
0	1	1	Register 3 (R3)
1	0	0	Register 4 (R4)
1	0	1	Register 5 (R5)

PROGRAM MODES

Figure 16 through Figure 21 show how the program modes are to be set up in the ADF4150HV.

A number of settings in the ADF4150HV are double buffered. These include the modulus value, phase value, R counter value, reference doubler, reference divide-by-2, and current setting. This means that two events have to occur before the part uses a new value of any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0. For example, any time the modulus value is updated, Register R0 must be written to, thus ensuring the modulus value is loaded correctly. Divider select in Register 4 (R4) is also double buffered, but only if DB13 of Register 2 (R2) is high.

OUTPUT STAGE

The RF_{OUT}+ and RF_{OUT}– pins of the ADF4150HV are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 14. To allow the user to optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable by Bit D2 and Bit D1 in Register 4 (R4). Four current levels may be set. These levels give output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm, respectively, using a 50 Ω resistor to AV_{DD} and ac coupling into a 50 Ω load. Alternatively, both outputs can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler (see the Output Matching section). If the outputs are used individually, the optimum output stage consists of a shunt inductor to AV_{DD}.

Another feature of the ADF4150HV is that the supply current to the RF output stage can be shut down until the part achieves lock as measured by the digital lock detect circuitry. This is enabled by the mute-till-lock detect (MTLD) bit in Register 4 (R4).

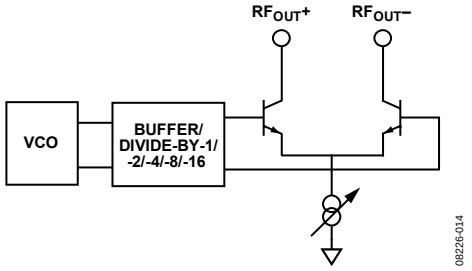


Figure 14. Output Stage

REGISTER MAPS

REGISTER 0

RESERVED	16-BIT INTEGER VALUE (INT)																12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED				PRESCALER	12-BIT PHASE VALUE (PHASE) DBR[1]												12-BIT MODULUS VALUE (MOD) DBR[1]												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	PR1	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3(0)	C2(0)	C1(1)

REGISTER 2

RESERVED	LOW NOISE AND LOW SPUR MODES		MUXOUT			REFERENCE DOUBLER DBR[1]	DBR[1] RDIV2	10-BIT R COUNTER DBR[1]									DOUBLE BUFF	RESERVED	DBR[1] CHARGE PUMP CURRENT SETTING			LDF	LDP	RESERVED	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L2	L1	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	0	CP3	CP2	CP1	U6	U5	1	U3	U2	U1	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED													RESERVED	RESERVED	CLK DIV MODE		12-BIT CLOCK DIVIDER VALUE												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED								FEEDBACK SELECT	DBB[2] DIVIDER SELECT			RESERVED									MTLD	RESERVED					RF OUTPUT ENABLE	OUTPUT POWER	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	D13	D12	D11	D10	BS8	BS7	BS6	BS5	BS4	BS3	BS2	BS1	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(1)	C2(0)	C1(0)

REGISTER 5

ABP PULSE WIDTH	CC ENABLE	RESERVED	RESERVED					LD PIN MODE	RESERVED	RESERVED		RESERVED																	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ABP2	ABP1	CE1	1	0	0	0	0	D15	D14	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C3(1)	C2(0)	C1(1)

[1] DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
[2] DBB = DOUBLE BUFFERED BITS—BUFFERED BY THE WRITE TO REGISTER 0, IF AND ONLY IF DB13 OF REGISTER 2 IS HIGH.

08226-015

Figure 15. Register Summary

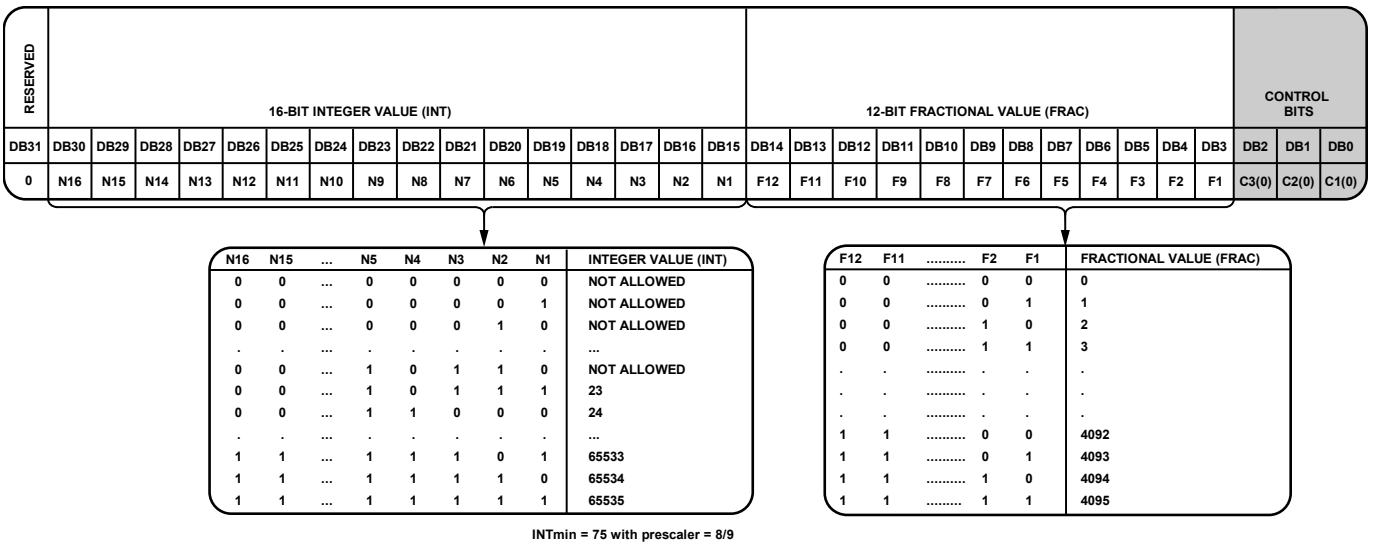


Figure 16. Register 0 (R0)

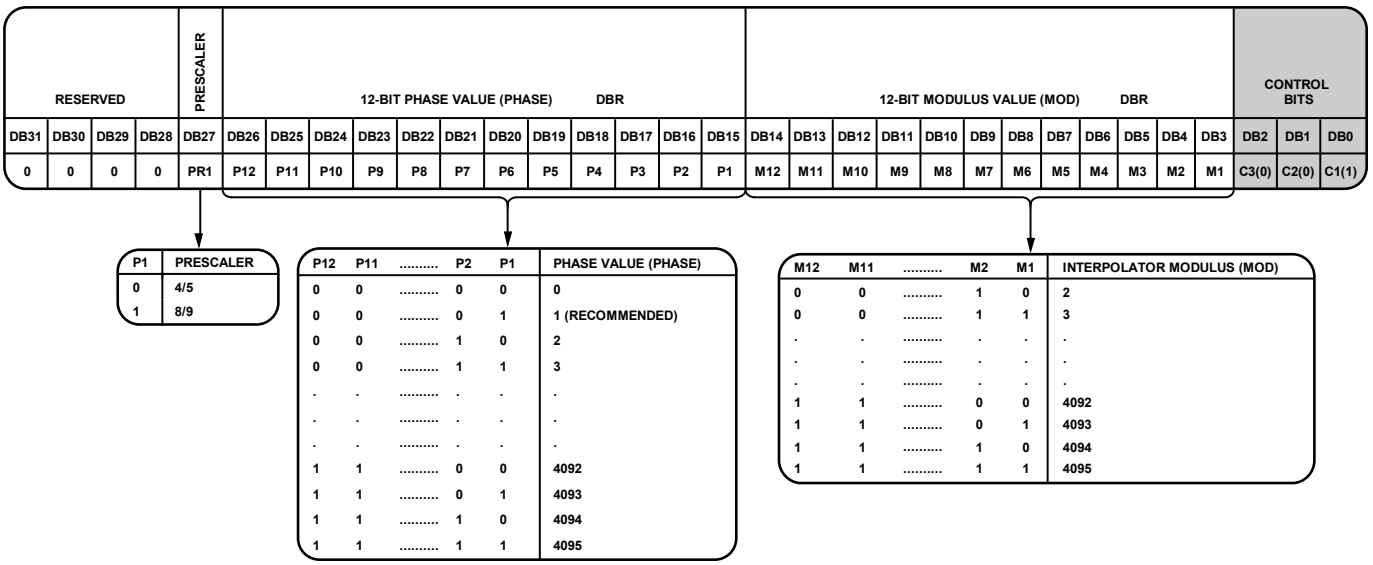


Figure 17. Register 1 (R1)

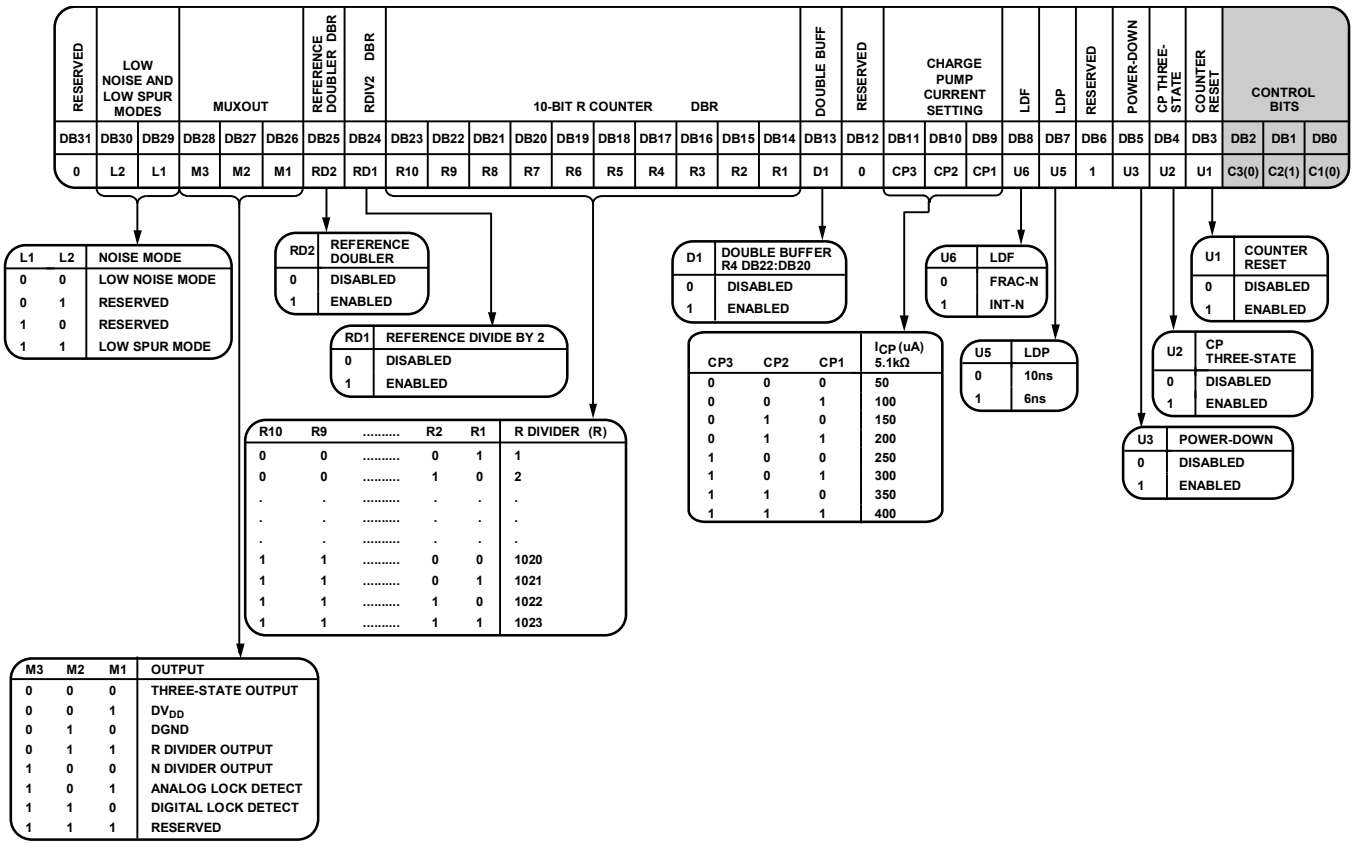


Figure 18. Register 2 (R2)

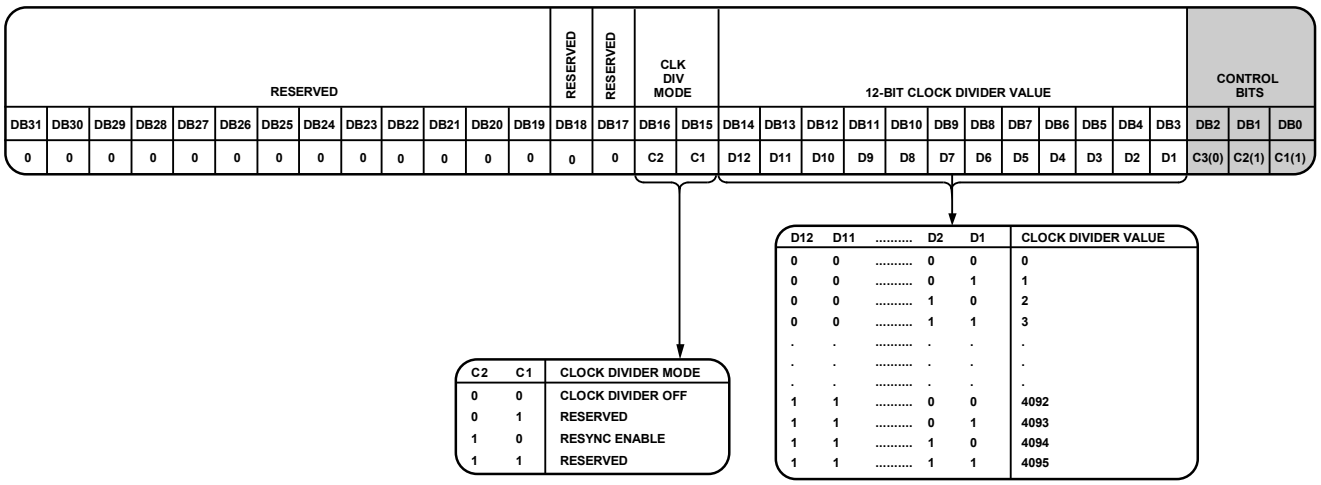


Figure 19. Register 3 (R3)

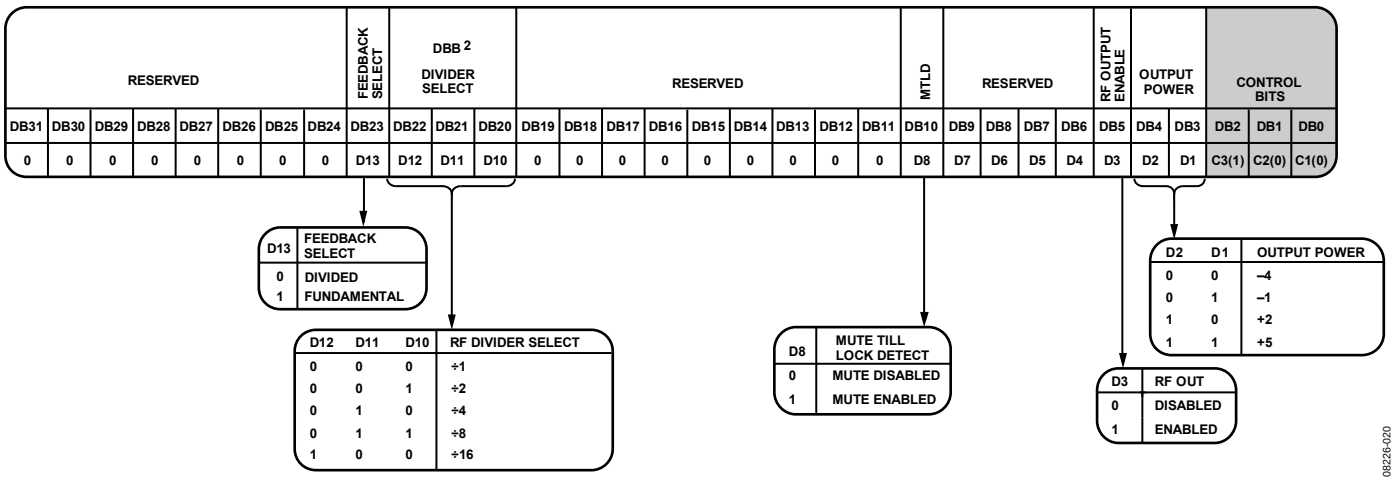


Figure 20. Register 4 (R4)

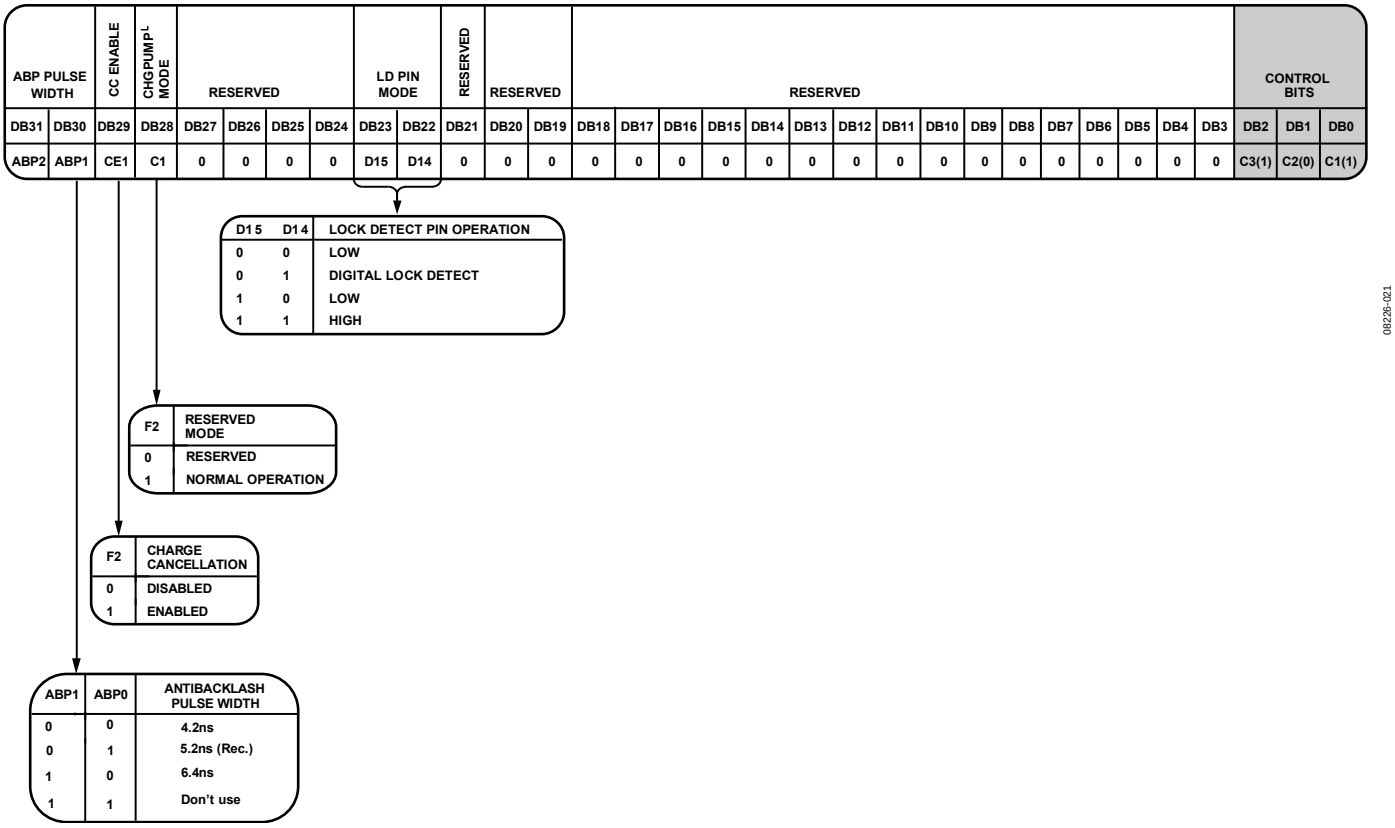


Figure 21. Register 5 (R5)

REGISTER 0

Control Bits

With Bits[C3:C1] set to 0, 0, 0, Register 0 is programmed. Figure 16 shows the input data format for programming this register.

16-Bit Integer Value (INT)

These 16 bits set the INT value, which determines the integer part of the feedback division factor. They are used in Equation 1 (see the INT, FRAC, MOD, and R Counter Relationship section). All integer values from 23 to 65,535 are allowed for 4/5 prescaler. For 8/9 prescaler, the minimum integer value is 75.

12-Bit Fractional Value(FRAC)

The 12 FRAC bits set the numerator of the fraction that is input to the Σ-Δ modulator. This, along with INT, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC values from 0 to MOD − 1 cover channels over a frequency range equal to the PFD reference frequency.

REGISTER 1

Control Bits

With Bits[C3:C1] set to 0, 0, 1, Register 1 is programmed. Figure 17 shows the input data format for programming this register.

Prescaler Value

The dual modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the VCO output to the PFD input.

Operating at CML levels, it takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4150HV above 3 GHz, this must be set to 8/9. The prescaler limits the INT value, where:

$P = 4/5$, $N_{MIN} = 23$
$P = 8/9$, $N_{MIN} = 75$

In the ADF4150HV, P1 in Register 1 sets the prescaler values.

12-Bit Phase Value (PHASE)

These bits control what is loaded as the phase word. The word must be less than the MOD value programmed in Register 1. The word is used to program the RF output phase from 0° to 360° with a resolution of 360°/MOD. See the Phase Resync section for more information. In most applications, the phase relationship between the RF signal and the reference is not important. In such applications, the PHASE value can be used to optimize the fractional and subfractional spur levels. See the Spur Consistency and Fractional Spur Optimization section for more information.

If neither the PHASE resync nor the spurious optimization functions are being used, it is recommended that the PHASE word be set to 1.

12-Bit Modulus Value (MOD)

This programmable register sets the fractional modulus. This is the ratio of the PFD frequency to the channel step resolution on the RF output. See the RF Synthesizer—A Worked Example section for more information.

REGISTER 2

Control Bits

With Bits[C3:C1] set to 0, 1, 0, Register 2 is programmed. Figure 18 shows the input data format for programming this register.

Low Noise and Spur Modes

The noise modes on the ADF4150HV are controlled by DB30 and DB29 in Register 2 (see Figure 18). The noise modes allow the user to optimize a design either for improved spurious performance or for improved phase noise performance.

When the lowest spur setting is chosen, dither is enabled. This randomizes the fractional quantization noise so it resembles white noise rather than spurious noise. As a result, the part is optimized for improved spurious performance. This operation would normally be used when the PLL closed-loop bandwidth is wide, for fast-locking applications. (Wide loop bandwidth is seen as a loop bandwidth greater than 1/10 of the RF_{OUT} channel step resolution (f_{RES})). A wide loop filter does not attenuate the spurs to the same level as a narrow loop bandwidth.

For best noise performance, use the lowest noise setting option. As well as disabling the dither, it also ensures that the charge pump is operating in an optimum region for noise performance. This setting is extremely useful where a narrow loop filter bandwidth is available. The synthesizer ensures extremely low noise and the filter attenuates the spurs. The typical performance characteristics give the user an idea of the trade-off in a typical W-CDMA setup for the different noise and spur settings.

MUXOUT

The on-chip multiplexer is controlled by Bits[DB28:DB26] (see Figure 18).

Reference Doubler

Setting DB25 to 0 feeds the REF_{IN} signal directly to the 10-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 10-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for the REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle in the lowest noise mode. The phase noise is insensitive to the REF_{IN} duty cycle when the doubler is disabled.

The maximum allowable REF_{IN} frequency when the doubler is enabled is 30 MHz.

RDIV2

Setting the DB24 bit to 1 inserts a divide-by-2 toggle flip-flop between the R counter and PFD, which extends the maximum REF_{IN} input rate. This function allows a 50% duty cycle signal to appear at the PFD input.

10-Bit R Counter

The 10-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

Double Buffer

DB13 enables or disables double buffering of Bits[DB22:DB20] in Register 4. The Divider Select section explains how double buffering works.

Current Setting

Bits[DB12:DB9] set the charge pump current setting. This should be set to the charge pump current that the loop filter is designed with (see Figure 18).

LDF

LDF controls the number of PFD cycles the lock detect circuit monitors to ascertain whether lock has been achieved or not. Setting DB8 to 0, sets the number of PFD cycles monitored to 40. Setting DB8 to 1 sets the number of PFD cycles to 5. It is recommended to set bit DB8 to 0 for fractional-N mode and set DB8 to 1 for integer-N mode.

Lock Detect Precision (LDP)

The Lock Detect Precision bit sets the comparison width in the lock detect circuit. When DB7 is set to 0, the comparison window is 10ns, when DB7 is set to 1 the window is 6ns. The lock detect circuit will go high when n consecutive PFD cycles are less than the comparison window value. In this case, n is set by the LDF bit DB8. So, for example, with DB7 = 0 and DB8 = 0 then 40 consecutive PFD cycles of 10 ns or less must occur before digital lock detect goes high. The recommended settings for the various modes are as follows:

Mode	DB8	DB7
Integer-N	1	1
Fractional-N Low Noise Mode	0	1
Fractional-N Low Spur Mode	0	0

Table 6. Recommended LDF/LDP bit settings.

Power-Down (PD)

DB5 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. When in software power-down mode, the part retains all information in its registers. Only if the supply voltages are removed are the register contents lost.

When a power-down is activated, the following events occur:

- The synthesizer counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RF_{OUT} buffers are disabled.
- The input register remains active and capable of loading and latching data.

Charge Pump (CP) Three-State

DB4 puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

Counter Reset

DB3 is the R counter and N counter reset bit for the ADF4150HV. When this bit is 1, the RF synthesizer N counter and R counter are held in reset. For normal operation, this bit should be set to 0.

REGISTER 3

Control Bits

With Bits[C3:C1] set to 0, 1, 1, Register 3 is programmed. Figure 19 shows the input data format for programming this register.

Clock Divider Mode

Bits[DB16:DB15] must be set to 1, 0 to activate PHASE resync or 0, 1 to activate fast lock. Setting Bits[DB16:DB15] to 0, 0 disables the clock divider. See Figure 19.

12-Bit Clock Divider Value

The 12-bit clock divider value sets the timeout counter for activation of PHASE resync. See the Phase Resync section for more information.

REGISTER 4

Control Bits

With Bits[C3: C1] set to 1, 0, 0, Register 4 is programmed. Figure 20 shows the input data format for programming this register.

Feedback Select

DB23 selects the feedback from VCO output to the N-counter. When this bit is set to 1, the signal is taken from the VCO directly. When this bit is set to 0, it is taken from the output of the output dividers. The dividers enable covering of the wide frequency band (137.5 MHz to 4.4 GHz). When the divider is enabled and the feedback signal is taken from the output, the RF output signals of two separately configured PLLs are in phase. This is useful in some applications where the positive interference of signals is required to increase the power.

Divider Select

Bits[DB22:DB20] select the value of the output divider (see Figure 20).

Mute-Till-Lock Detect

If DB10 is set to 1, the supply current to the RF output stage is shut down until the part achieves lock as measured by the digital lock detect circuitry.

RF Output Enable

DB5 enables or disables primary RF output, depending on the chosen value.

Output Power

DB4 and DB3 set the value of the primary RF output power level (see Figure 20).

REGISTER 5

Control Bits

With Bits[C3:C1] set to 1, 0, 1, Register 5 is programmed. Figure 21 shows the input data form for programming this register.

Lock Detect PIN Operation

Bits[DB23:DB22] set the operation of the lock detect pin (see Figure 21).

Charge Pump Mode

This bit (DB28) should be set to 1 for normal operation.

Charge Cancellation Mode Pulse Width

Setting DB29 to 1 enables charge pump charge cancellation. This has the effect of reducing PFD spurs in integer-N mode. In fractional-N mode, this bit should be set to 0.

Antibacklash Pulse Width

Bits [DB31:DB30] set the PFD antibacklash pulse width. The recommended value for fractional-N use is 5.2ns or setting [01]. By setting this bits to [00], the 4.2 ns pulse width is used and results in a phase noise and spur improvement in integer-N operation. For fractional-N mode it is not recommended to use this smaller setting.

INITIALIZATION SEQUENCE

The following sequence of registers is the correct sequence for initial power up of the ADF4150HV after the correct application of voltages to the supply pins:

- Register 5
- Register 4
- Register 3
- Register 2
- Register 1
- Register 0

RF SYNTHESIZER—A WORKED EXAMPLE

The following is an example how to program the ADF4150HV synthesizer:

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [f_{PFD}]/RF\ Divider \quad (3)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC is the fractionality.
MOD is the modulus.
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (4)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
T is the reference divide-by-2 bit (0 or 1).
R is the RF reference division factor.

For example consider the case where you want to program a 1.5GHz RF frequency output (RF_{OUT}) with a 500 kHz channel resolution (f_{RESOUT}) required on the RF output. The reference frequency input (REF_{IN}) is 25 MHz. You have a choice of using either a 1.5GHz VCO in fundamental mode or alternatively use a 3GHz VCO and enable the RF divider to 2, or a 6GHz VCO and set the RF divider to 4 etc.

When enabling the RF divider, you have the choice where to close the PLL loop, before or after the RF divider as depicted in Figure 22.

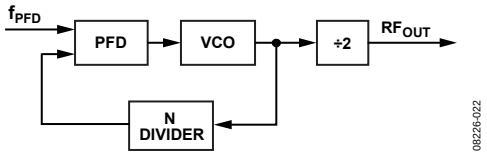


Figure 22. Loop Closed Before Output Divider

To minimize VCO feedthrough, let's choose the VCO at 3GHz. A channel resolution (f_{RESOUT}) of 500 kHz is required at the output of the RF divider. Therefore, channel resolution at the output of the VCO (f_{RES}) is to be twice the f_{RESOUT}, that is, 1 MHz.

$$MOD = REF_{IN}/f_{RES}$$
$$MOD = 25\ MHz/1\ MHz = 25$$

From Equation 4

$$f_{PFD} = [25\ MHz \times (1 + 0)/1] = 25\ MHz \quad (5)$$

$$1500.5\ MHz = 25\ MHz \times (INT + FRAC/25)/2 \quad (6)$$

where:
INT = 120, *FRAC* = 1, RF DIVIDER = 2

The ADF4150HV Evaluation software can be used to help determine integer and fractional values for a given setup and also determine the actual register settings to be programmed.

MODULUS

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution (f_{RES}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} sets the modulus to 65. This means the RF output resolution (f_{RES}) is the 200 kHz (13 MHz/65) necessary for GSM. With dither off, the fractional spur interval depends on the modulus values chosen (see Table).

REFERENCE DOUBLER AND REFERENCE DIVIDER

The reference doubler on-chip allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. It is important to note that the PFD cannot operate above 32 MHz due to a limitation in the speed of the Σ-Δ circuit of the N-divider.

The reference divide-by-2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency.

12-BIT PROGRAMMABLE MODULUS

Unlike most other fractional-N PLLs, the ADF4150HV allows the user to program the modulus over a 12-bit range. This means the user can set up the part in many different configurations for the application, when combined with the reference doubler and the 10-bit R counter.

For example, consider an application that requires 1.75 GHz RF and 200 kHz channel step resolution. The system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz directly to the PFD and programming the modulus to divide by 65. This results in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create 26 MHz from the 13 MHz input signal. The 26 MHz is then fed into the PFD programming the modulus to divide by 130. This also results in 200 kHz resolution and offers superior phase noise performance over the previous setup.

The programmable modulus is also very useful for multi-standard applications with different channel spacing requirements.

It is important that the PFD frequency remain constant (13 MHz in this case). This allows the user to design one loop filter for both setups without running into stability issues. It is important to remember that the ratio of the RF frequency to the PFD frequency principally affects the loop filter design, not the actual channel spacing.

SPURIOUS OPTIMIZATION

Narrow loop bandwidths can filter unwanted spurious signals, but these usually have a long lock time. A wider loop bandwidth achieves faster lock times, but a wider loop bandwidth may lead to increased spurious signals inside the loop bandwidth.

SPUR MECHANISMS

This section describes the three different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4150HV.

Fractional Spurs

The fractional interpolator in the ADF4150HV is a third-order Σ-Δ modulator (SDM) with a modulus (MOD) that is programmable to any integer value from 2 to 4095. In low spur mode (dither enabled), the minimum allowable value of MOD is 50. The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution
of f_{PFD}/MOD.

In low noise mode (dither off), the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is f_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the third-order modulator used in the ADF4150HV, the repeat length depends on the value of MOD, as listed in Table .

Table 7. Fractional Spurs with Dither Off

Condition (Dither Off)	Repeat Length	Spur Interval
If MOD is divisible by 2, but not 3	2 × MOD	Channel step/2
If MOD is divisible by 3, but not 2	3 × MOD	Channel step/3
If MOD is divisible by 6	6 × MOD	Channel step/6
Otherwise	MOD	Channel step

In low spur mode (dither on), the repeat length is extended to 2^{21} cycles, regardless of the value of MOD, which makes the quantization error spectrum look like broadband noise. This may degrade the in-band phase noise at the PLL output by as much as 10 dB. For lowest noise, dither off is a better choice, particularly when the final loop bandwidth is low enough to attenuate even the lowest frequency fractional spur.

Integer Boundary Spurs

Another mechanism for fractional spur creation is the interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (the point of a fractional-N synthesizer) spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth, therefore the name integer boundary spurs.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. PCB layout needs to ensure adequate isolation between VCO traces and the input reference to avoid a possible feedthrough path on the board.

SPUR CONSISTENCY AND FRACTIONAL SPUR OPTIMIZATION

With dither off, the fractional spur pattern due to the quantization noise of the SDM also depends on the particular phase word with which the modulator is seeded.

The phase word can be varied to optimize the fractional and subfractional spur levels on any particular frequency. Thus, a look-up table of phase values corresponding to each frequency can be constructed for use when programming the ADF4150HV.

If a look-up table is not used, keep the phase word at a constant value to ensure consistent spur levels on any particular frequency.

PHASE RESYNC

The output of a fractional-N PLL can settle to any one of the MOD phase offsets with respect to the input reference, where MOD is the fractional modulus. The phase resync feature in the ADF4150HV produces a consistent output phase offset with respect to the input reference. This is necessary in applications where the output phase and frequency are important, such as digital beam forming. See the Phase Programmability section for how to program a specific RF output phase when using phase resync.

Phase resync is enabled by setting Bit DB16, Bit DB15 in Register 3 to 1, 0. When PHASE resync is enabled, an internal timer generates sync signals at intervals of t_{SYNC} given by the following formula:

$$t_{SYNC} = CLK\_DIV\_VALUE \times MOD \times t_{PFD}$$

where:
t_{PFD} is the PFD reference period.
CLK_DIV_VALUE is the decimal value programmed in Bits[DB14:DB3] of Register 3 and can be any integer in the range of 1 to 4095.
MOD is the modulus value programmed in Bits[DB14:DB3] of Register 1 (R1).

When a new frequency is programmed, the second sync pulse after the LE rising edge is used to resynchronize the output phase to the reference. The t_{SYNC} time is to be programmed to a value that is at least as long as the worst-case lock time. This guarantees that the PHASE resync occurs after the last cycle slip in the PLL settling transient.

In the example shown in Figure 23, the PFD reference is 25 MHz and MOD is 125 for a 200 kHz channel spacing. t_{SYNC} is set to 400 µs by programming CLK_DIV_VALUE to 80.

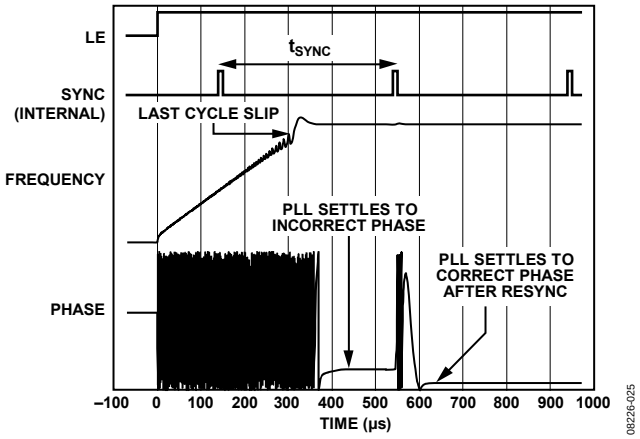


Figure 23. Phase Resync Example

Phase Programmability

The phase word in Register 1 controls the RF output phase. As this word is swept from 0 to MOD, the RF output phase sweeps over a 360° range in steps of 360°/MOD.

APPLICATIONS INFORMATION

ULTRA WIDEBAND PLL

The ADF4150HV when paired with an octave tuning range VCO provides an ultra wideband PLL function. This is achieved by the use of on-board RF dividers, which with an octave tuning range at the fundamental frequency, provides full frequency coverage with no gaps down to much lower frequencies. For example by using a 1GHz to 2GHz octave range VCO (like the Synergy DCYS100-200-12) you can obtain contiguous output frequencies from 62.5MHz to 2GHz at the ADF4150HV RF outputs, as shown in figure 24. A broadband output match is achieved by using a 27nH inductor in parallel with a 50 Ω resistor. See the output matching section for more information. Achieving such a wide output range can be useful where you want the same PLL hardware design to generate different system frequencies for each of your different hardware platforms.

MICROWAVE PLL

The ADF4150HV can be interfaced directly to a wide tuning range microwave VCO without the need for an active filter. Typically most microwave VCOs have a maximum tuning range of 15V. In this case you would set Vp on the ADF4150HV to be 16.5V or higher to ensure sufficient headroom in the charge pump. An external prescaler like the ADF5001 is required to divide down VCO frequencies that are above the maximum RF input frequency of 4.4GHz. In the application circuit shown in figure 25, the ADF5001 is dividing down the 16GHz VCO signal to 4GHz, which can then be input directly into the ADF4150HV RF inputs. The ADF5001 can be connected either single-ended or differentially to the ADF4150HV. It is recommended to use a differential connection for best performance and achieve maximum power transfer.

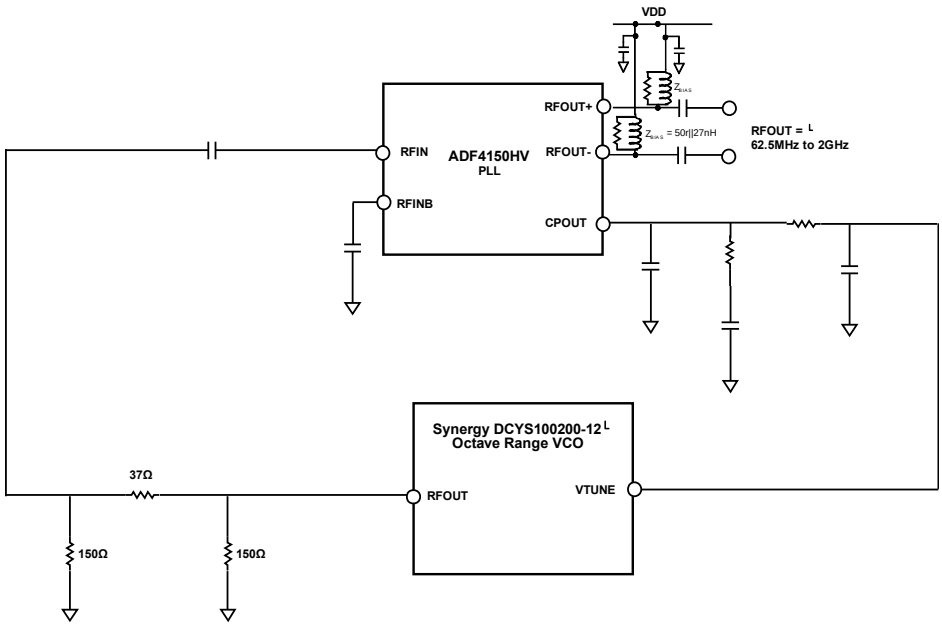


Figure 24. Ultra Wideband PLL using ADF4150HV and octave tuning range VCO

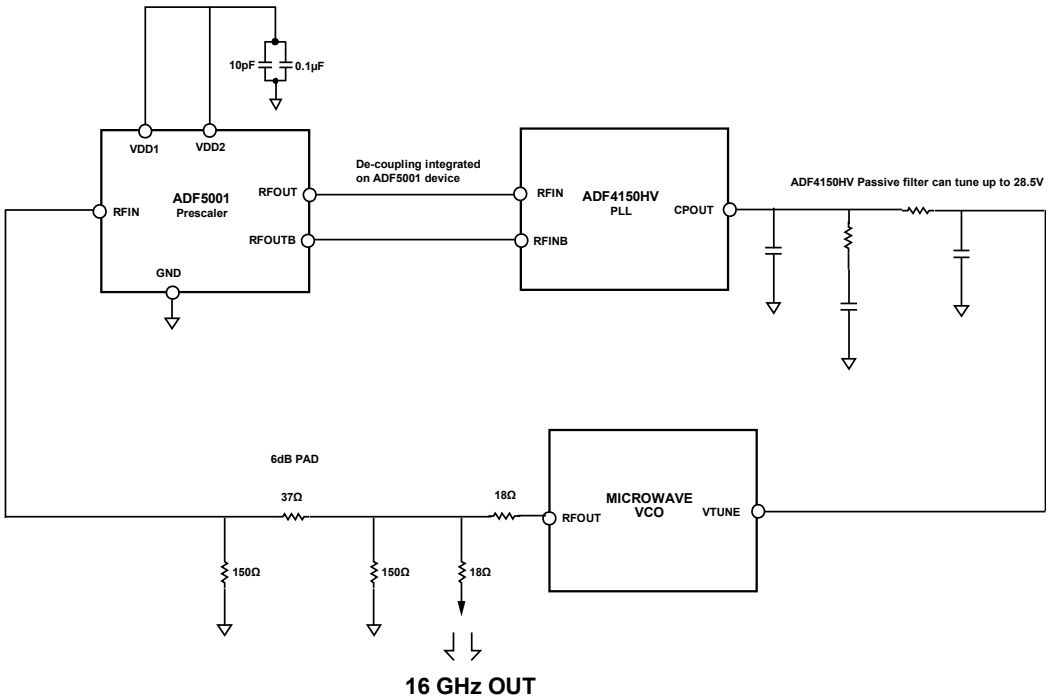


Figure 25. 16GHz Microwave PLL

INTERFACING

The ADF4150HV has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 32 bits that have been clocked into the appropriate register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table for the register address table.

ADu7020 Interface

Figure 26 shows the interface between the ADF4150HV and the ADuC70xx family of analog microcontrollers. The ADuC70xx family is based on an AMR7 core, although the same interface can be used with any 8051-based microcontroller.

The microcontoller is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4150HV needs a 32-bit word, which is accomplished by writing four 8-bit bytes from the microcontoller to the device. When the fourth byte has been written, the LE input should be brought high to complete the transfer.

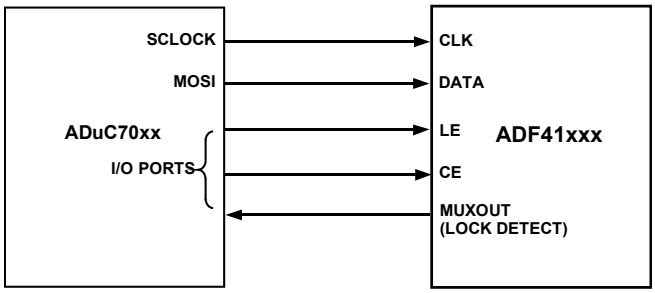


Figure 26. ADuC70XX to ADF4150HV Interface

When operating in the mode described, the maximum SPI transfer rate of the ADuC7023 is 20Mbps. This means that the maximum rate at which the output frequency can be changed is 833 kHz. If using a faster SPI clock just make sure the SPI timing requirements listed in Table 1 are adhered to.

Blackfin BF527 Interface

Figure 27 shows the interface between the ADF4150HV and a Blackfin ADSP-BF527 digital signal processor (DSP). The ADF4150HV needs a 32-bit serial word for each latch write. The easiest way to accomplish this using the Blackfin family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

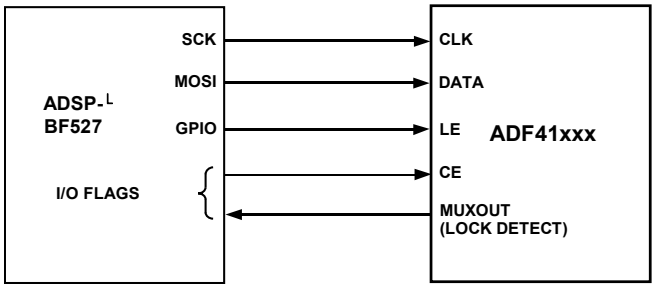


Figure 27. ADSP-21xx to ADF4150HV Interface

Set up the word length for 8 bits and use four memory locations for each 32-bit word. To program each 32-bit latch, store the 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer. As in the microcontroller case just make sure the clock speeds are within the maximum limits outlined in table 1.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the chip scale package (CP-32-11) are rectangular. The PCB pad for these is to be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land is to be centered on the pad. This ensures the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad.

The thermal pad on the PCB is to be at least as large as the exposed pad. On the PCB, there is to be a minimum clearance of 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve the thermal performance of the package. If vias are used, they are to be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter is to be between 0.3 mm and 0.33 mm, and the via barrel is to be plated with one ounce copper to plug the via.

OUTPUT MATCHING

There are a number of ways to match the output of the ADF4150HV for optimum operation; the most basic is to use a 50 Ω resistor to AV_{DD}. A dc bypass capacitor of 100 pF is connected in series as shown in Figure 28. Because the resistor is not frequency dependent, this provides a good broadband match. The output power in this circuit into a 50 Ω load typically gives values chosen by Bits[DB4:DB3] in Register 4 (R4).

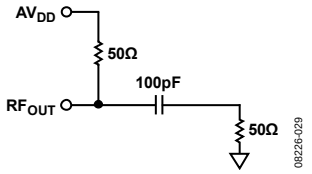


Figure 28. Simple ADF4150HV Output Stage

A better solution is to use a shunt inductor (acting as an RF choke) to AV_{DD}. This gives a better match and, therefore, more output power.

Experiments indicate that the circuit shown in Figure 29 provides an excellent match to 50 Ω for frequencies above 1GHz. The maximum output power in that case is about 7 dBm. For frequencies below 1GHz, the pull-up or choke inductor should be increased in value. A 27nH value in parallel with a 50 Ω resistor gives a good broadband match from 250MHz to 4.4GHz. The inductor can be increased further for operation below 250MHz. Both single-ended architectures can be examined using the EVAL-ADF4150HVEB1Z evaluation board.

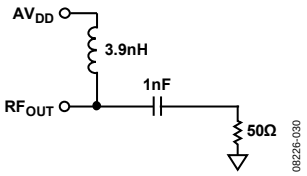
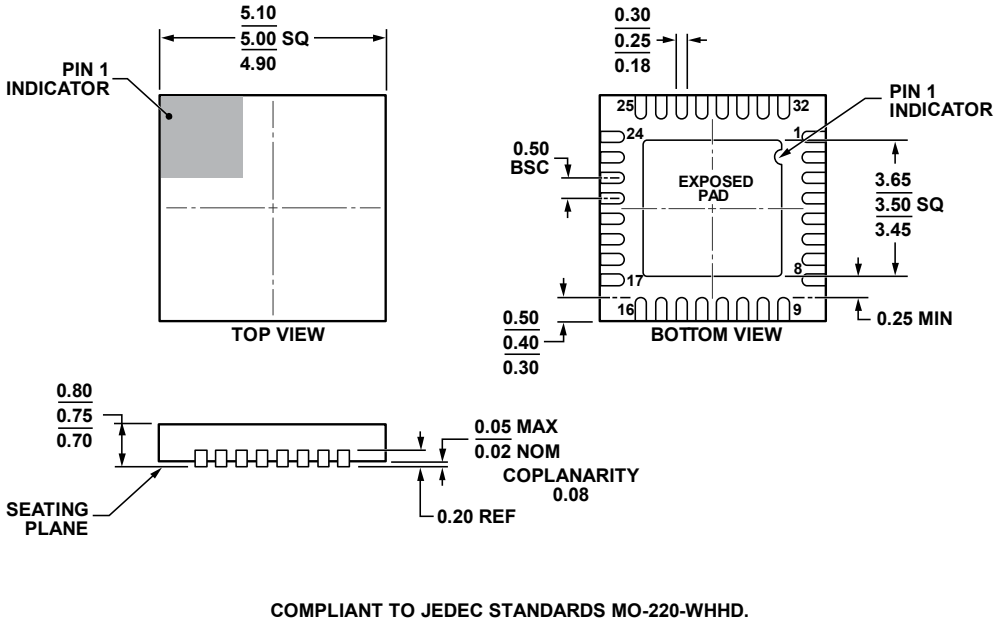


Figure 29. Optimum ADF4150HV Output Stage

If differential outputs are not needed, the unused output can be terminated or combined with both outputs using a balun.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 4. 32-Lead Lead Frame Chip Scale Package (CP-32-11).
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4150HVBCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-11
ADF4150HVBCPZ-RL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-11
EVAL-ADF4150HV-EB1Z		Evaluation Board	
EVAL-ADF4150HV-EB1ZU1		Pre-Release Evaluation Board	

NOTES