# 8-BIT Fm+ I2C-BUS CONSTANT-CURRENT LED SINK DRIVER

## FEATURES

- **Eight LED Drivers (Each Output Programmable At Off, On, Programmable LED Brightness, Programmable Group Dimming/Blinking Mixed With Individual LED Brightness**
- **Eight Constant-Current Open-Drain Output Channels**
- **256-Step (8-Bit) Linear Programmable Brightness Per LED Output Varying From Fully Off (Default) to Maximum Brightness Using a 97-kHz PWM Signal**
- **256-Step Group Brightness Control Allows General Dimming (Using a 190-Hz PWM Signal From Fully Off to Maximum Brightness (Default)**
- **256-Step Group Blinking With Frequency Programmable From 24 Hz to 10.73 s and Duty Cycle From 0% to 99.6%**
- **Four Hardware Address Pins Allow 14 TLC59108 Devices to be Connected to the Same I2C Bus**
- **Four Software-Programmable I2C Bus Addresses (One LED Group Call Address and Three LED Sub Call Addresses) Allow Groups of Devices to be Addressed at the Same Time in Any Combination. For Example, One Register Used for All Call, so That All the TLC59108 Devices on the I2C Bus Can be Addressed at the Same Time, and the Second Register Can be Used for Three Different Addresses so That One-Third of All Devices on the Bus Can be Addressed at the Same Time in a Group.**
- **Software Enable and Disable for I2C Bus Address**

- **Software Reset Feature (SWRST Call) Allows Device to be Reset Through I2C Bus**
- **Up to 14 Possible Hardware-Adjustable Individual I2C Bus Addresses Per Device, So That Each Device Can Be Programmed**
- **Open-Load/Overtemperature Detection Mode to Detect Individual LED Errors**
- **Output State Change Programmable on the Acknowledge or the Stop Command to Update Outputs Byte by Byte or All at the Same Time (Default to Change on Stop)**
- **Output Current Adjusted Through an External Resistor**
- **Constant Output Current Range: 10 mA to 120 mA**
- **Maximum Output Voltage: 17 V**
- **25-MHz Internal Oscillator Requires No External Components**
- **1-MHz Fast Mode Plus Compatible I2C Bus Interface With 30-mA High Drive Capability on SDA Output for Driving High-Capacitive Buses**
- **Internal Power-On Reset**
- **Noise Filter on SCL/SDA Inputs**
- **No Glitch on Power Up**
- **Active-Low Reset**
- **Supports Hot Insertion**
- **Low Standby Current**
- **3.3-V or 5-V Supply Voltage**
- **5.5-V Tolerant Inputs**
- **Offered in 20-Pin TSSOP (PW) and QFN (RGY) Packages**
- **−40°C to 85°C Operation**

## DESCRIPTION/ORDERING INFORMATION

The TLC59108 is an I2C bus controlled 8-bit LED driver that is optimized for red/green/blue/amber (RGBA) color mixing and backlight application for amusement products. Each LED output has its own 8-bit resolution (256 steps) fixed-frequency individual PWM controller that operates at 97 kHz, with a duty cycle that is adjustable from 0% to 99.6%. The individual PWM controller allows each LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds, with a duty cycle that is adjustable from 0% to 99.6%. The group PWM controller dims or blinks all LEDs with the same value.

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## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Each LED output can be off, on (no PWM control), or set at its individual PWM controller value at both individual and group PWM controller values.

The TLC59108 is one of the first LED controller devices in a new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and longer, more densely populated bus operation (up to 4000 pF).

Software programmable LED group and three Sub Call $I^2C$ bus addresses allow all or defined groups of TLC59108 devices to respond to a common $I^2C$ bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing $I^2C$ bus commands. Four hardware address pins allow up to 14 devices on the same bus.
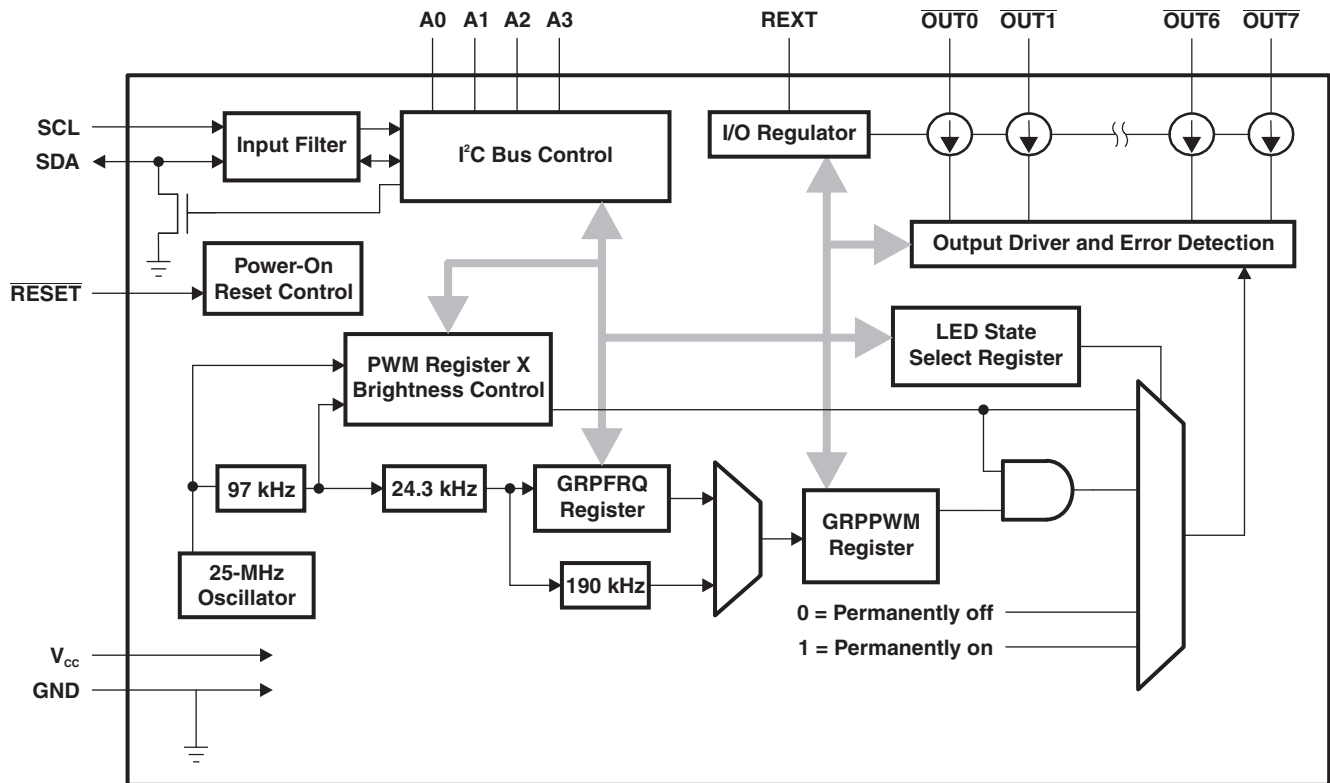
The Software Reset (SWRST) call allows the master to perform a reset of the TLC59108 through the $I^2C$ bus, identical to the Power-On Reset (POR) that initializes the registers to their default state, causing the outputs to be set high (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.
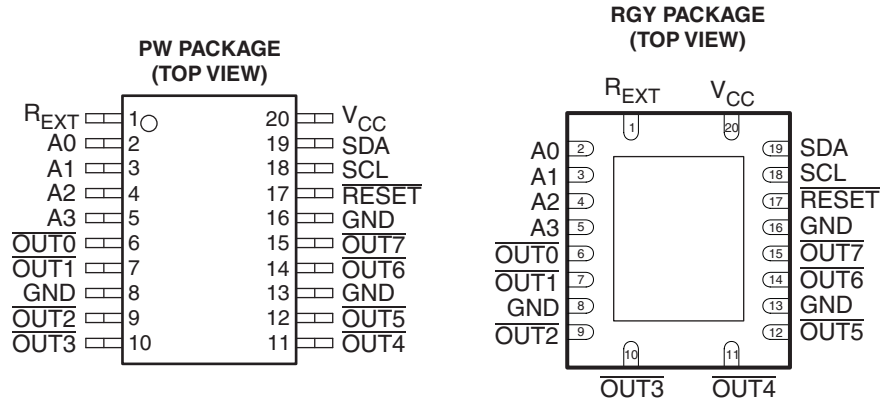
### ORDERING INFORMATION[1]

| $T_A$ | PACKAGE[2] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | TLC59108IRGYR | Y59108 |
| | TSSOP – PW | Reel of 2000 | TLC59108IPWR | Y59108 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

### BLOCK DIAGRAM

**PW PACKAGE**
**(TOP VIEW)**

```
R_EXT   1  ○      20   V_CC
A0      2         19   SDA
A1      3         18   SCL
A2      4         17   RESET
A3      5         16   GND
OUT0    6         15   OUT7
OUT1    7         14   OUT6
GND     8         13   GND
OUT2    9         12   OUT5
OUT3   10         11   OUT4
```

**RGY PACKAGE**
**(TOP VIEW)**

```
        R_EXT    V_CC
          1       20
A0   2                   19   SDA
A1   3                   18   SCL
A2   4                   17   RESET
A3   5                   16   GND
OUT0 6                   15   OUT7
OUT1 7                   14   OUT6
GND  8                   13   GND
OUT2 9                   12   OUT5
         10      11
        OUT3    OUT4
```

## TERMINAL FUNCTIONS

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | PW/RGY PIN NO. | | |
| A0 | 2 | I | Address input 0 |
| A1 | 3 | I | Address input 1 |
| A2 | 4 | I | Address input 2 |
| A3 | 5 | I | Address input 3 |
| GND | 8, 13, 16 | | Ground |
| OUT0 | 6 | O | Constant current output 0, LED on at low |
| OUT1 | 7 | O | Constant current output 1, LED on at low |
| OUT2 | 9 | O | Constant current output 2, LED on at low |
| OUT3 | 10 | O | Constant current output 3, LED on at low |
| OUT4 | 11 | O | Constant current output 4, LED on at low |
| OUT5 | 12 | O | Constant current output 5, LED on at low |
| OUT6 | 14 | O | Constant current output 6, LED on at low |
| OUT7 | 15 | O | Constant current output 7, LED on at low |
| RESET | 17 | I | Active-low reset input |
| R_EXT | 1 | | Input terminal used to connect an external resistor for setting up all output currents |
| SCL | 18 | I | Serial clock input |
| SDA | 19 | I/O | Serial data input/output |
| V_CC | 20 | | Power supply |

(1)  I = input, O = output

## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | 0 | 7 | V |
| $V_I$ | Input voltage range | −0.4 | 7 | V |
| $V_O$ | Output voltage range | −0.5 | 20 | V |
| $I_O$ | Output current |  | 120 | mA |
| $\theta_{JA}$ | Thermal impedance, junction to free air[2] |  | 83 | °C/W |
| $T_J$ | Junction temperature range | −40 | 150 | °C |
| $T_{stg}$ | Storage temperature range | −55 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS[1]

|  |  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage |  |  | 3 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | SCL, SDA, $\overline{RESET}$, A0, A1, A2, A3 |  | $0.7 \times V_{CC}$ | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | SCL, SDA, $\overline{RESET}$, A0, A1, A2, A3 |  | 0 | $0.3 \times V_{CC}$ | V |
| $V_O$ | Supply voltage to output pins | $\overline{OUT0}$ to $\overline{OUT7}$ |  |  | 17 | V |
| $I_{OL}$ | Low-level output current sink | SDA | $V_{CC}$ = 3 V |  | 20 | mA |
|  |  |  | $V_{CC}$ = 3 V |  | 30 | |
| $I_O$ | Output current | $\overline{OUT0}$ to $\overline{OUT7}$ |  | 5 | 120 | mA |
| $T_A$ | Operating free-air temperature |  |  | −40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation.

## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 3 V to 5.5 V, $T_A$ = −40°C to 85°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_I$ | Input/output leakage current | SCL, SDA, A0, A1, A2, A3, $\overline{RESET}$ | $V_I$ = $V_{CC}$ or GND | | | | ±0.3 | μA |
| | Output leakage current | $\overline{OUT0}$ to $\overline{OUT7}$ | $V_O$ = 17 V, $T_J$ = 25°C | | | | 0.5 | μA |
| $V_{POR}$ | Power-on reset voltage | | | | | 2.5 | | V |
| $I_{OL}$ | Low-level output current | SDA | $V_{CC}$ = 3 V, $V_{OL}$ = 0.4 V | | 20 | | | mA |
| | | | $V_{CC}$ = 5 V, $V_{OL}$ = 0.4 V | | 30 | | | |
| $I_{O(1)}$ | Output current 1 | $\overline{OUT0}$ to $\overline{OUT7}$ | $V_O$ = 0.6 V, $R_{ext}$ = 720 Ω, CG = 0.992 | | | 26 | | mA |
| | Output current error | $\overline{OUT0}$ to $\overline{OUT7}$ | $I_O$ = 26 mA, $V_O$ = 0.6 V, $R_{ext}$ = 720 Ω, $T_J$ = 25°C | | | | ±8 | % |
| | Output channel to channel current error | $\overline{OUT0}$ to $\overline{OUT7}$ | $I_O$ = 26 mA, $V_O$ = 0.6 V, $R_{ext}$ = 720 Ω, $T_J$ = 25°C | | | | ±3 | % |
| $I_{O(2)}$ | Output current 2 | $\overline{OUT0}$ to $\overline{OUT7}$ | $V_O$ = 0.8 V, $R_{ext}$ = 360 Ω, CG = 0.992 | | | 52 | | mA |
| | Output current error | $\overline{OUT0}$ to $\overline{OUT7}$ | $I_O$ = 52 mA, $V_O$ = 0.8 V, $R_{ext}$ = 360 Ω, $T_J$ = 25°C | | | | ±8 | % |
| | Output channel to channel current error | $\overline{OUT0}$ to $\overline{OUT7}$ | $I_O$ = 52 mA, $V_O$ = 0.8 V, $R_{ext}$ = 360 Ω, $T_J$ = 25°C | | | | ±3 | % |
| $I_{OUT}$ vs $V_{OUT}$ | Output current vs output voltage regulation | $\overline{OUT0}$ to $\overline{OUT7}$ | $V_O$ = 1 V to 3 V, $I_O$ = 26 mA | | | ±0.1 | | %/V |
| | | | $V_O$ = 3 V to 5.5 V, $I_O$ = 26 mA to 120 mA | | | ±1 | | |
| $I_{OUT,Th1}$ | Threshold current 1 for error detection | $\overline{OUT0}$ to $\overline{OUT7}$ | $I_{OUT,target}$ = 26 mA | | | 0.5 × $I_{TARGET}$ | | % |
| $I_{OUT,Th2}$ | Threshold current 2 for error detection | $\overline{OUT0}$ to $\overline{OUT7}$ | $I_{OUT,target}$ = 52 mA | | | 0.5 × $I_{TARGET}$ | | % |
| $I_{OUT,Th3}$ | Threshold current 3 for error detection | $\overline{OUT0}$ to $\overline{OUT7}$ | $I_{OUT,target}$ = 104 mA | | | 0.5 × $I_{TARGET}$ | | % |
| $T_{SD}$ | Overtemperature shutdown[2] | | | | 150 | 175 | 200 | °C |
| $T_{HYS}$ | Restart hysteresis | | | | | 15 | | °C |
| $C_i$ | Input capacitance | SCL, A0, A1, A2, A3, $\overline{RESET}$ | $V_I$ = $V_{CC}$ or GND | | | | 5 | pF |
| $C_{io}$ | Input/output capacitance | SDA | $V_I$ = $V_{CC}$ or GND | | | | 5 | pF |
| $I_{CC}$ | Supply current | | $V_{CC}$ = 5.5 V | $\overline{OUT0}$ to $\overline{OUT7}$ = OFF, $R_{ext}$ = Open | | | 17 | mA |
| | | | | $\overline{OUT0}$ to $\overline{OUT7}$ = OFF, $R_{ext}$ = 720 Ω | | | 20 | |
| | | | | $\overline{OUT0}$ to $\overline{OUT7}$ = OFF, $R_{ext}$ = 360 Ω | | | 23 | |
| | | | | $\overline{OUT0}$ to $\overline{OUT7}$ = OFF, $R_{ext}$ = 180 Ω | | | 28 | |
| | | | | $\overline{OUT0}$ to $\overline{OUT7}$ = ON, $R_{ext}$ = 720 Ω | | | 21 | |
| | | | | $\overline{OUT0}$ to $\overline{OUT7}$ = ON, $R_{ext}$ = 360 Ω | | | 23 | |
| | | | | $\overline{OUT0}$ to $\overline{OUT7}$ = ON, $R_{ext}$ = 180 Ω | | | 28 | |

(1) All typical values are at $T_A$ = 25°C.
(2) Specified by design

## TIMING REQUIREMENTS

$T_A = -40°C$ to 85°C

| | | STANDARD MODE I²C BUS | | FAST MODE I²C BUS | | FAST MODE PLUS I²C BUS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **I²C Interface** | | | | | | | | |
| $f_{SCL}$ | SCL clock frequency[1] | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| $t_{BUF}$ | I²C bus free time between stop and start | 4.7 | | 1.3 | | 0.5 | | µs |
| $t_{HD;STA}$ | Hold time (repeated) Start condition | 4 | | 0.6 | | 0.26 | | µs |
| $t_{SU;STA}$ | Set-up time for a repeated Start condition | 4.7 | | 0.6 | | 0.26 | | µs |
| $t_{SU;STO}$ | Set-up time for Stop condition | 4 | | 0.6 | | 0.26 | | µs |
| $tHD;DAT$ | Data hold time | 0 | | 0 | | 0 | | ns |
| $t_{VD;ACK}$ | Data valid acknowledge time[2] | 0.3 | 3.45 | 0.1 | 0.9 | 0.05 | 0.45 | µs |
| $t_{VD;DAT}$ | Data valid time[3] | 0.3 | 3.45 | 0.1 | 0.9 | 0.05 | 0.45 | µs |
| $t_{SU;DAT}$ | Data set-up time | 250 | | 100 | | 50 | | ns |
| $t_{LOW}$ | Low period of the SCL clock | 4.7 | | 1.3 | | 0.5 | | µs |
| $t_{HIGH}$ | High period of the SCL clock | 4 | | 0.6 | | 0.26 | | µs |
| $t_f$ | Fall time of both SDA and SCL signals[4][5] | | 300 | $20+0.1C_b$[6] | 300 | | 120 | ns |
| $t_r$ | Rise time of both SDA and SCL signals | | 1000 | $20+0.1C_b$[6] | 300 | | 120 | ns |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by the input filter[7] | | 50 | | 50 | | 50 | ns |
| **Reset** | | | | | | | | |
| $t_W$ | Reset pulse width | 10 | | 10 | | 10 | | ns |
| $t_{REC}$ | Reset recovery time | 0 | | 0 | | 0 | | ns |
| $t_{RESET}$ | Time to reset[8][9] | 400 | | 400 | | 400 | | ns |

(1) Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either SDA or SCL is held low for a minimum of 25 ms. Disable bus time-out feature for DC operation.
(2) $t_{VD;ACK}$ = time for Acknowledgement signal from SCL low to SDA (out) low.
(3) $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.
(4) A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the VIL of the SCL signal) in order to bridge the undefined region of SCLs falling edge.
(5) The maximum tf for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time ($t_f$) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.
(6) $C_b$ = total capacitance of one bus line in pF.
(7) Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns
(8) Resetting the device while actively communicating on the bus may cause glitches or errant Stop conditions.
(9) Upon reset, the full delay will be the sum of $t_{RESET}$ and the RC time constant of the SDA bus.
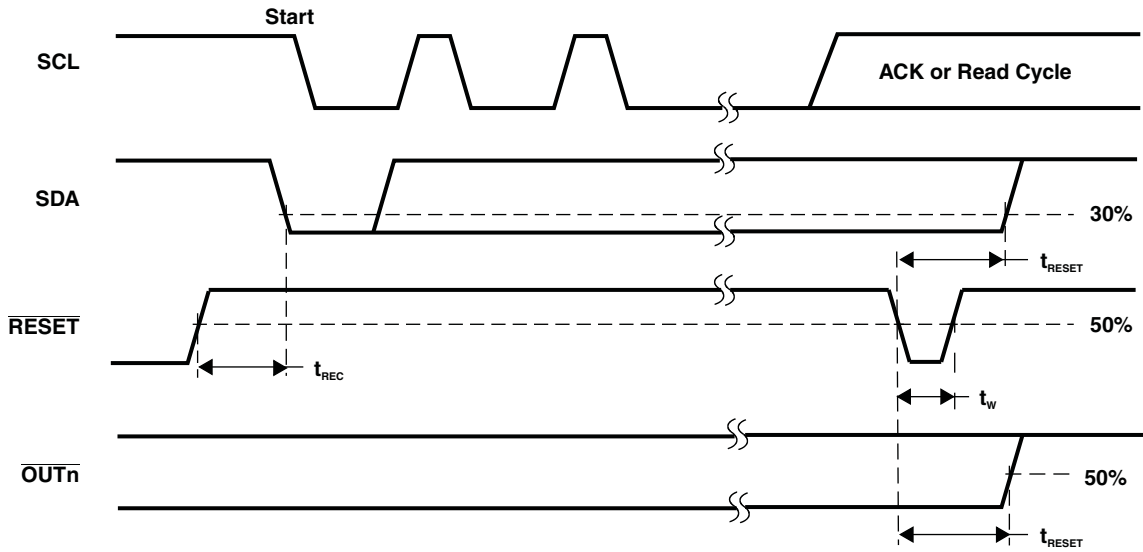
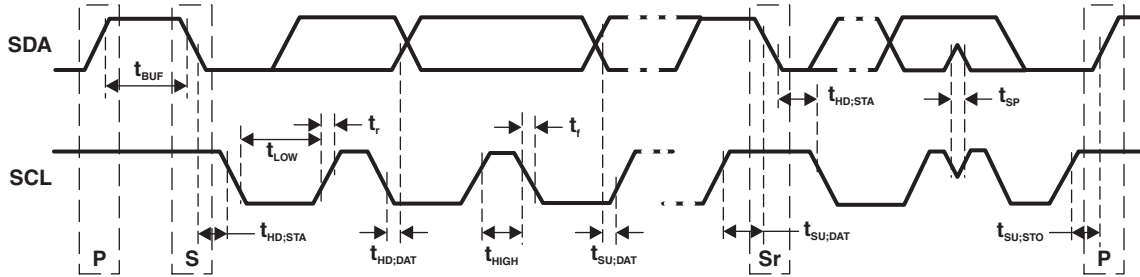# PARAMETER MEASUREMENT INFORMATION
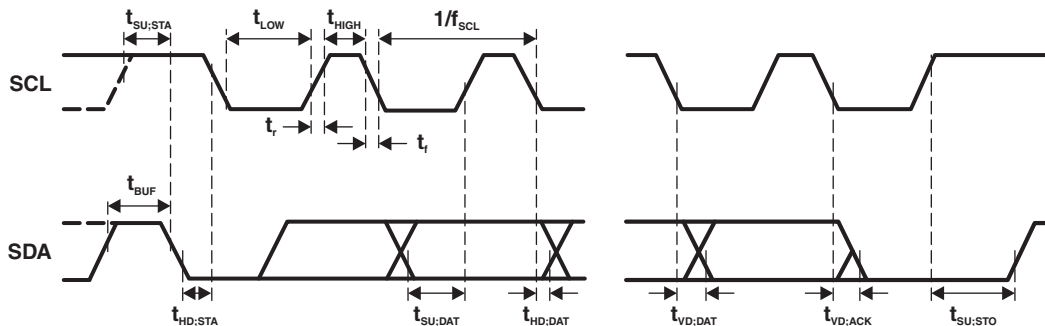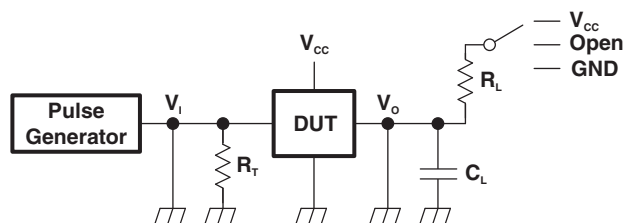


**Figure 1. Reset Timing**



**Figure 2. Definition of Timing**

| Protocol | Start Condition (S) | Bit 7 MSB (A7) | Bit 6 (A6) | | Bit 7 (D1) | Bit 8 (D0) | Acknowledge (A) | Stop Condition (P) |
|---|---|---|---|---|---|---|---|---|



NOTE: Rise and fall times refer to $V_{IL}$ and $V_{IH}$.

**Figure 3. I²C Bus Timing**

# PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: $R_L$ = Load resistance for SDA and SCL; should be >1 kΩ at 3-mA or lower current.

$C_L$ = Load capacitance; includes jig and probe capacitance.

$R_T$ = Termination resistance; should be equal to the output impedance ($Z_O$) of the pulse generator.

**Figure 4. Test Circuit for Switching Characteristics**

# APPLICATION INFORMATION

## Functional Description

### Device Address

Following a Start condition, the bus master must output the address of the slave it is accessing.

### Regular I²C Bus Slave Address

The I²C bus slave address of the TLC59108 is shown in Figure 5. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low. For buffer management purpose, a set of sector information data should be stored.
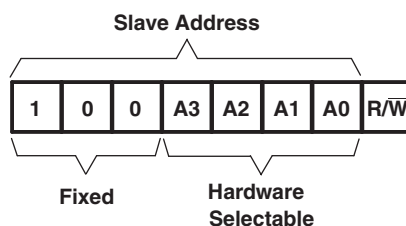
**Slave Address**

| 1 | 0 | 0 | A3 | A2 | A1 | A0 | R/$\overline{W}$ |
|---|---|---|----|----|----|----|---|

Fixed        Hardware
             Selectable

**Figure 5. Slave Address**

The last bit of the address byte defines the operation to be performed. When set to logic 1, a read operation is selected. When set to logic 0, a write operation is selected.

### LED All Call I²C Bus Address
- Default power-up value (ALLCALLADR register): 90h or 1001 000
- Programmable through I²C bus (volatile programming)
- At power-up, LED All Call I²C bus address is enabled. TLC59108 sends an ACK when 90h (R/$\overline{W}$ = 0) or 91h (R/$\overline{W}$ = 1) is sent by the master.

See LED All Call I2C Bus Address Register (ALLCALLADR) for more detail.

**NOTE:**

The default LED All Call I²C bus address (90h or 1001 000) must not be used as a regular I²C bus slave address since this address is enabled at power-up. All the TLC59108s on the I²C bus will acknowledge the address if sent by the I²C bus master

### LED Sub Call I²C Bus Address
- Three different I²C bus address can be used
- Default power-up values:
  – SUBADR1 register: 92h or 1001 001
  – SUBADR2 register: 94h or 1001 010
  – SUBADR3 register: 98h or 1001 100
- Programmable through I²C bus (volatile programming)
- At power-up, Sub Call I²C bus address is disabled. TLC59108 does not send an ACK when 92h (R/$\overline{W}$ = 0) or 93h (R/$\overline{W}$ = 1) or 94h (R/$\overline{W}$ = 0) or 95h (R/$\overline{W}$ = 1) or 98h (R/$\overline{W}$ = 0) or 99h (R/$\overline{W}$ = 1) is sent by the master.

See I2C Bus Subaddress Registers 1 to 3 (SUBADR1 to SUBADR3) for more detail.

**NOTE:**

The default LED Sub Call I²C bus address may be used as a regular I²C bus slave address as long as they are disabled.

## Software Reset I²C Bus Address

The address shown in Figure 6 is used when a reset of the TLC59108 needs to be performed by the master. The software reset address (SWRST Call) must be used with R/$\overline{W}$ = 0. If R/$\overline{W}$ = 1, the TLC59108 does not acknowledge the SWRST. See Software Reset for more detail.

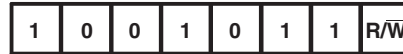| 1 | 0 | 0 | 1 | 0 | 1 | 1 | R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|

**Figure 6. Software Reset Address**

**NOTE:**

The Software Reset I²C bus address is reserved address and cannot be use as regular I²C bus slave address or as an LED All Call or LED Sub Call address.

## Control Register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the TLC59108, which will be stored in the Control register. The lowest 5 bits are used as a pointer to determine which register will be accessed (D[4:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).
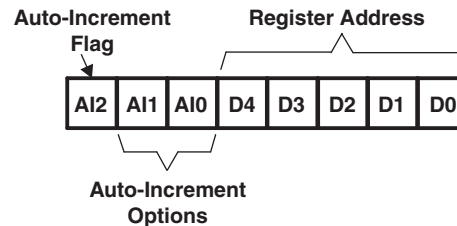
Auto-Increment
Flag      Register Address

| AI2 | AI1 | AI0 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|----|----|----|----|----|

Auto-Increment
Options

**Figure 7. Control Register**

When the Auto-Increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

**Table 1. Auto-Increment Options**

| AI2 | AI1 | AI0 | DESCRIPTION |
|-----|-----|-----|-------------|
| 0 | 0 | 0 | No auto-increment |
| 1 | 0 | 0 | Auto-increment for all registers. D[4:0] roll over to 0 0000 after the last register (1 1011) is accessed. |
| 1 | 0 | 1 | Auto-increment for individual brightness registers only. D[4:0] roll over to 0 0010 after the last register (1 0001) is accessed. |
| 1 | 1 | 0 | Auto-increment for global control registers only. D[4:0] roll over to 1 0010 after the last register (1 0011) is accessed. |
| 1 | 1 | 1 | Auto-increment for individual and global control registers only. D[4:0] roll over to 0 0010 after the last register (1 0011) is accessed. |

**NOTE:**

Other combinations not shown in Table 1. (AI[2:0] = 001, 010 and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I²C bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I²C bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I$^2$C bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individually and global changes must be performed during the same I$^2$C bus communication, for example, changing color and global brightness at the same time.

Only the 5 least significant bits D[4:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[4:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0 0000 and 1 1011 (as defined in ). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See for rollover values. For example, if the Control register = 1111 0100 (F4h), then the register addressing sequence will be (in hex):

14 → ... → 1B → 00 → ... → 13 → 02 → ... → 13 → 02 → ... as long as the master keeps sending or reading data.

## Driver Output

### Constant Current Output

In LED display applications, TLC59108 provides nearly no current variations from channel to channel and from device to device. While $I_{OUT}$ ≤ 100 mA, the maximum current skew between channels is less than ±3% and less than ±6% between devices.

### Adjusting Output Current

TLC59108 scales up the reference current ($I_{ref}$) set by the external resistor ($R_{ext}$) to sink the output current ($I_{out}$) at each output port. The following formulas can be used to calculate the target output current $I_{OUT,target}$ in the saturation region:

$V_{REXT}$ = 1.26 V × VG

$I_{ref}$ = $V_{REXT}/R_{ext}$, if another end of the external resistor $R_{ext}$ is connected to ground

$I_{OUT,target}$ = $I_{ref}$ × 15 × $3^{CM-1}$

Where $R_{ext}$ is the resistance of the external resistor connected to the $R_{EXT}$ terminal, and $V_{REXT}$ is the voltage of $R_{EXT}$, which is controlled by the programmable voltage gain (VG), which is defined by the Configuration Code. The Current Multiplier (CM) determines that the ratio $I_{OUT,target}/I_{ref}$ is 15 or 5. After power on, the default value of VG is 127/128 = 0.992, and the default value of CM is 1, so that the ratio $I_{OUT,target}/I_{ref}$ = 15. Based on the default VG and CM.

$V_{REXT}$ = 1.26 V × 127/128 = 1.25 V

$I_{OUT,target}$ = (1.25 V/$R_{ext}$) × 15

Therefore, the default current is approximately 52 mA at 360 Ω and 26 mA at 720 Ω. The default relationship after power on between $I_{OUT,target}$ and $R_{ext}$ is shown in Figure 8.
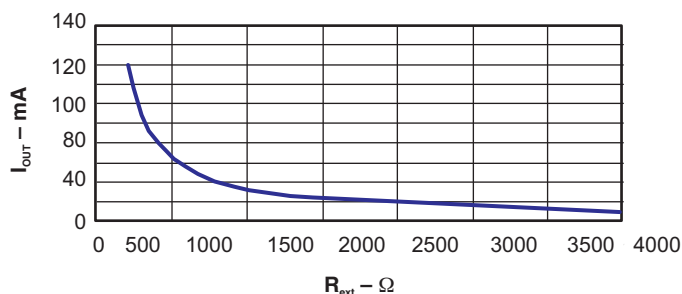


Figure 8. $I_{OUT,target}$ vs $R_{ext}$

## Register Descriptions

Table 2 describes the registers in the TLC59108.

**Table 2. Register Descriptions**

| REGISTER NUMBER (HEX) | NAME | ACCESS[1] | DESCRIPTION |
|---|---|---|---|
| 00 | MODE1 | R/W | Mode 1 |
| 01 | MODE2 | R/W | Mode 2 |
| 02 | PWM0 | R/W | Brightness control LED0 |
| 03 | PWM1 | R/W | Brightness control LED1 |
| 04 | PWM2 | R/W | Brightness control LED2 |
| 05 | PWM3 | R/W | Brightness control LED3 |
| 06 | PWM4 | R/W | Brightness control LED4 |
| 07 | PWM5 | R/W | Brightness control LED5 |
| 08 | PWM6 | R/W | Brightness control LED6 |
| 09 | PWM7 | R/W | Brightness control LED7 |
| 0A | GRPPWM | R/W | Group duty cycle control |
| 0B | GRPFREQ | R/W | Group frequency |
| 0C | LEDOUT0 | R/W | LED output state 0 |
| 0D | LEDOUT1 | R/W | LED output state 1 |
| 0E | SUBADR1 | R/W | $I^2C$ bus subaddress 1 |
| 0F | SUBADR2 | R/W | $I^2C$ bus subaddress 2 |
| 10 | SUBADR3 | R/W | $I^2C$ bus subaddress 3 |
| 11 | ALLCALLADR | R/W | LED All Call $I^2C$ bus address |
| 12 | IREF | R/W | IREF configuration |
| 13 | EFLAG | R | Error flag |

(1)  R = read, W = write

## Mode Register 1 (MODE1)

Table 3 describes Mode Register 1.

**Table 3. MODE1 – Mode Register 1 (Address 00h) Bit Description**

| BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 | AI2 | R | 0[2] | Register Auto-Increment disabled |
| | | | 1 | Register Auto-Increment enabled |
| 6 | AI1 | R | 0[2] | Auto-Increment bit 1 = 0 |
| | | | 1 | Auto-Increment bit 1 = 1 |
| 5 | AI0 | R | 0[2] | Auto-Increment bit 0 = 0 |
| | | | 1 | Auto-Increment bit 0 = 1 |
| 4 | SLEEP | R/W | 0 | Normal mode[3] |
| | | | 1[2] | Low power mode. Oscillator off[4]. |
| 3 | SUB1 | R/W | 0[2] | Device does not respond to $I^2C$ bus subaddress 1. |
| | | | 1 | Device responds to $I^2C$ bus subaddress 1. |
| 2 | SUB2 | R/W | 0[2] | Device does not respond to $I^2C$ bus subaddress 2. |
| | | | 1 | Device responds to $I^2C$ bus subaddress 2. |
| 1 | SUB3 | R/W | 0[2] | Device does not respond to $I^2C$ bus subaddress 3. |
| | | | 1 | Device responds to $I^2C$ bus subaddress 3. |
| 0 | ALLCALL | R/W | 0 | Device does not respond to LED All Call $I^2C$ bus address. |
| | | | 1[2] | Device responds to LED All Call $I^2C$ bus address. |

(1) R = read, W = write
(2) Default value
(3) Requires 500 μs maximum for the oscillator to be up and running once SLEEP bit has been set to logic 1. Timings on LED outputs are not guaranteed if PWMx, GRPPWM, or GRPFREQ registers are accessed within the 100 μs window.
(4) No blinking or dimming is possible when the oscillator is off.

## Mode Register 2 (MODE2)

Table 4 describes Mode Register 2.

**Table 4. MODE2 – Mode Register 2 (Address 01h) Bit Description**

| BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 | EFCLR | R/W | 0[2] | Enable error status flag |
| | | | 1 | Clear error status flag |
| 6 | | R | 0[2] | Reserved |
| 5 | DMBLNK | R/W | 0[2] | Group control = dimming |
| | | | 1 | Group control = blinking |
| 4 | | R | 0[2] | Reserved |
| 3 | OCH | R/W | 0[2] | Outputs change on Stop command[3] |
| | | | 1 | Outputs change on ACK |
| 2:0 | | R | 000[2] | Reserved |

(1) R = read, W = write
(2) Default value
(3) Change of the outputs at the Stop command allows synchronizing outputs of more than one TLC59108. Applicable to registers from 02h (PWM0) to 0Dh (LEDOUT) only.

**Brightness Control Registers 0 to 7 (PWM0 to PWM7)**

Table 6 describes Brightness Control Registers 0 to 7.

**Table 5. PWM0 to PWM7 – PWM Registers 0 to 7 (Address 02h to 09h) Bit Description**

| ADDRESS | REGISTER | BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---|---|---|---|---|---|---|
| 02h | PWM0 | 7:0 | IDC0[7:0] | R/W | 0000 0000[2] | PWM0 individual duty cycle |
| 03h | PWM1 | 7:0 | IDC1[7:0] | R/W | 0000 0000[2] | PWM1 individual duty cycle |
| 04h | PWM2 | 7:0 | IDC2[7:0] | R/W | 0000 0000[2] | PWM2 individual duty cycle |
| 05h | PWM3 | 7:0 | IDC3[7:0] | R/W | 0000 0000[2] | PWM3 individual duty cycle |
| 06h | PWM4 | 7:0 | IDC4[7:0] | R/W | 0000 0000[2] | PWM4 individual duty cycle |
| 07h | PWM5 | 7:0 | IDC5[7:0] | R/W | 0000 0000[2] | PWM5 individual duty cycle |
| 08h | PWM6 | 7:0 | IDC6[7:0] | R/W | 0000 0000[2] | PWM6 individual duty cycle |
| 09h | PWM7 | 7:0 | IDC7[7:0] | R/W | 0000 0000[2] | PWM7 individual duty cycle |

(1) R = read, W = write
(2) Default value

A 97-kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 and LEDOUT1 registers).

Duty cycle = IDCn[7:0] / 256

**Group Duty Cycle Control Register (GRPPWM)**

Table 6 describes the Group Duty Cycle Control Register.

**Table 6. GRPPWM – Group Brightness Control Register (Address 0Ah) Bit Description**

| ADDRESS | REGISTER | BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---|---|---|---|---|---|---|
| 0Ah | GRPPWM | 7:0 | GDC0[7:0] | R/W | 1111 1111[2] | GRPPWM register |

(1) R = read, W = write
(2) Default value

When the DMBLNK bit (MODE2 register) is programmed with logic 0, a 190-Hz fixed-frequency signal is superimposed with the 97-kHz individual brightness control signal. GRPPWM is then used as a global brightness control, allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a Don't care.

General brightness for the eight outputs is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

When DMBLNK bit is programmed with logic 1, the GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ defines the blinking period (from 24 Hz to 10.73 s) and GRPPWM defines the duty cycle (ON/OFF ratio in %).

Duty cycle = GDC0[7:0] / 256

## Group Frequency Register (GRPFREQ)

Table 7 describes the Group Frequency Register.

**Table 7. GRPFREQ – Group Frequency Register (Address 0Bh) Bit Description**

| ADDRESS | REGISTER | BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---------|----------|-----|--------|-----------|-------|-------------|
| 0Bh | GRPFREQ | 7:0 | GFRQ[7:0] | R/W | 0000 0000[2] | GRPFREQ register |

(1)  R = read, W = write
(2)  Default value

GRPFREQ is used to program the global blinking period when the DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a Don't care when DMBLNK = 0. Applicable to LED output programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

Global blinking period (seconds) = (GFRQ[7:0] + 1) / 24

## LED Driver Output State Registers (LEDOUT0, LEDOUT1)

Table 8 describes LED Driver Output State Registers 0 and 1.

**Table 8. LEDOUT0 and LEDOUT1 – LED Driver Output State Registers (Address 0Ch and 0Dh) Bit Description**

| ADDRESS | REGISTER | BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---------|----------|-----|--------|-----------|-------|-------------|
| 0Ch | LEDOUT0 | 7:6 | LDR3[1:0] | R/W | 00[2] | LED3 output state control |
|  |  | 5:4 | LDR2[1:0] | R/W | 00[2] | LED2 output state control |
|  |  | 3:2 | LDR1[1:0] | R/W | 00[2] | LED1 output state control |
|  |  | 1:0 | LDR0[1:0] | R/W | 00[2] | LED0 output state control |
| 0Dh | LEDOUT1 | 7:6 | LDR7[1:0] | R/W | 00[2] | LED7 output state control |
|  |  | 5:4 | LDR6[1:0] | R/W | 00[2] | LED6 output state control |
|  |  | 3:2 | LDR5[1:0] | R/W | 00[2] | LED5 output state control |
|  |  | 1:0 | LDR4[1:0] | R/W | 00[2] | LED4 output state control |

(1)  R = read, W = write
(2)  Default value

LDRx = 00: LED driver x is off (default power-up state).

LDRx = 01: LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10: LED driver x is individual brightness can be controlled through its PWMx register.

LDRx = 11: LED driver x is individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

## I²C Bus Subaddress Registers 1 to 3 (SUBADR1 to SUBADR3)

Table 9 describes I²C Bus Subaddress Registers 1 to 3.

**Table 9. SUBADR1 to SUBADR3 – I²C Bus Subaddress Registers 1 to 3 (Address 0Eh to 10h) Bit Description**

| ADDRESS | REGISTER | BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---|---|---|---|---|---|---|
| 0Eh | SUBADR1 | 7:5 | A1[7:5] | R | 100[2] | Reserved |
| | | 4:1 | A1[4:1] | R/W | 1001[2] | I²C bus subaddress 1 |
| | | 0 | A1[0] | R | 0[2] | Reserved |
| 0Fh | SUBADR2 | 7:5 | A2[7:1] | R | 100[2] | Reserved |
| | | 4:1 | A2[4:1] | R/W | 1010[2] | I²C bus subaddress 2 |
| | | 0 | A2[0] | R | 0[2] | Reserved |
| 10h | SUBADR3 | 7:5 | A3[7:1] | R | 100[2] | Reserved |
| | | 4:1 | A3[4:1] | R/W | 1100[2] | I²C bus subaddress 3 |
| | | 0 | A3[0] | R | 0[2] | Reserved |

(1)  R = read, W = write
(2)  Default value

Subaddresses are programmable through the I²C bus. Default power-up values are 92h, 94h, 98h. The TLC59108 does not acknowledge these addresses immediately after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to valid values, the SUBx bits (MODE1 register) must be set to 1 to allows the device to acknowledge these addresses.

Only the 7 MSBs representing the I²C bus subaddress are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to 1, the corresponding I²C bus subaddress can be used during either an I²C bus read or write sequence.

## LED All Call I²C Bus Address Register (ALLCALLADR)

Table 10 describes the LED All Call I²C Bus Address Register.

**Table 10. ALLCALLADR – LED All Call I²C Bus Address Register (Address 11h) Bit Description**

| ADDRESS | REGISTER | BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---|---|---|---|---|---|---|
| 11h | ALLCALLADR | 7:5 | AC[7:5] | R | 100[2] | Reserved |
| | | 4:1 | AC[4:1] | R/W | 1000[2] | All Call I²C bus address register |
| | | 0 | AC[0] | R | 0[2] | Reserved |

(1)  R = read, W = write
(2)  Default value

The LED All Call I²C bus address allows all the TLC59108 devices in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1, which is the power-up default state). This address is programmable through the I²C bus and can be used during either an I²C bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

## Output Gain Control Register (IREF)

Table 11 describes the Output Gain Control Register.

**Table 11. IREF – Output Gain Control Register (Address 12h) Bit Description**

| ADDRESS | REGISTER | BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---------|----------|-----|--------|-----------|-------|-------------|
| 11h | ALLCALLADR | 7 | CM | R/W | 1[2] | High/low current multiplier |
| | | 6 | HC | R/W | 1[2] | Subcurrent |
| | | 5:0 | CC[5:0] | R/W | 11 1111[2] | Current multiplier |

(1)  R = read, W = write
(2)  Default value

$I_{REF}$ determines the voltage gain (VG), which affects the voltage at the $R_{EXT}$ terminal and indirectly the reference current ($I_{REF}$) flowing through the external resistor at terminal $R_{EXT}$. Bit 0 is the Current Multiplier (CM) bit, which determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM sets a Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown below:

  $VG = (1 + HC) \times (1 + D/64) / 4$

  $D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$

  Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:

  Low voltage sub-band (HC = 0): VG = 1/4 to 127/256, linearly divided into 64 steps

  High voltage sub-band (HC = 1): VG = 1/2 to 127/128, linearly divided into 64 steps

- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.

  High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref}$ = 15, suitable for output current range $I_{OUT}$ = 10 mA to 120 mA.

  Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref}$ = 5, suitable for output current range $I_{OUT}$ = 5 mA to 40 mA

- CG: The total Current Gain is defined as the following.

  $V_{REXT} = 1.26 V \times VG$

  $I_{ref} = V_{REXT}/R_{ext}$, if the external resistor, $R_{ext}$, is connected to ground.

  $I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26 V/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26 V/R_{ext} \times 15) \times CG$

  $CG = VG \times 3^{CM-1}$

  Therefore, CG = (1/12) to (127/128), and it is divided into 256 steps. If CG = 127/128 = 0.992, the $I_{OUT,target}$-$R_{ext}$.

## Examples

- $I_{REF}$ Code {CM, HC, CC[0:5]} = {1,1,111111}
  VG = 127/128 = 0.992 and CG = VG $\times 3^0$ = VG = 0.992
- $I_{REF}$ Code {CM, HC, CC[0:5]} = {1,1,000000}
  VG = (1 + 1) $\times$ (1 + 0/64)/4 = 1/2 = 0.5, and CG = 0.5
- $I_{REF}$ Code {CM, HC, CC[0:5]} = {0,0,000000}
  VG = (1 + 0) $\times$ (1 + 0/64)/4 = 1/4, and CG = (1/4) $\times 3^{-1}$ = 1/12

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain is shown in Figure 9.

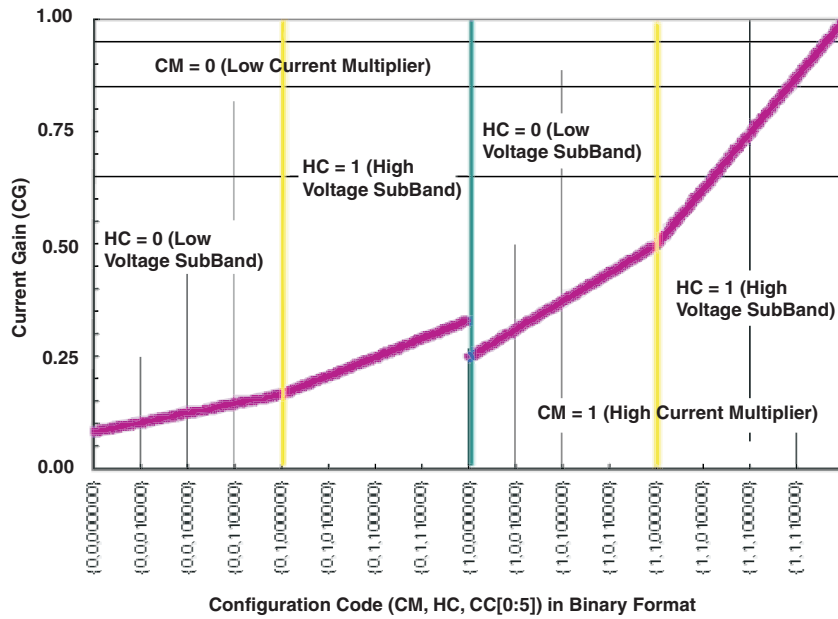**Figure 9. Current Gain vs Configuration Code**

## Error Flags Registers (EFLAG)

Table 12 describes the Error Flags Register.

**Table 12. EFLAG – Error Flags Register (Address 13h) Bit Description**

| ADDRESS | REGISTER | BIT | SYMBOL | ACCESS[1] | VALUE | DESCRIPTION |
|---------|----------|-----|--------|-----------|-------|-------------|
| 13h | EFLAG | 7:0 | EFLAG[7:0] | R | 1111 1111[2] | Error flag status by channel |

(1)  R = read, W = write
(2)  Default value

## Open-Circuit Detection

The TLC59108 LED open-circuit detection compares the effective current level Iout with the open load detection threshold current $I_{OUT, Th}$. If $I_{OUT}$ is below the threshold $I_{OUT, Th}$ the TLC59108 detects an open load condition. This error status can be read out as an error flag through the EFLAG register.

For open-circuit error detection, a channel must be on.

**Table 13. Open-Circuit Detection**

| STATE OF OUTPUT PORT | CONDITION OF OUTPUT CURRENT | ERROR STATUS CODE | MEANING |
|---|---|---|---|
| Off | $I_{OUT}$ = 0 mA | 0 | Detection not possible |
| On | $I_{OUT} < I_{OUT,Th}$[(1)] | 0 | Open circuit |
|  | $I_{OUT} \geq I_{OUT,Th}$[(1)] | Channel n error status bit 1 | Normal |

(1)  $I_{OUT,Th}$ = 0.5 × $I_{OUT,target}$ (typical)

## Overtemperature Detection and Shutdown

The TLC59108 LED is equipped with a global overtemperature sensor and eight individual channel-selective overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shutdown, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in the EFLAG register.

- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the EFLAG register.

For channel-specific overtemperature error detection, a channel must be on.

The error flags of open-circuit and overtemperature are ORed to set the EFLAG register.

The error status code due to overtemperature is reset when the host writes 1 to bit 7 of the MODE2 register. The host must write 0 to bit 7 of the MODE2 register to enable the overtemperature error flag.

**Table 14. Overtemperature Detection[(1)]**

| STATE OF OUTPUT PORT | CONDITION | ERROR STATUS CODE | MEANING |
|---|---|---|---|
| On On → all channels Off | $T_j < T_{j,trip}$ global | 1 | Normal |
|  | $T_j > T_{j,trip}$ global | All error status bits = 0 | Global overtemperature |
| On On → Off | $T_j < T_{j,trip}$ channel n | 1 | Normal |
|  | $T_j > T_{j,trip}$ channel n | Channel n error status bit = 0 | Channel n overtemperature |

(1)  The global shutdown threshold temperature is approximately 170°C.

## Power-On Reset

When power is applied to $V_{CC}$, an internal power-on reset holds the TLC59108 in a reset condition until $V_{CC}$ reaches $V_{POR}$. At this point, the reset condition is released and the TLC59108 registers, and I2C bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter, $V_{CC}$ must be lowered below 0.2 V to reset the device.

## External Reset

A reset can be accomplished by holding the RESET pin low for a minimum of $t_W$. The TLC59108 registers and I2C state machine are held in their default states until the RESET input is again high.

This input requires a pullup resistor to $V_{CC}$ if no active connection is used.

## Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I$^2$C bus to be reset to the power-up state value through a specific I$^2$C bus command. To be performed correctly, the I$^2$C bus must be functional and there must be no device hanging the bus.

The SWRST Call function is defined as the following:

1. A Start command is sent by the I$^2$C bus master.
2. The reserved SWRST I$^2$C bus address 1101 011 with the R/$\overline{W}$ bit set to 0 (write) is sent by the I$^2$C bus master.
3. The TLC59108 device(s) acknowledge(s) after seeing the SWRST Call address 1101 0110 (96h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I$^2$C bus master.
4. Once the SWRST Call address has been sent and acknowledged, the master sends two bytes with two specific values (SWRST data byte 1 and byte 2):
    a. Byte1 = A5h: the TLC59108 acknowledges this value only. If byte 1 is not equal to A5h, the TLC59108 does not acknowledge it.
    b. Byte 2 = 5Ah: the TLC59108 acknowledges this value only. If byte 2 is not equal to 5Ah, the TLC59108 does not acknowledge it.

    If more than two bytes of data are sent, the TLC59108 does not acknowledge any more.
5. Once the correct two bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a Stop command to end the SWRST Call. The TLC59108 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time ($t_{BUF}$).

The I$^2$C bus master may interpret a non-acknowledge from the TLC59108 (at any time) as a SWRST Call Abort. The TLC59108 does not initiate a reset of its registers. This happens only when the format of the Start Call sequence is not correct.

## Individual Brightness Control With Group Dimming/Blinking

A 97-kHz fixed-frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control the individual brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the four LED outputs):

- A lower 190-Hz fixed-frequency signal with programmable duty cycle (8 bits, 256 steps) provides a global brightness control.
- A programmable frequency signal from 24 Hz to 1/10.73 s (8 bits, 256 steps) provides a global blinking control.

**Figure 10. Brightness and Group Dimming Signals**
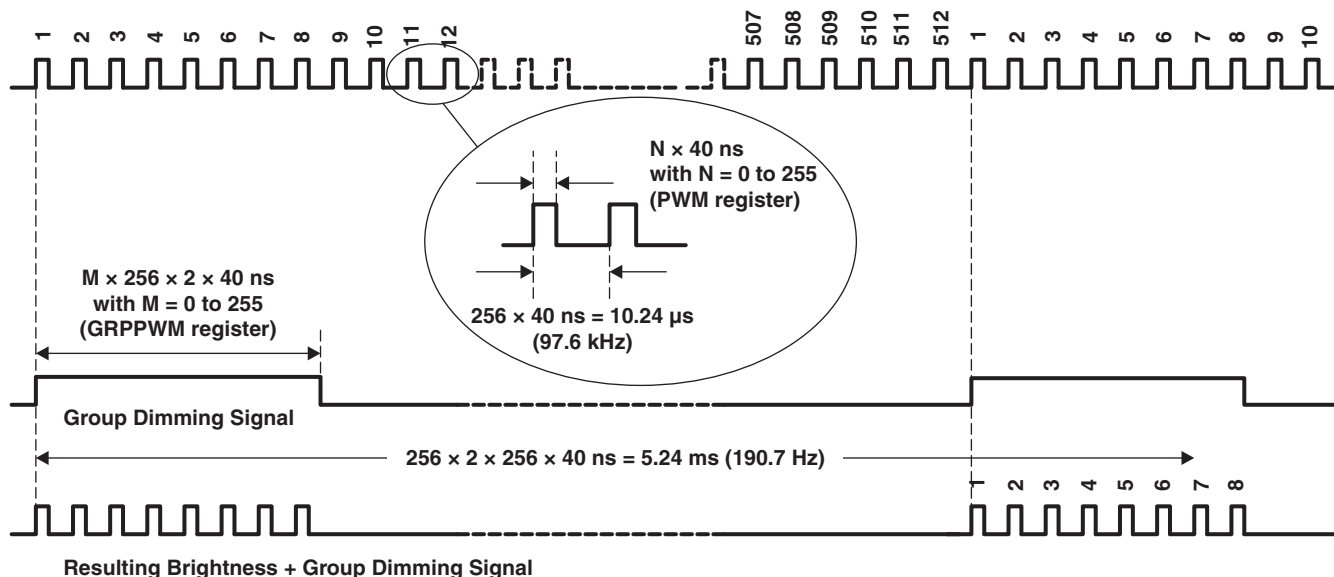
NOTE: Minimum pulse width for LEDn brightness control is 40 ns.

Minimum pulse width for group dimming is 20.48 µs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal has two pulses of the LED Brightness Control signal (pulse width = n × 40 ns, with n defined in the PWMx register). This resulting Brightness + Group Dimming signal shows a resulting control signal with n = 4 (8 pulses).

## Characteristics of the I$^2$C Bus

The I$^2$C bus is for two-way two-line communication between different devices or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 11).
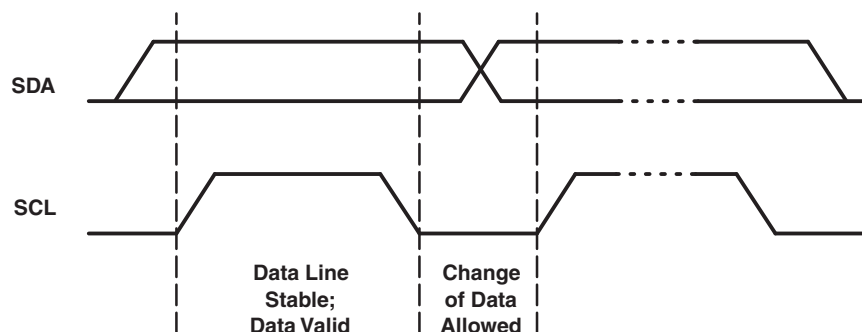


**Figure 11. Bit Transfer**

**Start and Stop Conditions**

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the Start condition (S). A low-to-high transition of the data line while the clock is high is defined as the Stop condition (P) (see Figure 12).
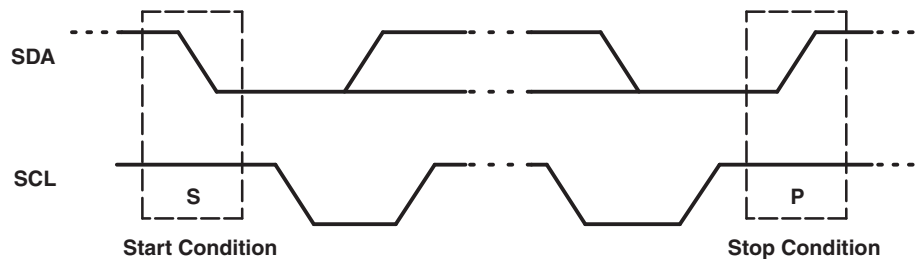


**Figure 12. Start and Stop Conditions**

## System Configuration

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 13).
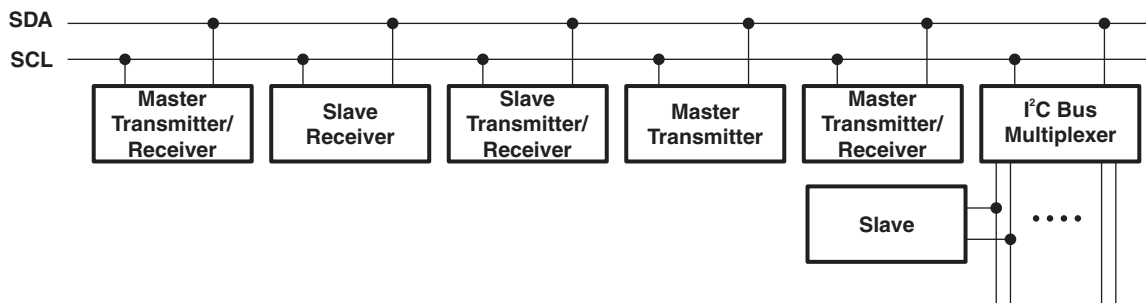


**Figure 13. System Configuration**

## Acknowledge

The number of data bytes transferred between the Start and the Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line high to enable the master to generate a Stop condition.
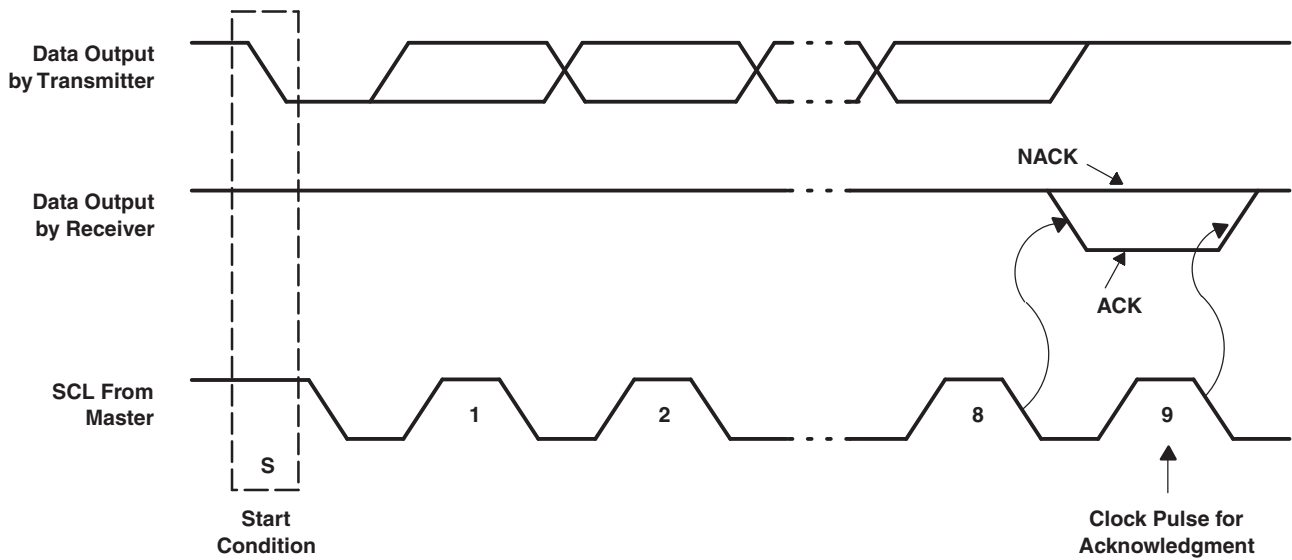
**Figure 14. Acknowledge/Not Acknowledge on I²C Bus**
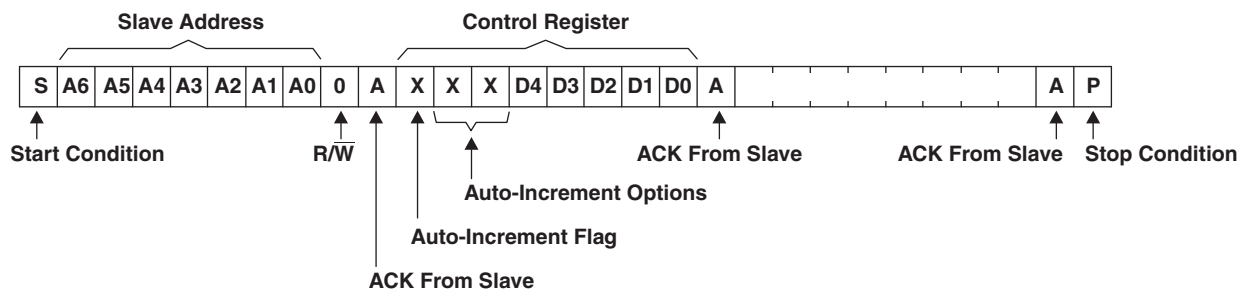


**Figure 15. Write to a Specific Register**
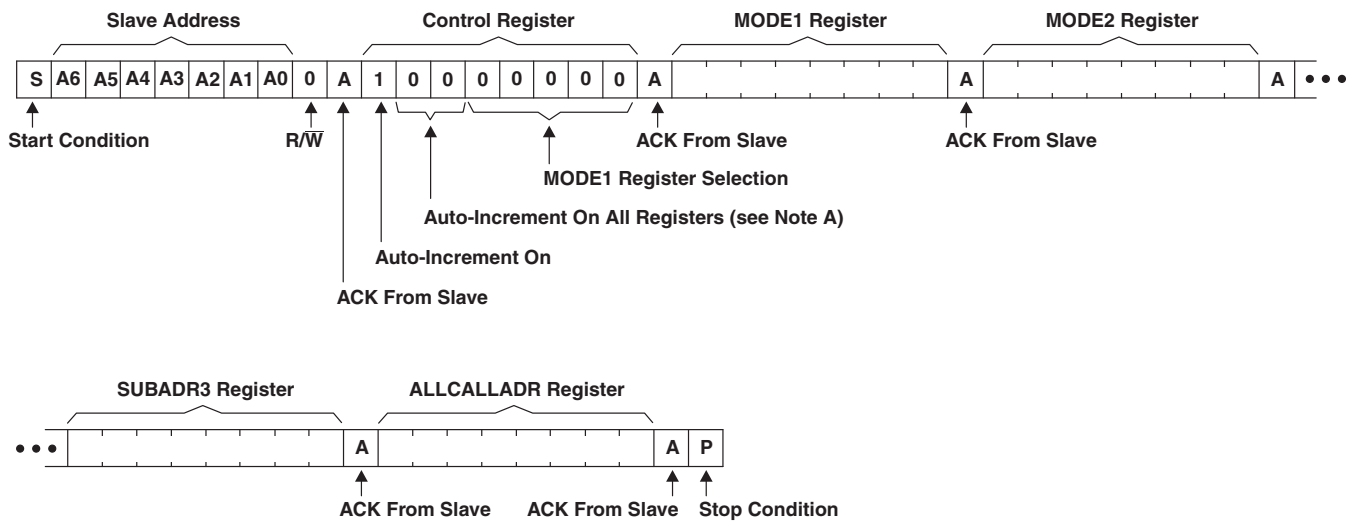


A.   See Table 2 for register definitions.

**Figure 16. Write to All Registers Using Auto-Increment**
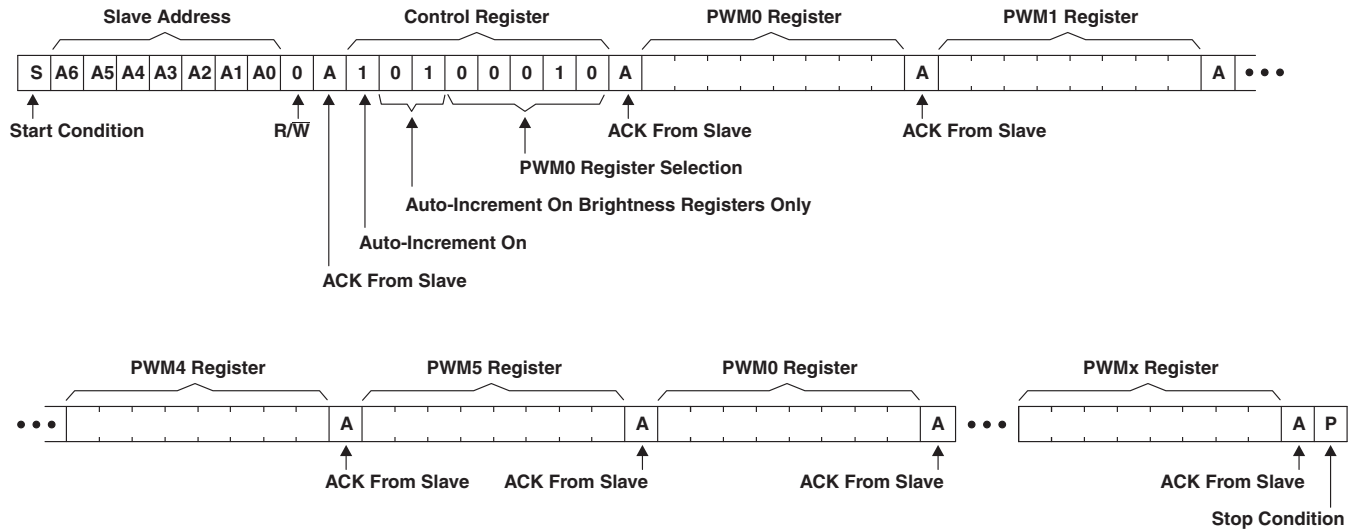
# TLC59108

**Figure 17. Multiple Writes to Individual Brightness Registers Using Auto-Increment**
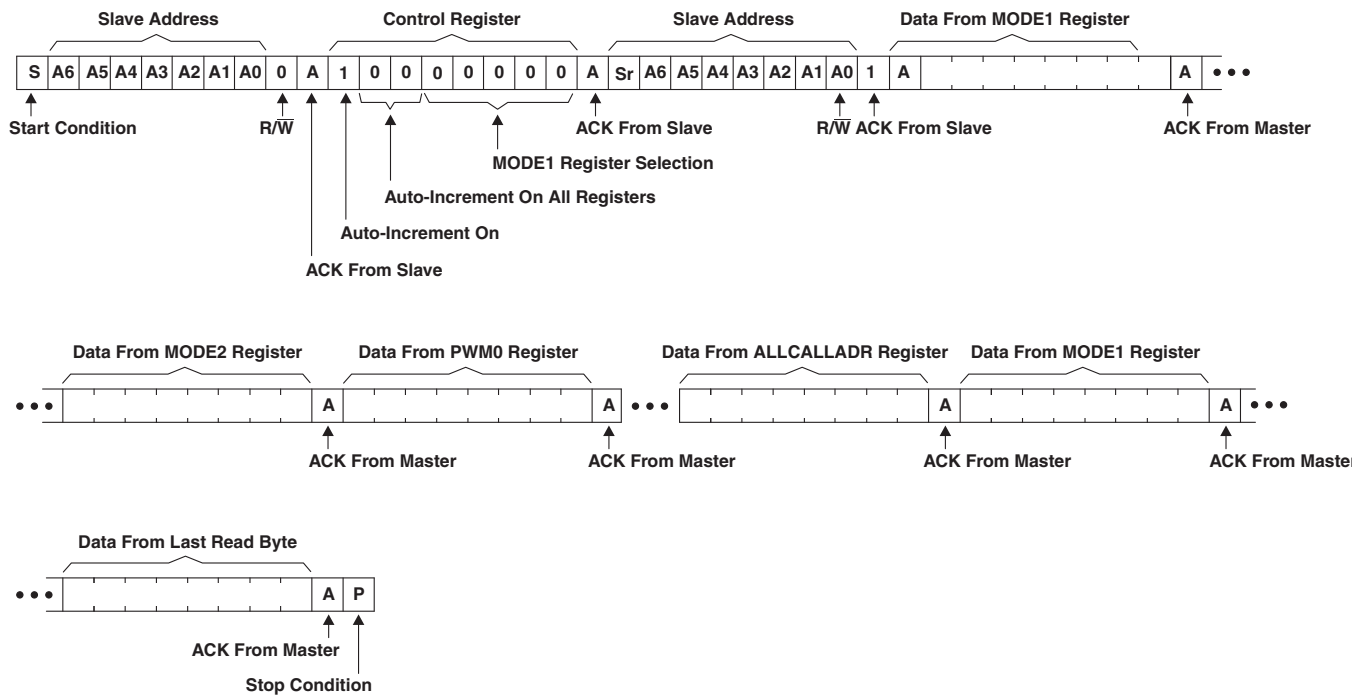


**Figure 18. Read All Registers Auto-Increment**
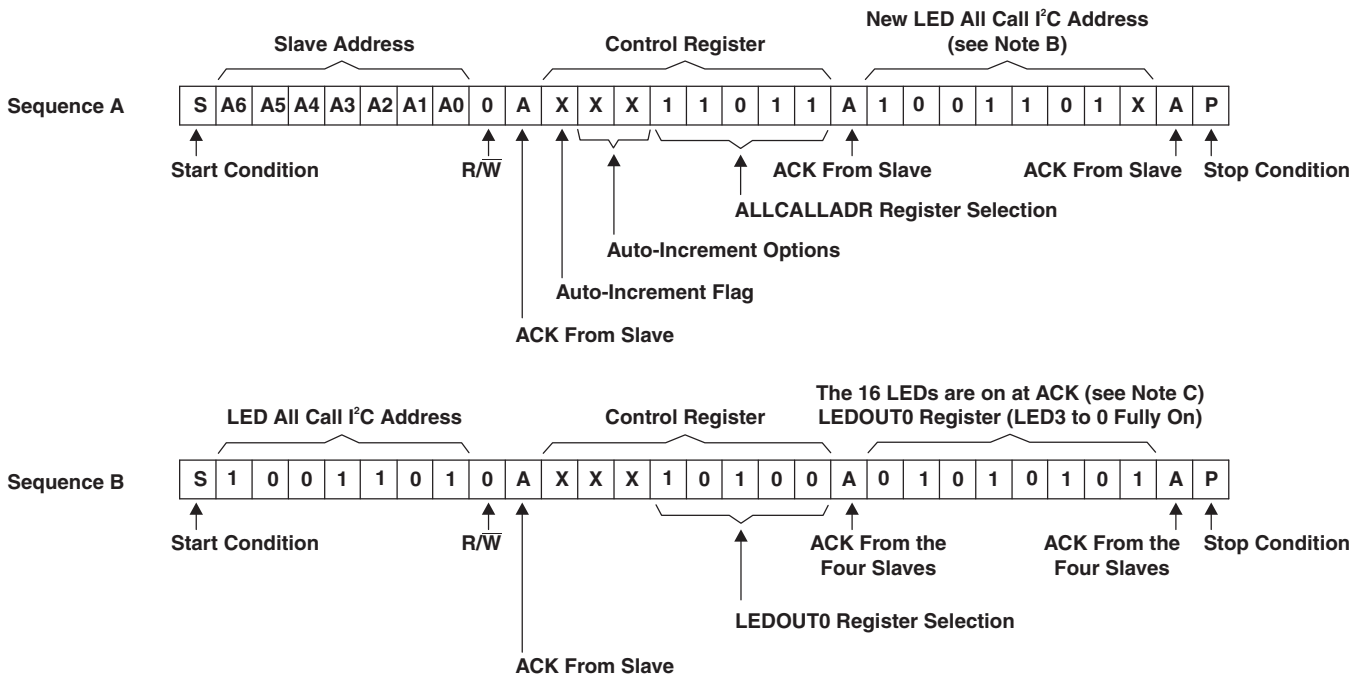
A. In this example, several TLC59108 devices are used, and the same Sequence A is sent to each of them.
B. The ALLCALL bit in the MODE1 register is equal to 1 for this example.
C. The OCH bit in the MODE2 register is equal to 1 for this example.

**Figure 19. LED All Call I²C Bus Address Programming and LED All Call Sequence**

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| TLC59108IPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC59108IRGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |
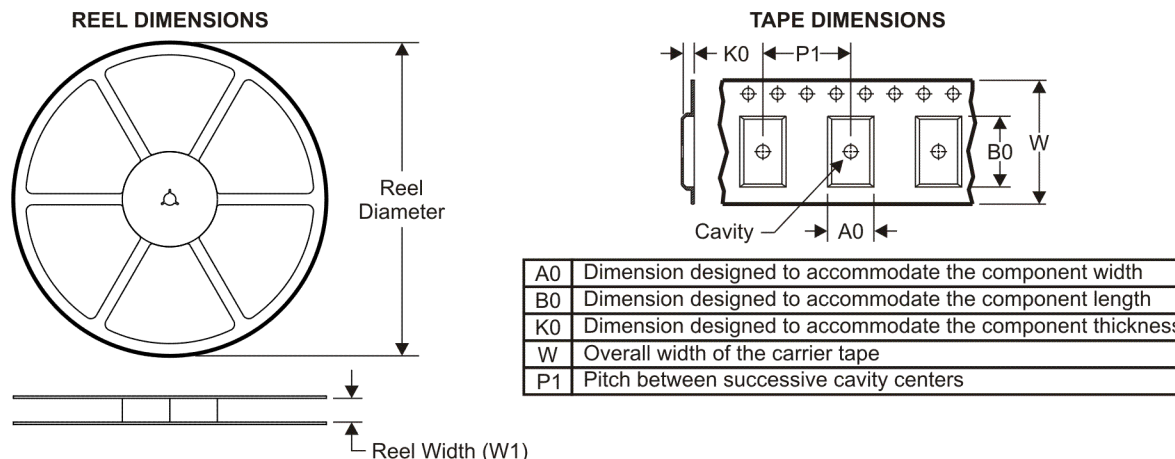
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
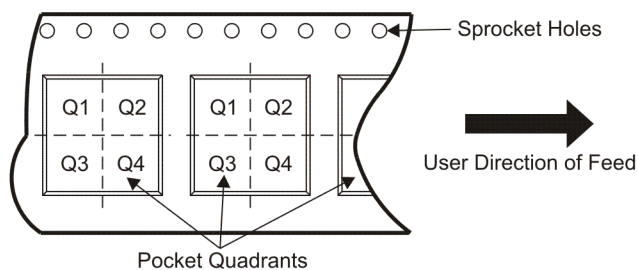
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLC59108IPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TLC59108IRGYR | VQFN | RGY | 20 | 3000 | 180.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLC59108IPWR | TSSOP | PW | 20 | 2000 | 346.0 | 346.0 | 33.0 |
| TLC59108IRGYR | VQFN | RGY | 20 | 3000 | 190.5 | 212.7 | 31.8 |

"TLC59108"

RGY (R−PVQFN−N20)                    PLASTIC QUAD FLATPACK NO−LEAD

4,65 / 4,35    A

B

19          12

20                    11

3,65 / 3,35

1                    10

Pin 1 Index Area
Top and Bottom

2          9

E

1,00 / 0,80

0,20 Nominal
Lead Frame

Seating Plane

0,08  C

0,05 / 0,00
Seating Height

C

3,50

0,50

20X  0,50 / 0,30

2          9

1                    10

1,50

11

20

20X  0,30 / 0,18

Exposed Thermal Pad

D

19          12

+0,10

⊕ | 0,10 Ⓜ | C | A | B
0,05 Ⓜ | C

Bottom View

4203539−4/H  06/2009

NOTES:   A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
         C.  QFN (Quad Flatpack No−Lead) package configuration.
         D.  The package thermal pad must be soldered to the board for thermal and mechanical performance.
             See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E.  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
             The Pin 1 identifiers are either a molded, marked, or metal feature.
         F.  Package complies to JEDEC MO−241 variation BC.

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THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

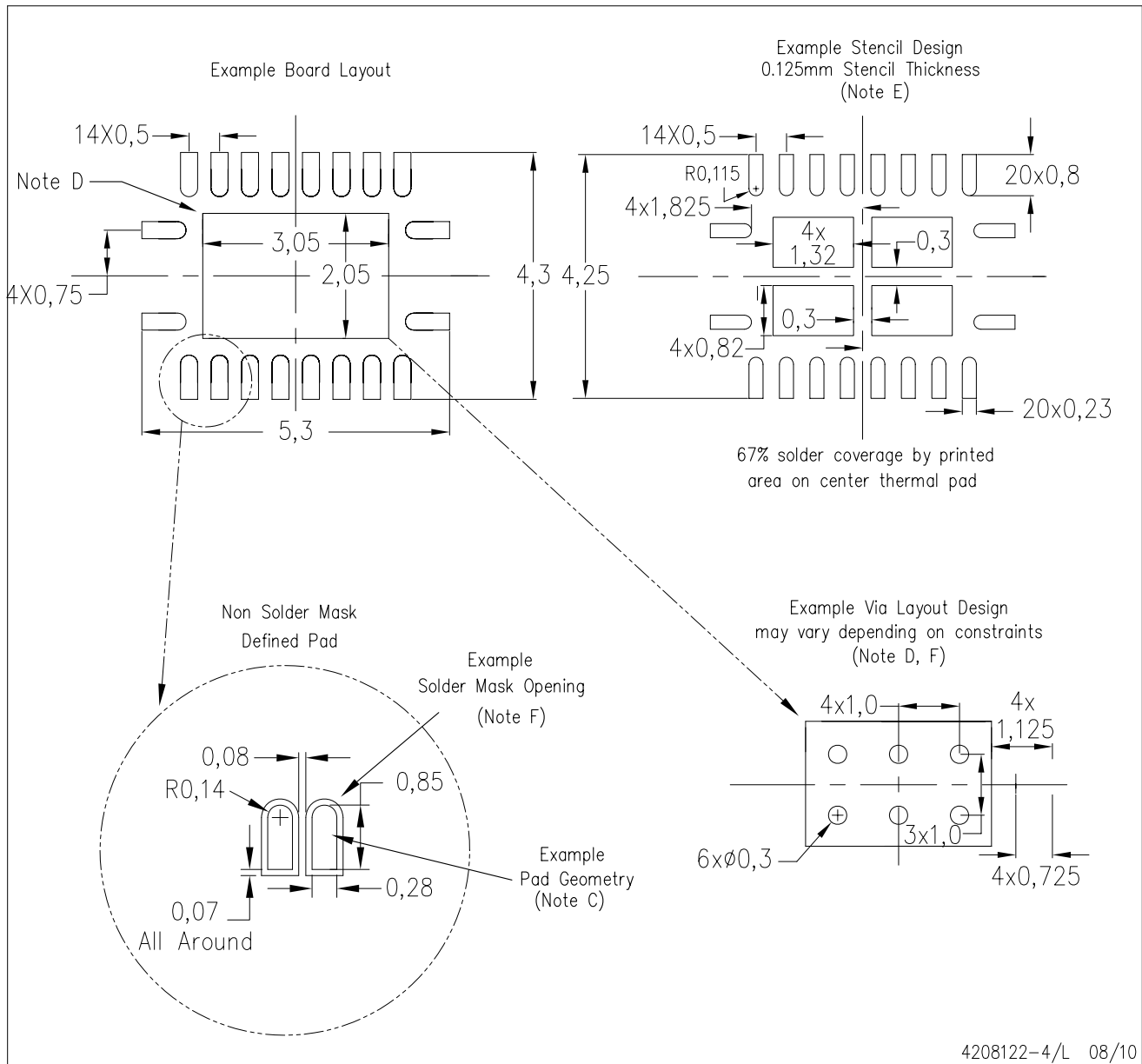The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad

2,05±0,10

3,05±0,10
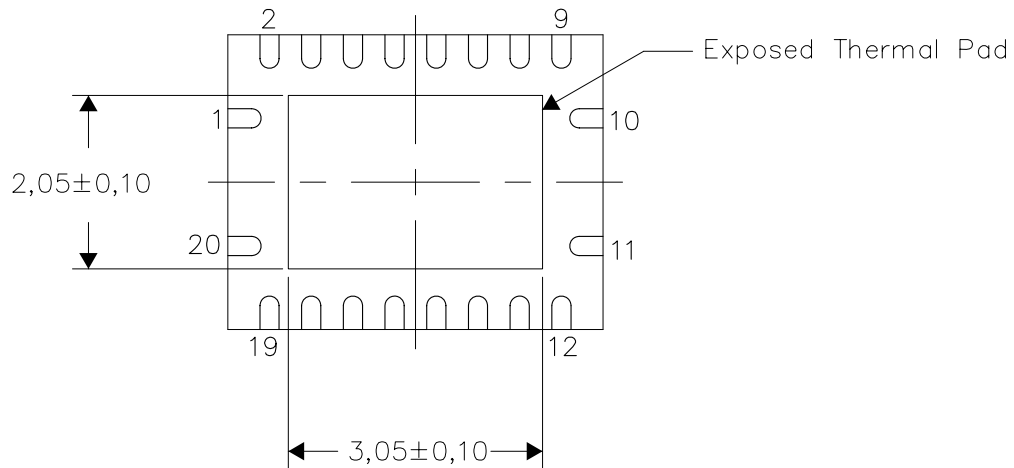
Bottom View

NOTE:   All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206353−4/L  08/10

RGY (R−PVQFN−N20)        PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

14X0,5

Note D

3,05

2,05

4,3 4,25

4X0,75

5,3

14X0,5

R0,115

4x1,825

20x0,8

4x
1,32

0,3

0,3

4x0,82

20x0,23

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07

0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

4x1,0

4x
1,125

6xØ0,3

3x1,0
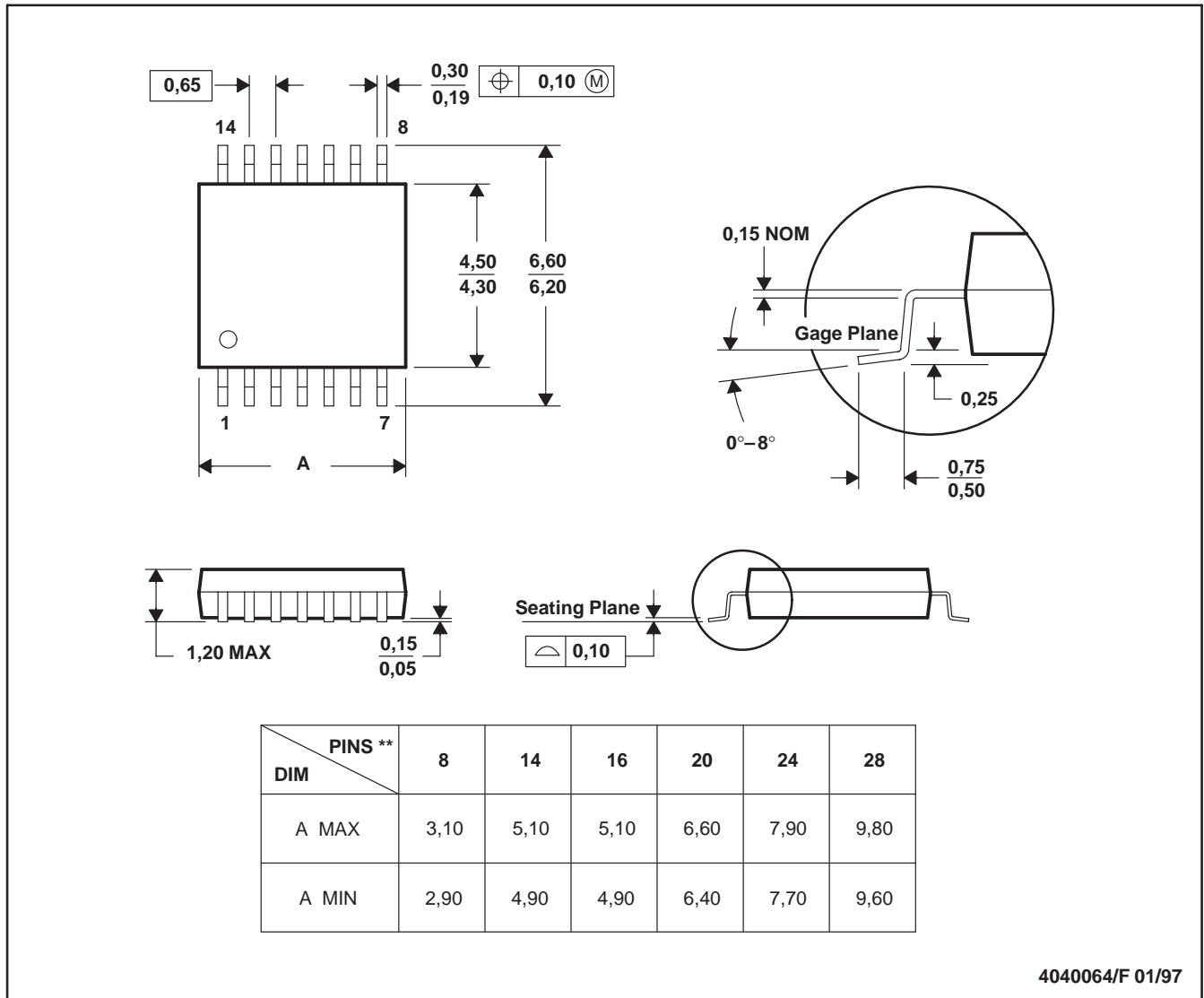
4x0,725

4208122−4/L   08/10

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat−Pack
              QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.
              These documents are available at www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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**PW (R-PDSO-G\*\*)**                                      **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**



| PINS \*\* DIM | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153

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