DYMEC

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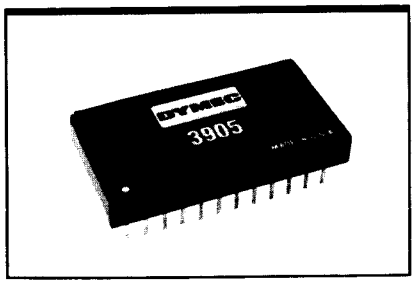
SILICON TRANSISTOR CORP.

MODEL

3905

5MHz Voltage-to-Frequency Converter



Description

The **3905** is a high performance, precision 5 MHz full scale Voltage-to-Frequency Converter, intended for those applications which require maximum performance at the most economical cost. The **3905** features overall performance and stability virtually identical to similar units costing 40% more.

The unit accepts a $-100\ \mu V$ to $-10V$ Full Scale, single-ended, analog input signal with a 5% overrange capability, and a dynamic range of greater than 5,000,000 to 1 (>134 dB). The input signal is converted to an output signal proportional to the full scale frequency, within 0.02% linearity utilizing the long-proven charge balance technique. Buffered complementary TTL-compatible frequency outputs are provided that will drive up to 50 pF capacitive loads.

Stability of the **3905** V/F over temperature is excellent for a V/F converter in its price range, with a $10\ \mu V/^{o}C$ typical, $30\ \mu V/^{o}C$ maximum offset and 60 ppm/°C typical, 100 ppm/°C maximum gain tempco. Warm-up time to fully specified accuracy is less than two (2) minutes.

In applications where overall system throughput must be maintained at a specific rate, or where fixed offset or different full scale voltages would be convenient, **custom frequencies** and/or **custom trimming** can be easily accommodated. By increasing the full scale output frequency by 10-20%, for example, additional time would be available for the system microprocessor to access the results of each conversion. Please contact the factory to discuss your specific system timing requirements.

The **3905** is packaged in a 1.31" X 0.69" X 0.22" 24-pin DIL plastic package. Pin spacing is 0.6" (double DIP). Power dissipation is less than 0.8W maximum, and operation is over the 0°C to +70°C temperature range.

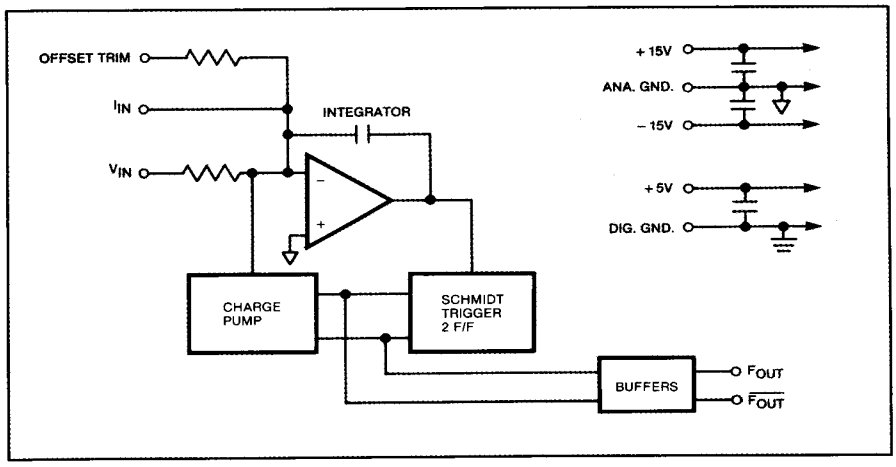


Figure 1. 3905 Block Diagram.

Features

- ☐ **Outstanding Price/ Performance Ratio**
- ☐ **Guaranteed minimum/ maximum specifications**
- ☐ **Wide Dynamic Range**
  >5,000,000:1
  >134 dB
- ☐ **Excellent Linearity**
  0.02% FS ±0.02% of input
- ☐ **Excellent Stability**
  10 μV/°C offset
  60 ppm/°C gain
- ☐ **Complementary Frequency Outputs**
  TTL/CMOS Compatible
- ☐ **Small Size**
  24-pin Double-DIP
- ☐ **Low Power**
  <0.8W

Applications

- ☐ **Analytical Instrumentation**
- ☐ **Medical Instrumentation**
- ☐ **Telemetry**
- ☐ **Data Recording**
- ☐ **Weighing Systems**

Specifications

All Specifications Guaranteed at 25°C Unless Otherwise Noted

Analog Input

Input Range
– 100 μV to – 10V

Overrange
5% minimum

Configuration
Single-ended

Impedance
6 KΩ

Offset Voltage
± 7 mV typical, ± 10 mV maximum; Adjustable to zero

Overvoltage Protection
± Vs without damage

Transfer Characteristics

Full Scale Frequency Output (Fout)
5 MHz ± 5%

Transfer Characteristic
5 MHz (Ein/10V)

Gain Error
± 1%, trimmable to zero

Non-Linearity
± 0.02% FS, ± 0.02% of input, maximum

Full Scale Step Response
2 cycles of new frequency, plus 10 μS

Overload Recovery
10 cycles of new frequency

Stability

Gain — Tempco
60 ppm FS/°C typical,
100 ppm FS/°C maximum

Gain — PS Sensitivity
200 ppm/1% change in supply voltage

Offset — Tempco
10 μV/°C typical,
30 μV/°C maximum

Offset — PS Sensitivity
10 μV/1% change in supply voltage

Warmup Time
≤ 2 minutes to specified accuracy

Output

Pulse Polarity
Positive and negative

Pulse Width
100 ± 20 ns

Logic Levels (Vcc = + 5V)
Logic "1" (High)
+ 4.0V ± 0.5V

Logic "0" (Low)
< 0.4V @ 3 mA sink

Load
≤ 50 pF for rated performance

Power Requirements

(+ Vs) + 15V, ± 3%
30 mA maximum

(– Vs) – 15V, ± 3%
10 mA maximum

(Vcc) + 5V, ± 5%
40 mA maximum

Power Dissipation
0.8W maximum

Environmental and Mechanical

Operating Temperature
0°C to + 70°C

Storage Temperature
– 65°C to + 150°C

Humidity
0-85%, non-condensing up to 40°C

Dimensions
1.31" X 0.69" X 0.22"
(33.2 X 17.5 X 5.5 mm)

Using the 3905

General Considerations

Figure 2 depicts a typical circuit configuration for the **3905**. The layout should be clean, with output pulses routed as far away from the input analog signals as possible. For maximum performance, bypass capacitors, as shown in Figure 2, should be mounted right at the appropriate pins of the **3905.**

Offset and Gain Trimming

The OFFSET adjustment potentiometer should be a 20 kΩ, 10-turn unit. To insure that the temperature coefficient of the potentiometer is not significant relative to the overall offset drift specification, a potentiometer with a temperature coefficient of 100 ppm or better is recommended. With this pot in the circuit, initial offsets of up to ± 10 mV may be trimmed to zero.

The GAIN adjustment potentiometer should be a 200Ω, 10-turn unit with a recommended temperature coefficient of 100 ppm or better. With this pot in the circuit, initial gain errors of up to ± 2% may be trimmed to zero.

Grounding

The Analog and Digital grounds are internally separate in the **3905**. The use of ground plane is not necessary for proper operation of the **3905**; however, a ground plane is recommended with any analog signal conditioning circuitry that may be used in front of the V/F, especially if this circuitry involves high gains. Any amplifiers used in front of the **3905** should be decoupled to eliminate potential problems with the high frequency output of the V/F.

Offset and Gain Calibration

Offset Calibration

Offset calibration should be performed prior to gain calibration. With a − 10 mV analog input signal at pin 11 of the **3905**, adjust the OFFSET potentiometer until a frequency of 5.000 KHz is observed on output pins 21, 23 or 24.

Gain Calibration

With a full scale analog input voltage of − 10.00V on pin 11, adjust the GAIN potentiometer until a full scale frequency of 5.000 MHz is observed on output pins 21, 23 or 24.

N/C Pins

Pins marked as N/C (no connection) have no electrical connection to the internal circuitry of the **3905.**

Output Pins

Pins 23 and 24 are tied together internally. Either or both may be used as the source of the frequency output of the **3905** as long as the load specifications are not exceeded. Pin 21 provides an inverted signal relative to pins 23 and 24 with the same loading limits.

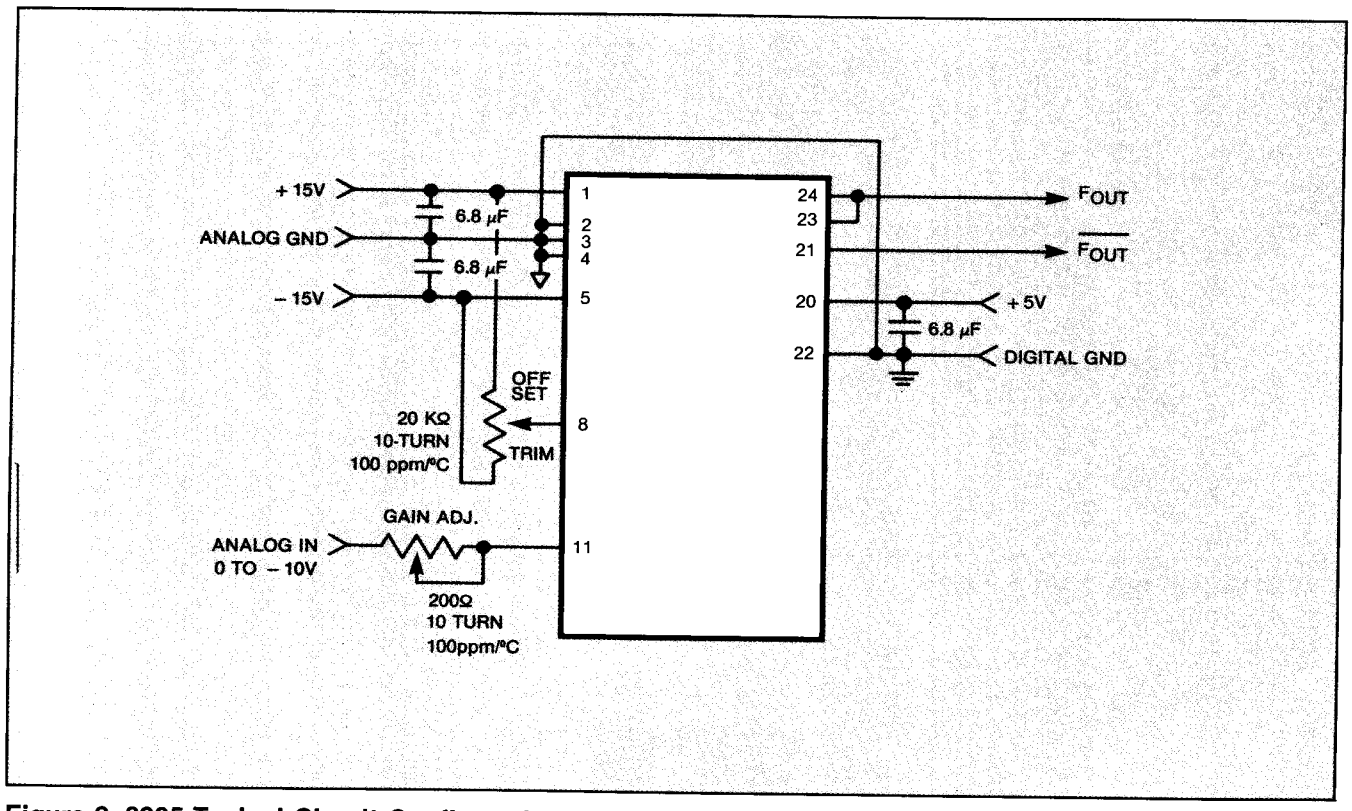


Figure 2. 3905 Typical Circuit Configuration.

Mechanical Dimensions & Pinout

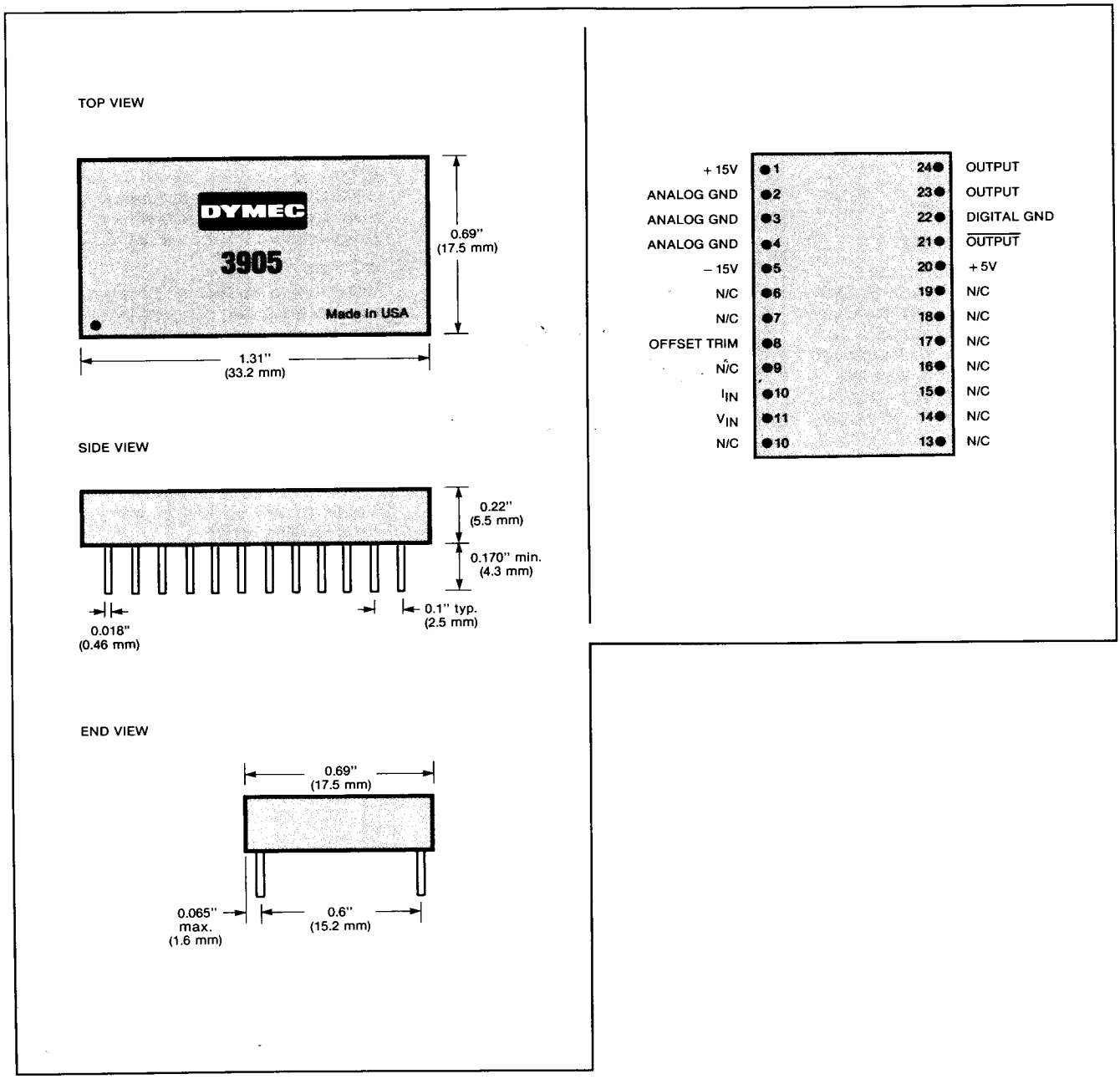


Figure 3. 3905 Mechanical & Pinout

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