

## 2:8 Low Additive Jitter LVDS Buffer

Check for Samples: [CDCLVD1208](#)

### FEATURES

- 2:8 Differential Buffer
- Low Additive Jitter: <300 fs RMS in 10 kHz to 20 MHz
- Low Output Skew of 45 ps (Max)
- Universal Inputs Accept LVDS, LVPECL, LVC MOS
- Selectable Clock Inputs through Control Pin
- 8 LVDS Outputs, ANSI EIA/TIA-644A Standard Compatible
- Clock Frequency up to 800 MHz
- 2.375–2.625V Device Power Supply
- LVDS Reference Voltage,  $V_{AC\_REF}$ , Available for Capacitive Coupled Inputs
- Industrial Temperature Range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Packaged in 5mm x 5mm 28-Pin QFN (RHD)
- ESD Protection Exceeds 3 kV HBM, 1 kV CDM

### APPLICATIONS

- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment
- Wireless Communications
- General Purpose Clocking

### DESCRIPTION

The CDCLVD1208 clock buffer distributes one of two selectable clock inputs (IN0, IN1) to 8 pairs of differential LVDS clock outputs (OUT0, OUT7) with minimum skew for clock distribution. The CDCLVD1208 can accept two clock sources into an input multiplexer. The inputs can either be LVDS, LVPECL, or LVC MOS.

The CDCLVD1208 is specifically designed for driving  $50\ \Omega$  transmission lines. If the input is in single ended mode, the appropriate bias voltage ( $V_{AC\_REF}$ ) should be applied to the unused negative input pin.

The IN\_SEL pin selects the input which is routed to the outputs. If this pin is left open it disables the outputs (static). The part supports a fail safe function. It incorporates an input hysteresis, which prevents random oscillation of the outputs in absence of an input signal

The device operates in 2.5 V supply environment and is characterized from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (ambient temperature). The CDCLVD1208 is packaged in small 28-pin, 5-mm x 5-mm QFN package.

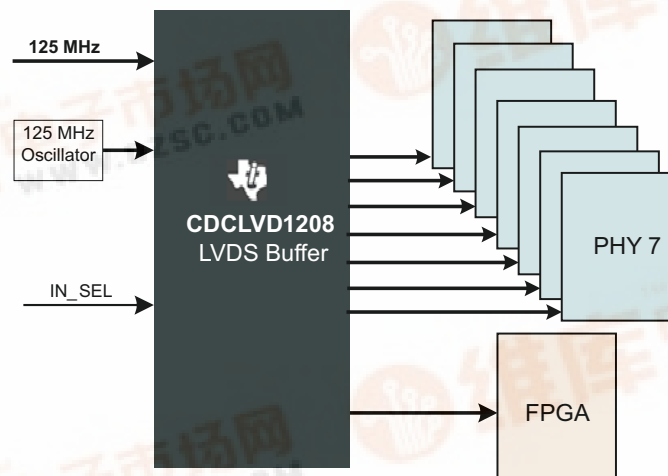


Figure 1. Application Example



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

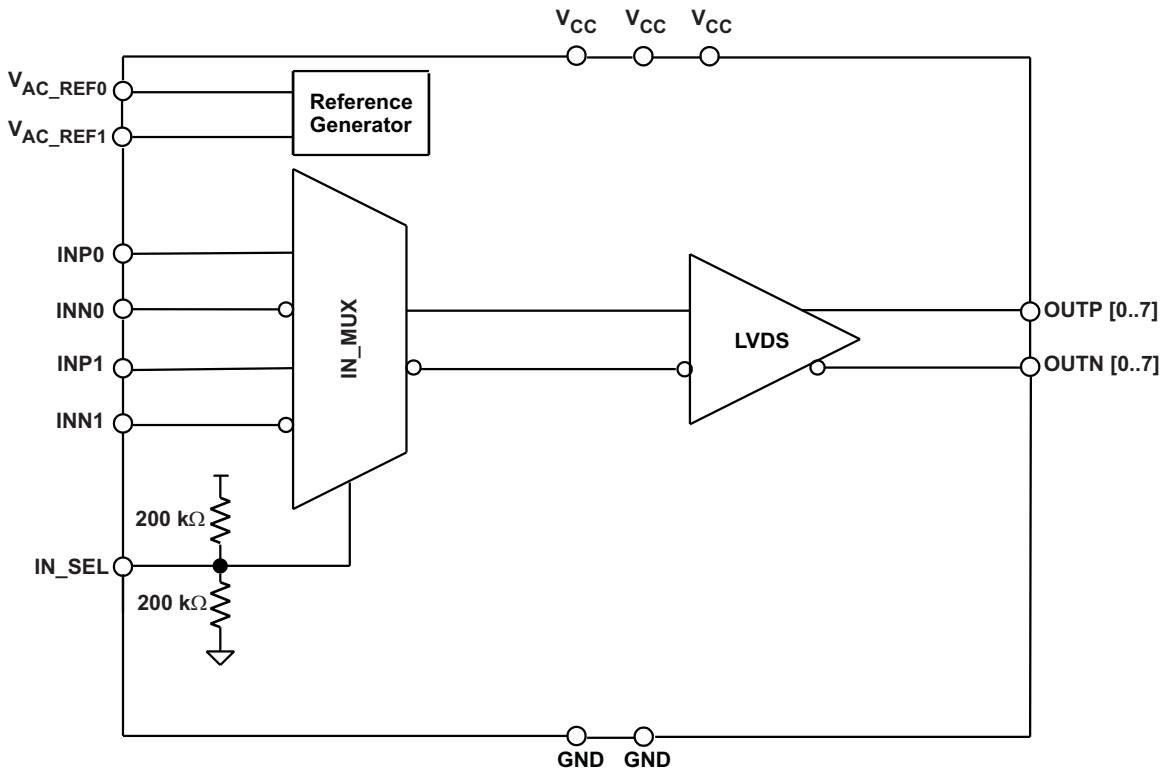
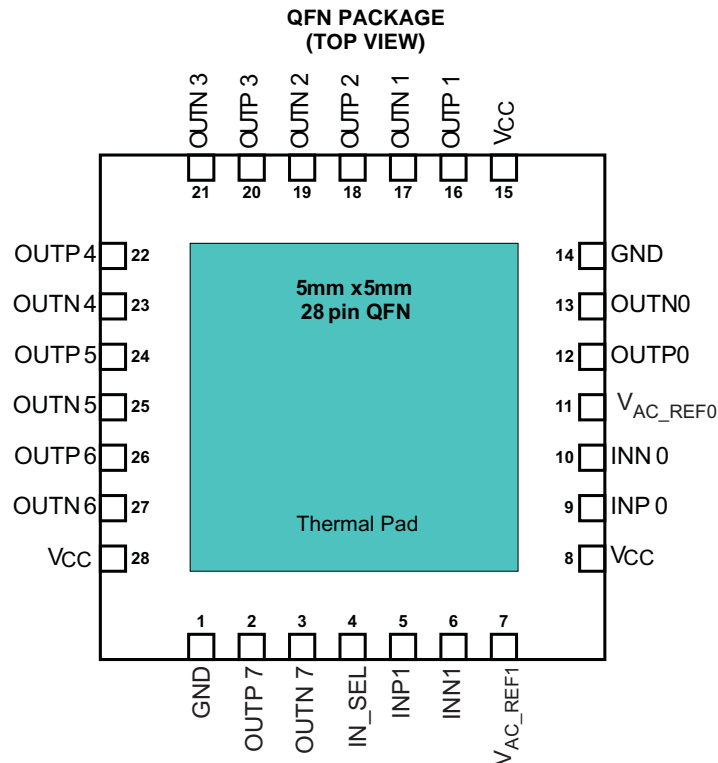


Figure 2. CDCLVD1208 Block Diagram



**PIN FUNCTIONS**

PIN			
NAME	NO.	TYPE	DESCRIPTION
V <sub>CC</sub>	8, 15, 28	Power	2.5V supplies for the device
GND	1, 14	Ground	Device ground
INP0, INN0	9, 10	Input	Differential input pair or single ended input
INP1, INN1	5, 6	Input	Differential redundant input pair or single ended input
OUTP0, OUTN0	12, 13	Output	Differential LVDS output pair no. 0
OUTP1, OUTN1	16, 17	Output	Differential LVDS output pair no. 1
OUTP2, OUTN2	18, 19	Output	Differential LVDS output pair no. 2
OUTP3, OUTN3	20, 21	Output	Differential LVDS output pair no. 3
OUTP4, OUTN4	22, 23	Output	Differential LVDS output pair no. 4
OUTP5, OUTN5	24, 25	Output	Differential LVDS output pair no. 5
OUTP6, OUTN6	26, 27	Output	Differential LVDS output pair no. 6
OUTP7, OUTN7	2, 3	Output	Differential LVDS output pair no. 7
V <sub>AC_REF0</sub>	11	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1μF to GND on this pin.
V <sub>AC_REF1</sub>	7	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1μF to GND on this pin.
IN_SEL	4	Input with internal 200kΩ pull-up and pull-down	Input Selection – selects input port; (See <a href="#">Table 1</a> )
Thermal Pad			See thermal management recommendations

**Table 1. Input Selection Table**

IN_SEL	ACTIVE CLOCK INPUT
0	INP0, INN0
1	INP1, INN1
Open	None <sup>(1)</sup>

(1) The input buffers are disabled and the outputs are static.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	VALUE	UNIT
Supply voltage range, V <sub>CC</sub>	–0.3 to 2.8	V
Input voltage range, V <sub>I</sub>	–0.2 to (V <sub>CC</sub> + 0.2)	V
Output voltage range, V <sub>O</sub>	–0.2 to (V <sub>CC</sub> + 0.2)	V
Driver short circuit current, I <sub>OSD</sub>	See Note <sup>(2)</sup>	
Electrostatic discharge (Human Body Model, 1.5 kΩ, 100 pF)	>3000	V

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) The outputs can handle permanent short.

**RECOMMENDED OPERATING CONDITIONS**

	MIN	TYP	MAX	UNIT
Device supply voltage, V <sub>CC</sub>	2.375	2.5	2.625	V
Ambient temperature, T <sub>A</sub>	–40		85	°C

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		CDCLVD1208	UNITS
		RHD (28 PINS)	
$\theta_{JA}$	Junction-to-ambient thermal resistance	34	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	27	
$\theta_{JB}$	Junction-to-board thermal resistance	9	
$\psi_{JT}$	Junction-to-top characterization parameter	0.4	
$\psi_{JB}$	Junction-to-board characterization parameter	8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## ELECTRICAL CHARACTERISTICS

At  $V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>IN_SEL CONTROL INPUT CHARACTERISTICS</b>					
$V_{dl3}$	3 State	Open	$0.5 \times V_{CC}$		V
$V_{dlH}$	Input high voltage	$0.7 \times V_{CC}$			V
$V_{dlL}$	Input low voltage		$0.2 \times V_{CC}$		V
$I_{dlH}$	Input high current	$V_{CC} = 2.625V$ , $V_{IH} = 2.625V$		30	$\mu A$
$I_{dlL}$	Input low current	$V_{CC} = 2.625V$ , $V_{IL} = 0V$		-30	$\mu A$
$R_{pull(IN\_SEL)}$	Input pull-up/ pull-down resistor		200		k $\Omega$
<b>2.5V LVCMOS (see Figure 7) INPUT CHARACTERISTICS</b>					
$f_{IN}$	Input frequency			200	MHz
$V_{th}$	Input threshold voltage	External threshold voltage applied to complementary input	1.1	1.5	V
$V_{IH}$	Input high voltage		$V_{th} + 0.1$	$V_{CC}$	V
$V_{IL}$	Input low voltage		0	$V_{th} - 0.1$	V
$I_{IH}$	Input high current	$V_{CC} = 2.625V$ , $V_{IH} = 2.625V$		10	$\mu A$
$I_{IL}$	Input low current	$V_{CC} = 2.625V$ , $V_{IL} = 0V$		-10	$\mu A$
$\Delta V/\Delta T$	Input edge rate	20%–80%	1.5		V/ns
$C_{IN}$	Input capacitance		2.5		pF
<b>DIFFERENTIAL INPUT CHARACTERISTICS</b>					
$f_{IN}$	Input frequency	Clock input		800	MHz
$V_{IN, DIFF}$	Differential input voltage peak-to-peak	$V_{ICM} = 1.25V$	0.3	1.6	$V_{PP}$
$V_{ICM}$	Input common mode voltage range	$V_{IN, DIFF, PP} > 0.4V$	1	$V_{CC} - 0.3$	V
$I_{IH}$	Input high current	$V_{CC} = 2.625V$ , $V_{IH} = 2.625V$		10	$\mu A$
$I_{IL}$	Input low current	$V_{CC} = 2.625V$ , $V_{IL} = 0V$		-10	$\mu A$
$\Delta V/\Delta T$	Input edge rate	20%–80%	0.75		V/ns
$C_{IN}$	Input capacitance		2.5		pF

**ELECTRICAL CHARACTERISTICS (continued)**

 At  $V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LVDS OUTPUT CHARACTERISTICS</b>						
$ V_{OD} $	Differential output voltage magnitude	$V_{IN, DIFF, PP} = 0.3V, R_L = 100\ \Omega$	250		450	mV
$\Delta V_{OD}$	Change in differential output voltage magnitude		-15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage		1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP} = 0.6V, R_L = 100\ \Omega$	-15		15	mV
$V_{ring}$	Output overshoot and undershoot	Percentage of output amplitude $V_{OD}$			10%	
$V_{OS}$	Output ac common mode	$V_{IN, DIFF, PP} = 0.6V, R_L = 100\ \Omega$		40	70	mV <sub>PP</sub>
$I_{OS}$	Short-circuit output current	$V_{OD} = 0\ V$			$\pm 24$	mA
$t_{PD}$	Propagation delay	$V_{IN, DIFF, PP} = 0.3\ V$		1.5	2.5	ns
$t_{SK, PP}$	Part-to-part Skew				600	ps
$t_{SK, O}$	Output skew				45	ps
$t_{SK, P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion	-50		50	ps
$t_{RJIT}$	Random additive jitter (with 50% duty cycle input)	Edge speed 0.75 V/ns, 10 kHz – 20 MHz			0.3	ps, RMS
$t_R/t_F$	Output rise/fall time	20% to 80%, 100 $\Omega$ , 5 pF	50		300	ps
$I_{CCSTAT}$	Static supply current	Outputs unterminated, $f = 0\ Hz$		17	28	mA
$I_{CC100}$	Supply current	All outputs, $R_L = 100\ \Omega, f = 100\ MHz$		62	84	mA
$I_{CC800}$	Supply current	All outputs, $R_L = 100\ \Omega, f = 800\ MHz$		87	111	mA
<b><math>V_{AC\_REF}</math> CHARACTERISTICS</b>						
$V_{AC\_REF}$	Reference output voltage	$V_{CC} = 2.5\ V, I_{load} = 100\ \mu A$	1.1	1.25	1.35	V

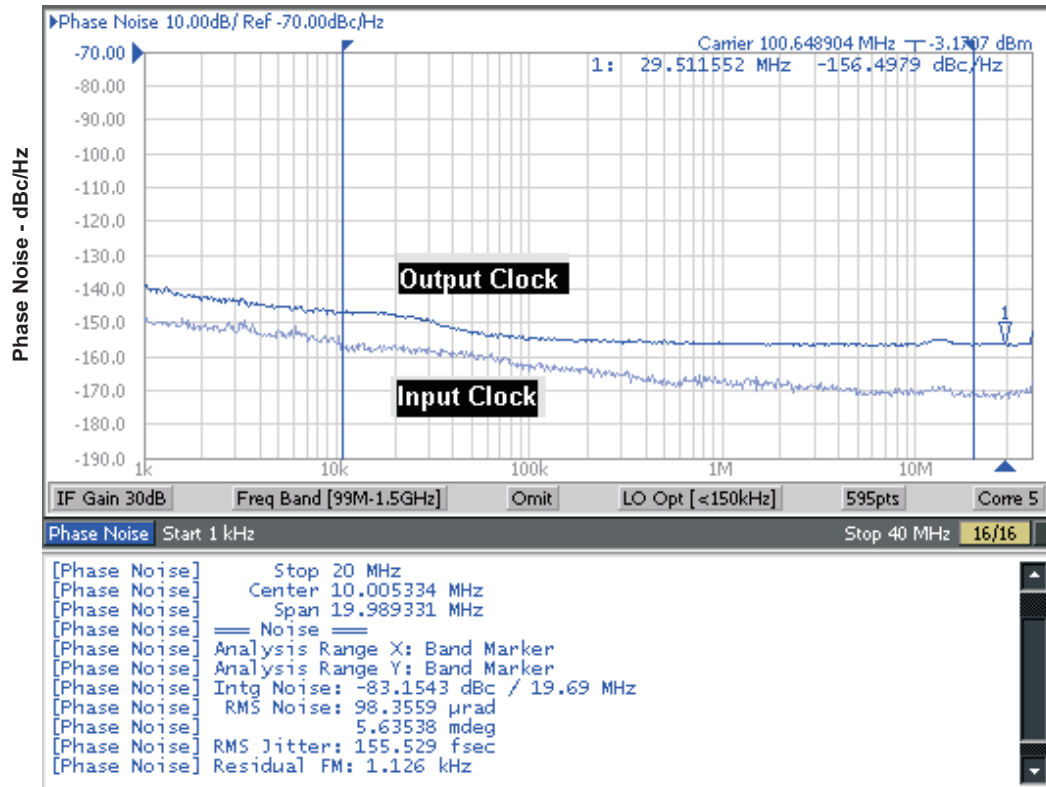
### Typical Additive Phase Noise Characteristics for 100 MHz Clock

PARAMETER		MIN	TYP	MAX	UNIT
phn <sub>100</sub>	Phase noise at 100 Hz offset		-132.9		dBc/Hz
phn <sub>1k</sub>	Phase noise at 1 kHz offset		-138.8		dBc/Hz
phn <sub>10k</sub>	Phase noise at 10 kHz offset		-147.4		dBc/Hz
phn <sub>100k</sub>	Phase noise at 100 kHz offset		-153.6		dBc/Hz
phn <sub>1M</sub>	Phase noise at 1 MHz offset		-155.2		dBc/Hz
phn <sub>10M</sub>	Phase noise at 10 MHz offset		-156.2		dBc/Hz
phn <sub>20M</sub>	Phase noise at 20 MHz offset		-156.6		dBc/Hz
t <sub>RJIT</sub>	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS

### Typical Additive Phase Noise Characteristics for 737.27 MHz Clock

PARAMETER		MIN	TYP	MAX	UNIT
phn <sub>100</sub>	Phase noise at 100 Hz offset		-80.2		dBc/Hz
phn <sub>1k</sub>	Phase noise at 1 kHz offset		-114.3		dBc/Hz
phn <sub>10k</sub>	Phase noise at 10 kHz offset		-138		dBc/Hz
phn <sub>100k</sub>	Phase noise at 100 kHz offset		-143.9		dBc/Hz
phn <sub>1M</sub>	Phase noise at 1 MHz offset		-145.2		dBc/Hz
phn <sub>10M</sub>	Phase noise at 10 MHz offset		-146.5		dBc/Hz
phn <sub>20M</sub>	Phase noise at 20 MHz offset		-146.6		dBc/Hz
t <sub>RJIT</sub>	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

**TYPICAL CHARACTERISTICS**  
**INPUT- AND OUTPUT-CLOCK PHASE NOISES**  
 vs  
**FREQUENCY FROM the CARRIER**  
 (T<sub>A</sub> = 25°C and V<sub>CC</sub> = 2.5V)



Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs

**Figure 3. 100 MHz Input and Output Phase Noise Plot**

**TYPICAL CHARACTERISTICS (continued)**

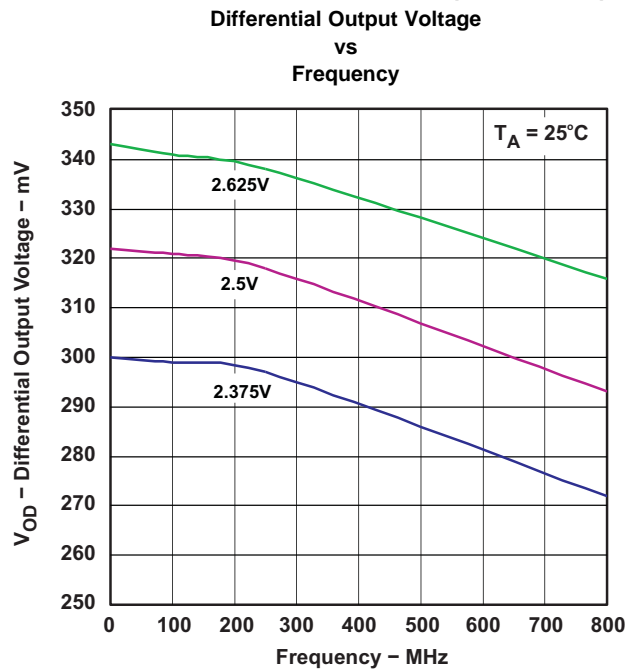


Figure 4.

**TEST CONFIGURATIONS**

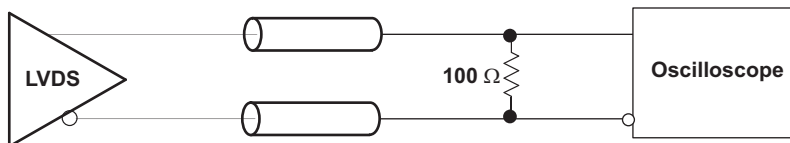


Figure 5. LVDS Output DC Configuration During Device Test

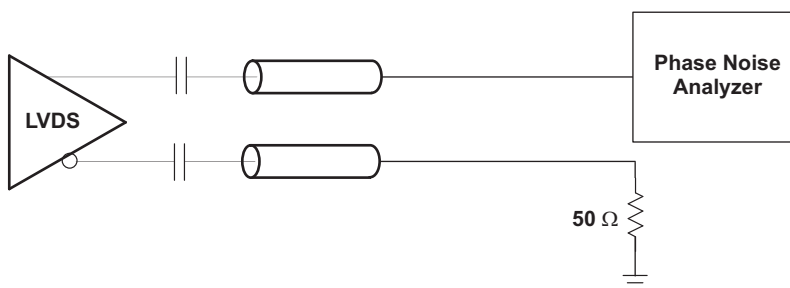


Figure 6. LVDS Output AC Configuration During Device Test



TYPICAL CHARACTERISTICS (continued)

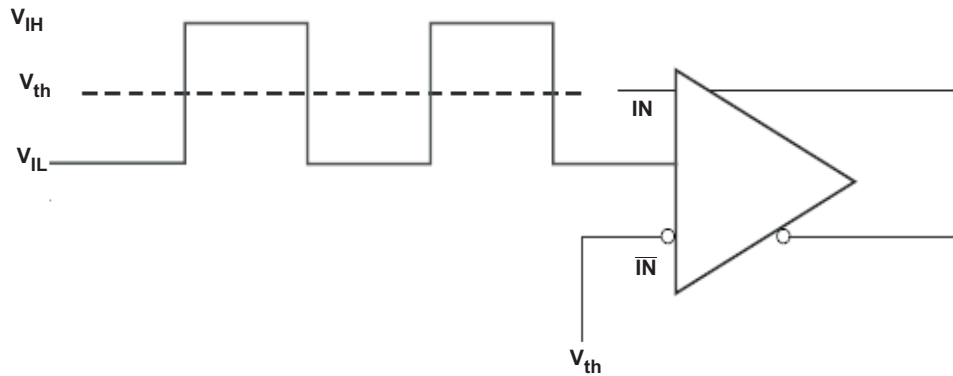


Figure 7. DC Coupled LVCMOS Input During Device Test

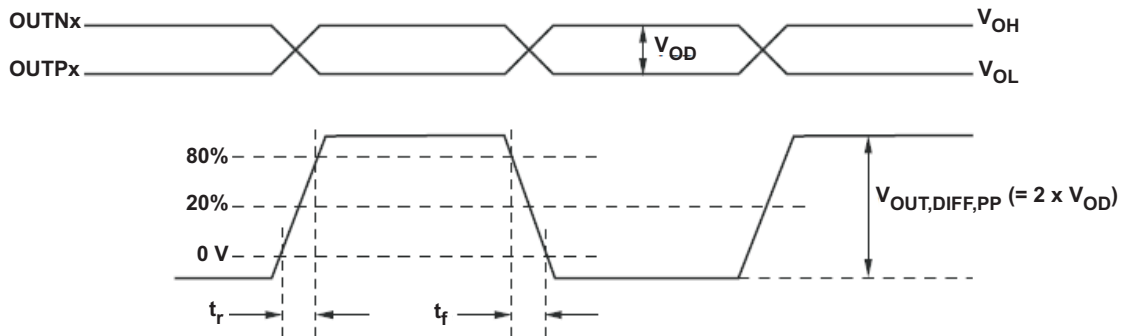
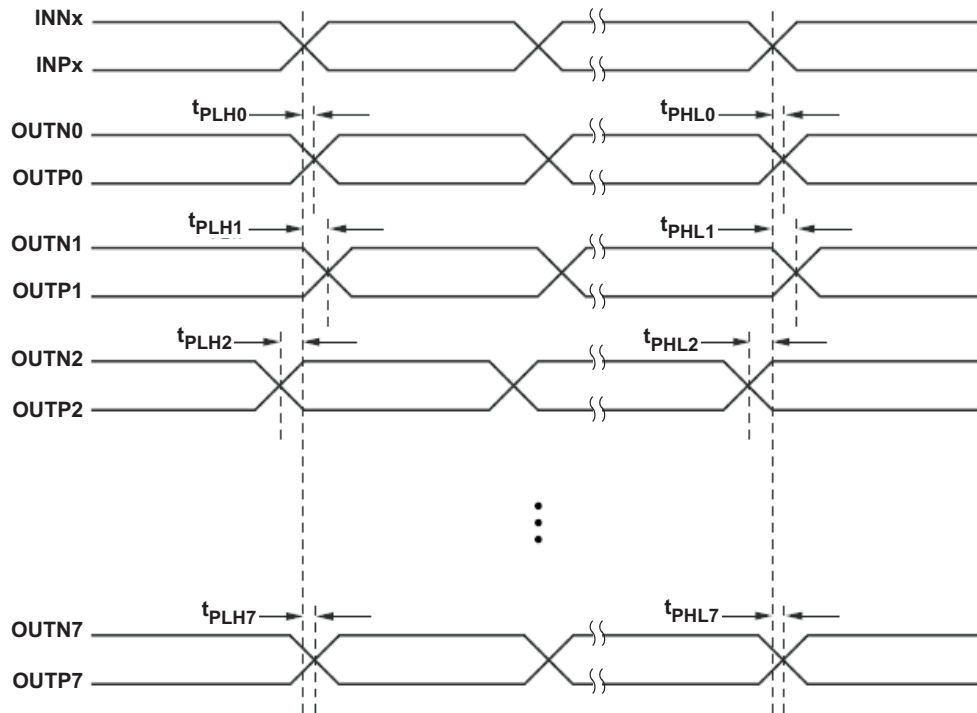


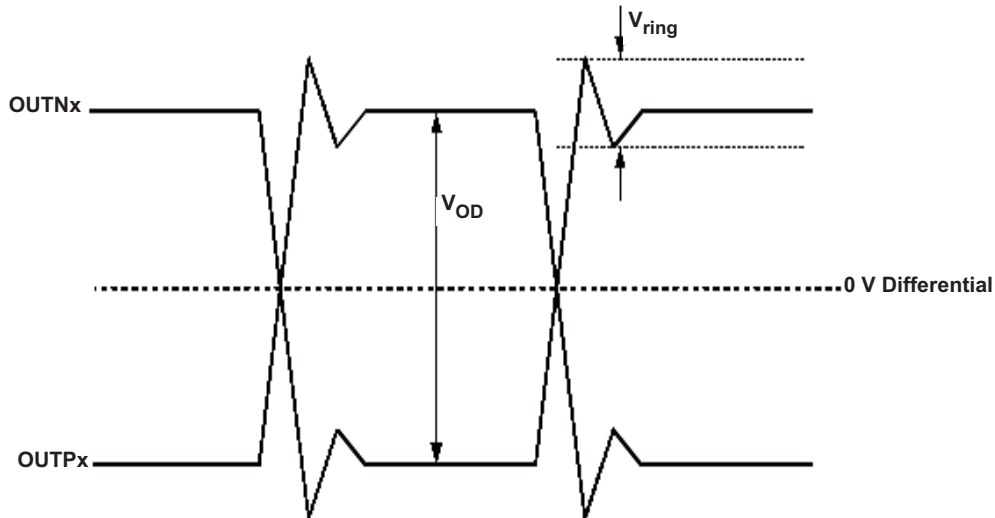
Figure 8. Output Voltage and Rise/Fall Time

**TYPICAL CHARACTERISTICS (continued)**



- A. Output skew is calculated as the greater of the following: As of the difference between the fastest and the slowest t<sub>PLH<sub>n</sub></sub> or the difference between the fastest and the slowest t<sub>PHL<sub>n</sub></sub> (n = 0, 1, 2, ..7)
- B. Part to part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t<sub>PLH<sub>n</sub></sub> or the difference between the fastest and the slowest t<sub>PHL<sub>n</sub></sub> across multiple devices (n = 0, 1, 2, ..7)

**Figure 9. Output Skew and Part-to-Part Skew**



**Figure 10. Output Overshoot and Undershoot**

### TYPICAL CHARACTERISTICS (continued)

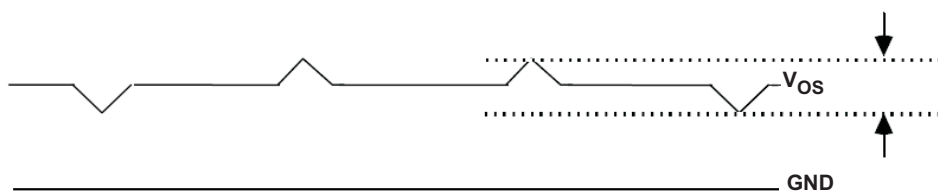


Figure 11. Output AC Common Mode

## APPLICATION INFORMATION

### THERMAL MANAGEMENT

For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Figure 12 shows a recommended land and via pattern.

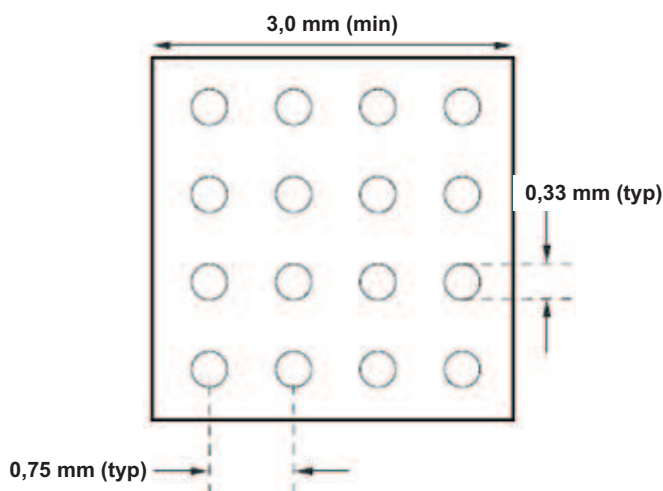


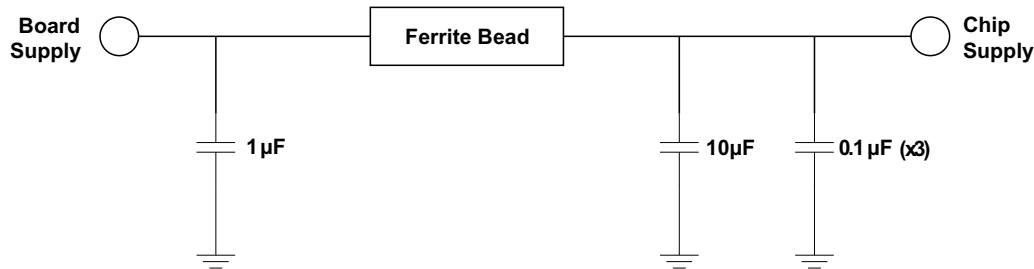
Figure 12. Recommended PCB Layout

### POWER SUPPLY FILTERING

High-performance clock buffers are sensitive to noises on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is critical to the application.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1  $\mu\text{F}$ ) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and

the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

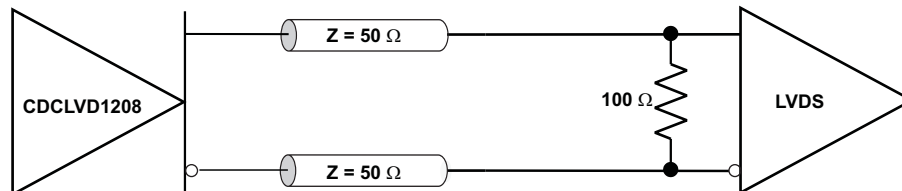


**Figure 13. Power Supply Filtering**

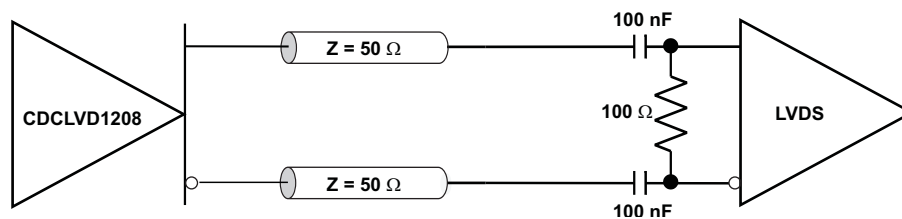
### LVDS OUTPUT TERMINATION

The proper LVDS termination for signal integrity over two 50  $\Omega$  lines is 100  $\Omega$  between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs. It is recommended to place termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common mode voltage of the CDCLVD1208, ac-coupling should be used. If the LVDS receiver has internal 100  $\Omega$  termination, external termination must be omitted.

Unused outputs can be left open without connecting any trace to the output pins.



**Figure 14. LVDS Output DC Termination**



**Figure 15. LVDS Output AC Termination with Receiver Internally Biased**

## INPUT TERMINATION

The CDCLVD1208 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS Driver can be connected to CDCLVD1208 inputs with dc or ac coupling as shown Figure 16 and Figure 17 respectively.

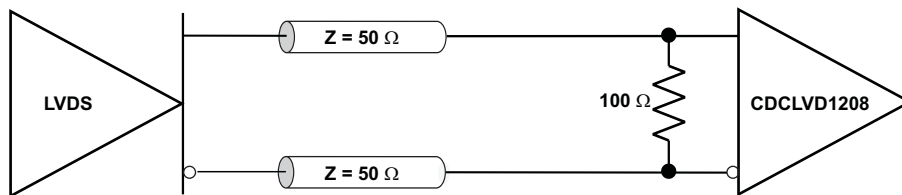


Figure 16. LVDS Clock Driver Connected to CDCLVD1208 Input (DC coupled)

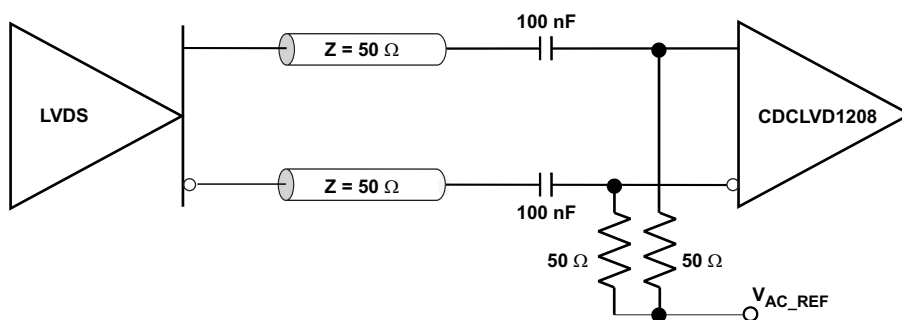


Figure 17. LVDS Clock Driver Connected to CDCLVD1208 Input (AC coupled)

Figure 18 shows how to connect LVPECL inputs to the CDCLVD1208. The series resistors are required to reduce the LVPECL signal swing if the signal swing is  $>1.6$  V<sub>pp</sub>.

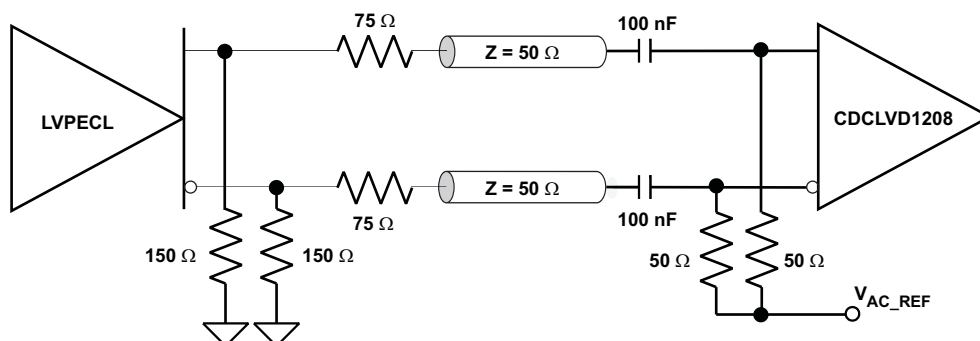
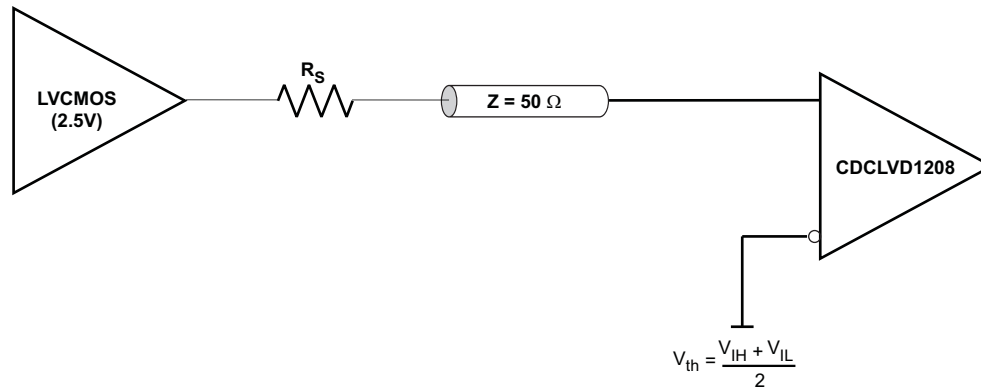


Figure 18. LVPECL Clock Driver Connected to CDCLVD1208 Input

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Figure 19 illustrates how to couple a 2.5 V LVC MOS clock input to the CDCLVD1208 directly. The series resistance ( $R_S$ ) should be placed close to the LVC MOS driver if needed. 3.3 V LVC MOS clock input swing needs to be limited to  $V_{IH} \leq V_{CC}$ .



**Figure 19. 2.5V LVC MOS Clock Driver Connected to CDCLVD1208 Input**

For unused input, it is recommended to ground both input pins (INP, INN) using 1 k $\Omega$  resistors.



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PACKAG

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp
CDCLVD1208RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
CDCLVD1208RHDT	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com> for more information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all RoHS materials, with the exception of lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in applications that require high temperature soldering processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based eutectic solder used between the leadframe and die. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (both of which are RoHS prohibited materials) in homogeneous material.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD1208RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCLVD1208RHDT	VQFN	RHD	28	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

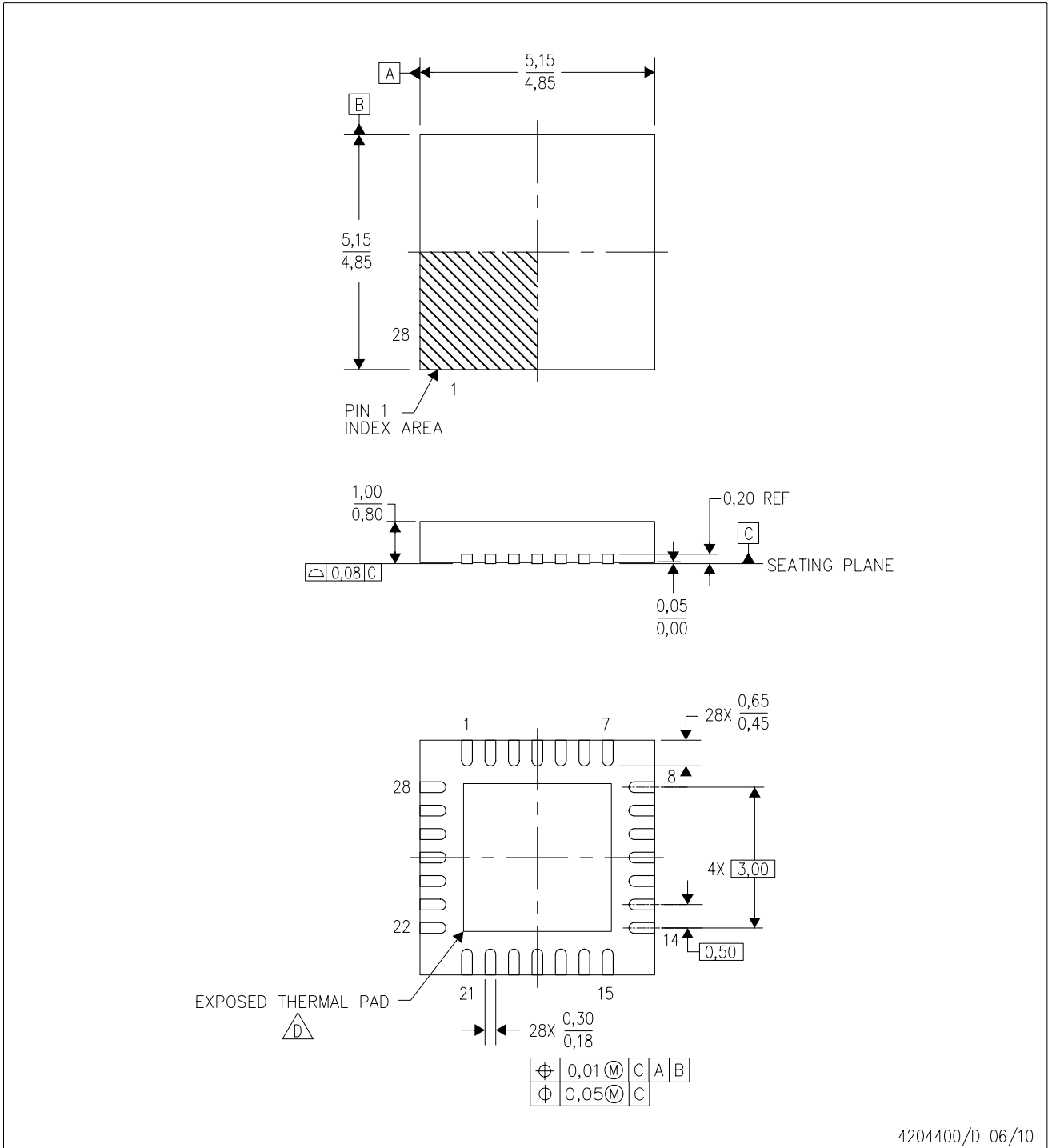


**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD1208RHDR	VQFN	RHD	28	3000	340.5	333.0	20.6
CDCLVD1208RHDT	VQFN	RHD	28	250	340.5	333.0	20.6



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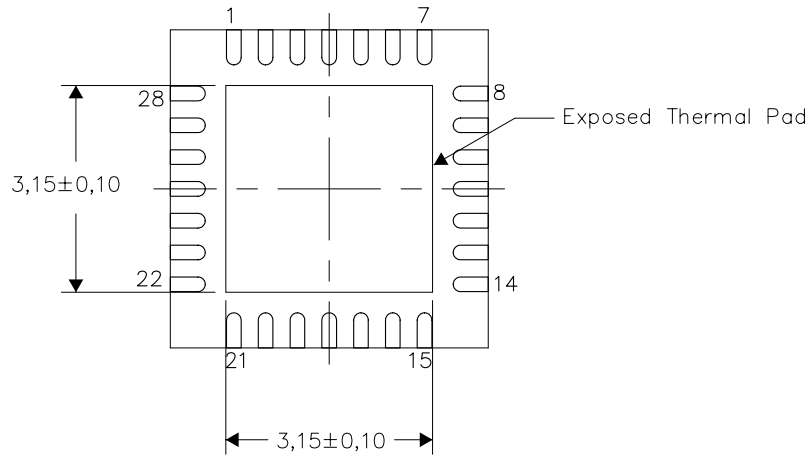
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



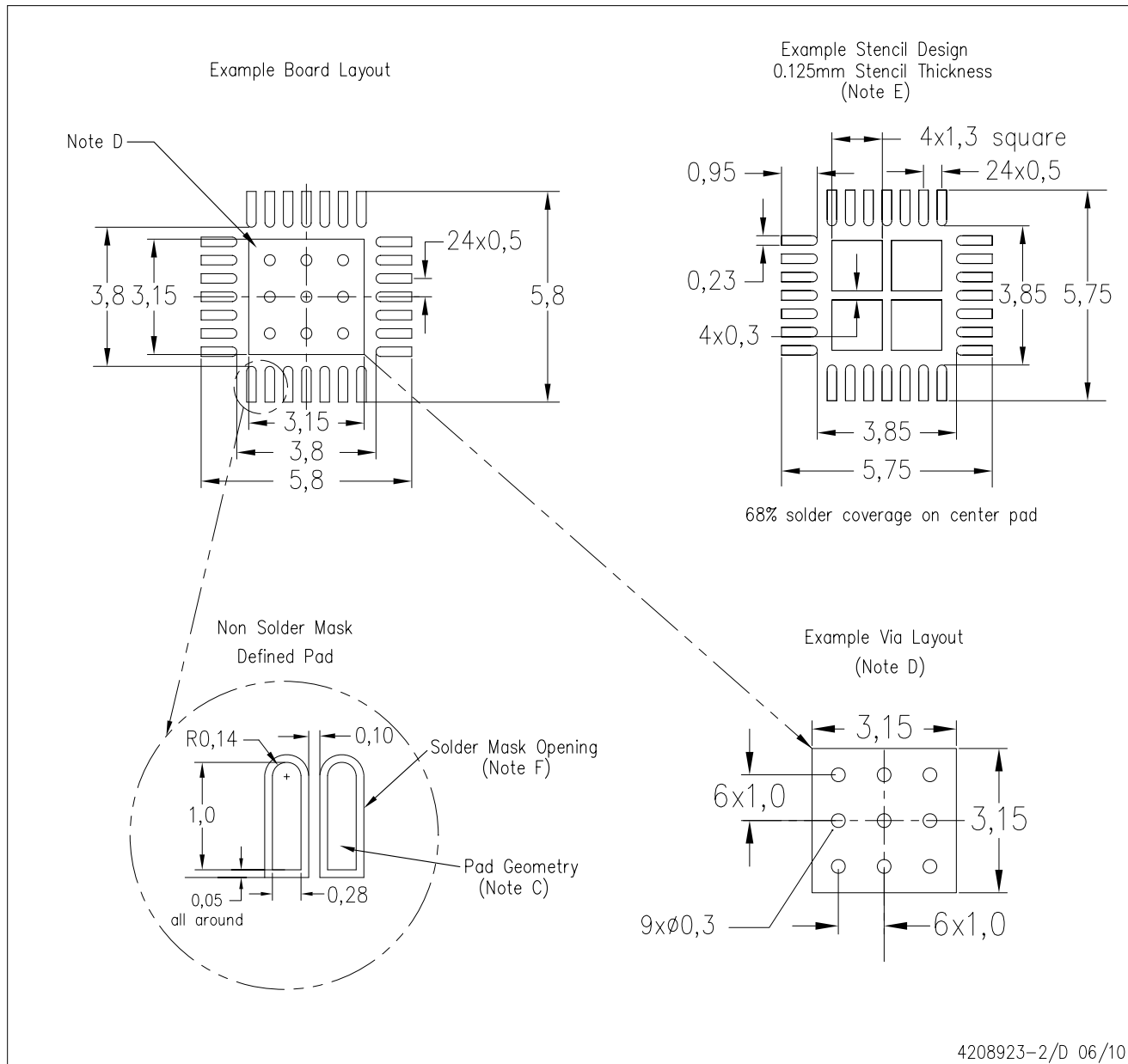
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHD (S-PVQFN-N28)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
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