

OKI semiconductor

MSM6355

LCD CONTROLLER LSI

GENERAL DESCRIPTION

MSM6355GS is a controller for large capacity dot matrix liquid crystal displays. Since the configuration of the internal register is based on the MSM6255, it is compatible with the MSM6255 in software instructions.

This controller has more function than the MSM6255. There are scrolling per character unit in the horizontal direction, smooth scrolling per character unit in the vertical direction and shifting the graphic cursor. The MSM6355GS is configured to make these extra functions very easy to implement.

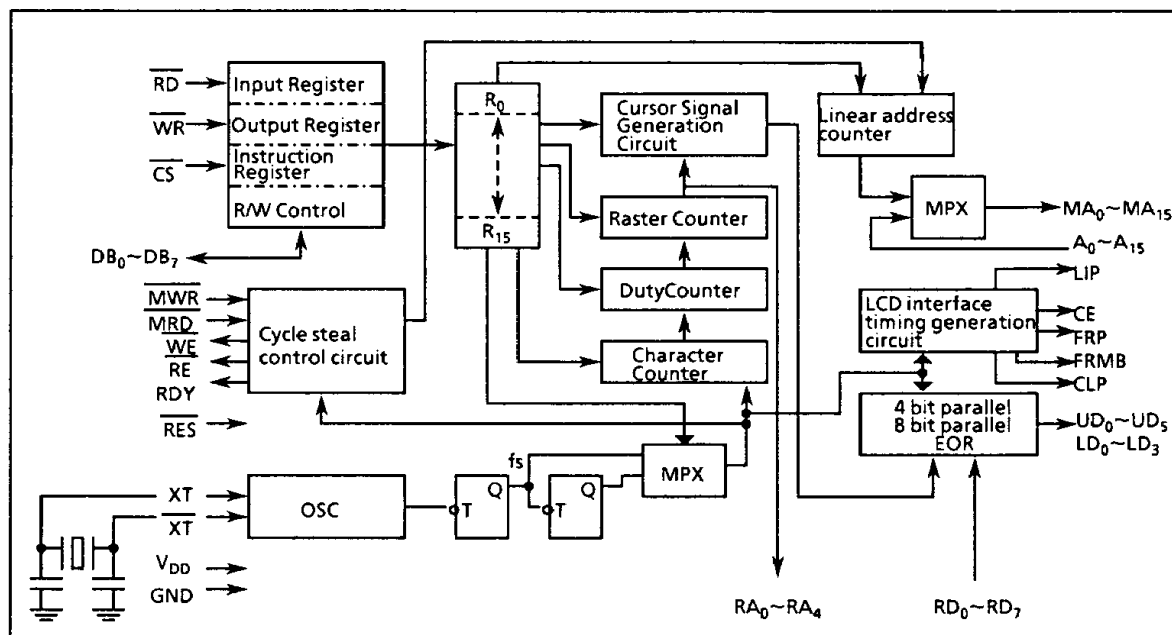
FEATURES

- Software is compatible with MSM6255.
- Graphic cursor function
 - The cursor display up to 32 dots both horizontally and vertically is possible in the graphic mode.
- Scrolling function
 - Scrolling of character units in the horizontal direction is possible.
 - Smooth scrolling per character unit in the vertical direction is possible.
- A built-in "cycle steal" circuit is provided.
- Display configuration: Vertical screen division can be selected.
- The screen size
 - Vertical : 104 dots(max.), 2048 dots(max.) when the screen is divided vertically.
 - Horizontal : 2048 dots(max.)
- Display duty : 1/2 - 1/1024
- Character font
 - Vertical direction : 1~32 dots
 - Horizontal direction : 8 dots fixed
- Cursor : ON/OFF, blinking speed, form and position are programmable.
- LCD driver interface : 4bit/8bit parallel
- Process : CMOS
- Single power source : $5V \pm 10\%$
- 80 pin Plastic QFP (QFP80-P-1420-K)

PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	MA ₅	17	A ₅	33	UD ₀	49	DB ₂	65	RA ₂
2	MA ₄	18	A ₄	34	UD ₁	50	DB ₃	66	RA ₃
3	MA ₃	19	A ₃	35	UD ₂	51	DB ₄	67	RA ₄
4	MA ₂	20	A ₂	36	UD ₃	52	DB ₅	68	XT
5	MA ₁	21	A ₁	37	DIEN	53	DB ₆	69	$\overline{\text{XT}}$
6	MA ₀	22	A ₀	38	$\overline{\text{CS}}$	54	DB ₇	70	V _{SS}
7	A ₁₅	23	FRP	39	$\overline{\text{RD}}$	55	RD ₀	71	MA ₁₅
8	A ₁₄	24	LIP	40	$\overline{\text{WR}}$	56	RD ₁	72	MA ₁₄
9	A ₁₃	25	CE Φ	41	$\overline{\text{MWR}}$	57	RD ₂	73	MA ₁₃
10	A ₁₂	26	CLP	42	$\overline{\text{MRD}}$	58	RD ₃	74	MA ₁₂
11	A ₁₁	27	FRMB	43	$\overline{\text{WE}}$	59	RD ₄	75	MA ₁₁
12	A ₁₀	28	LD ₀	44	$\overline{\text{RE}}$	60	RD ₅	76	MA ₁₀
13	A ₉	29	LD ₁	45	RDY	61	RD ₆	77	MA ₉
14	A ₈	30	LD ₂	46	$\overline{\text{RES}}$	62	RD ₇	78	MA ₈
15	A ₇	31	LD ₃	47	DB ₀	63	RA ₀	79	MA ₇
16	A ₆	32	V _{DD}	48	DB ₁	64	RA ₁	80	MA ₆

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	$T_a = 25^\circ\text{C}$	- 0.3~6	V
Input voltage	V_I	$T_a = 25^\circ\text{C}$	- 0.3~ V_{DD}	V
Storage temperature	T_{STg}	—	- 50~150	$^\circ\text{C}$

● Operating Range

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	—	4.5~5.5	V
Working temperature	T_{OP}	—	- 20~85	$^\circ\text{C}$
Operating frequency	$f_{(OSC)}$	$V_{DD} = 5V \pm 10\%$	0~11	MHz

● Input Characteristics

$V_{DD} = 5V \pm 10\%$, $T_a = -20 \sim 85^\circ\text{C}$

Parameter	Symbol	MIN	TYP	MAX	Unit	Applicable pin
High input voltage	V_{IH}	2.8	—	—	V	$\overline{A0} \sim \overline{A15}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{MRD}$, $\overline{MWR}$, $\overline{DIEN}$, $\overline{RD0} \sim \overline{RD7}$, $\overline{RES}$
Low input voltage	V_{IL}	—	—	0.7	V	
High input voltage	V_{IH}	4.0	—	—	V	XT, $\overline{DB0} \sim \overline{DB7}$
Low input voltage	V_{IL}	—	—	1.0	V	
High input current	I_{IH}	—	—	- 1	μA	$\overline{DB0} \sim \overline{DB7}$, $\overline{A0} \sim \overline{A15}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{MRD}$, $\overline{MWR}$, $\overline{DIEN}$, $\overline{RD0} \sim \overline{RD7}$, $\overline{RES}$
Low input current	I_{IL}	—	—	+ 1	μA	

● Output Characteristics

$V_{DD} = 5V \pm 10\%$, $T_a = -20 \sim 85^\circ\text{C}$

Parameter	Symbol	Symbol	MIN	TYP	MAX	Unit	Applicable pin
High output voltage	V_{OH}	$I_O = -500\mu\text{A}$	2.8	—	—	V	$\overline{LD0} \sim \overline{LD3}$, $\overline{UD0} \sim \overline{UD3}$, $\overline{MA0} \sim \overline{MA15}$, $\overline{RA0} \sim \overline{RA4}$, $\overline{DB0} \sim \overline{DB7}$, $\overline{CE\Phi}$, $\overline{LIP}$, $\overline{FRP}$, $\overline{FRMB}$, $\overline{CLP}$, $\overline{WE}$, $\overline{RE}$, $\overline{RDY}$
Low output voltage	V_{OL}	$I_O = 2.4\text{mA}$	—	—	0.4	V	

● Current Consumption

 $V_{DD} = 5V \pm 10\%$, $T_a = -20 \sim 85^\circ\text{C}$

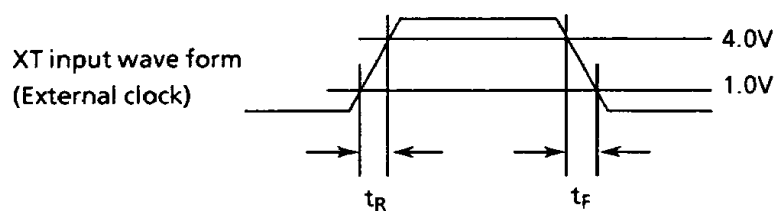
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Static current	I_{DDs}	$f_{(OSC)} = 0 \text{ MHz}$, No load	—	—	50	μA
Operating current	I_{DDs}	$f_{(OSC)} = 10 \text{ MHz}$, No load	—	—	16	mA

Note: The input terminal shall be VDD or GND.

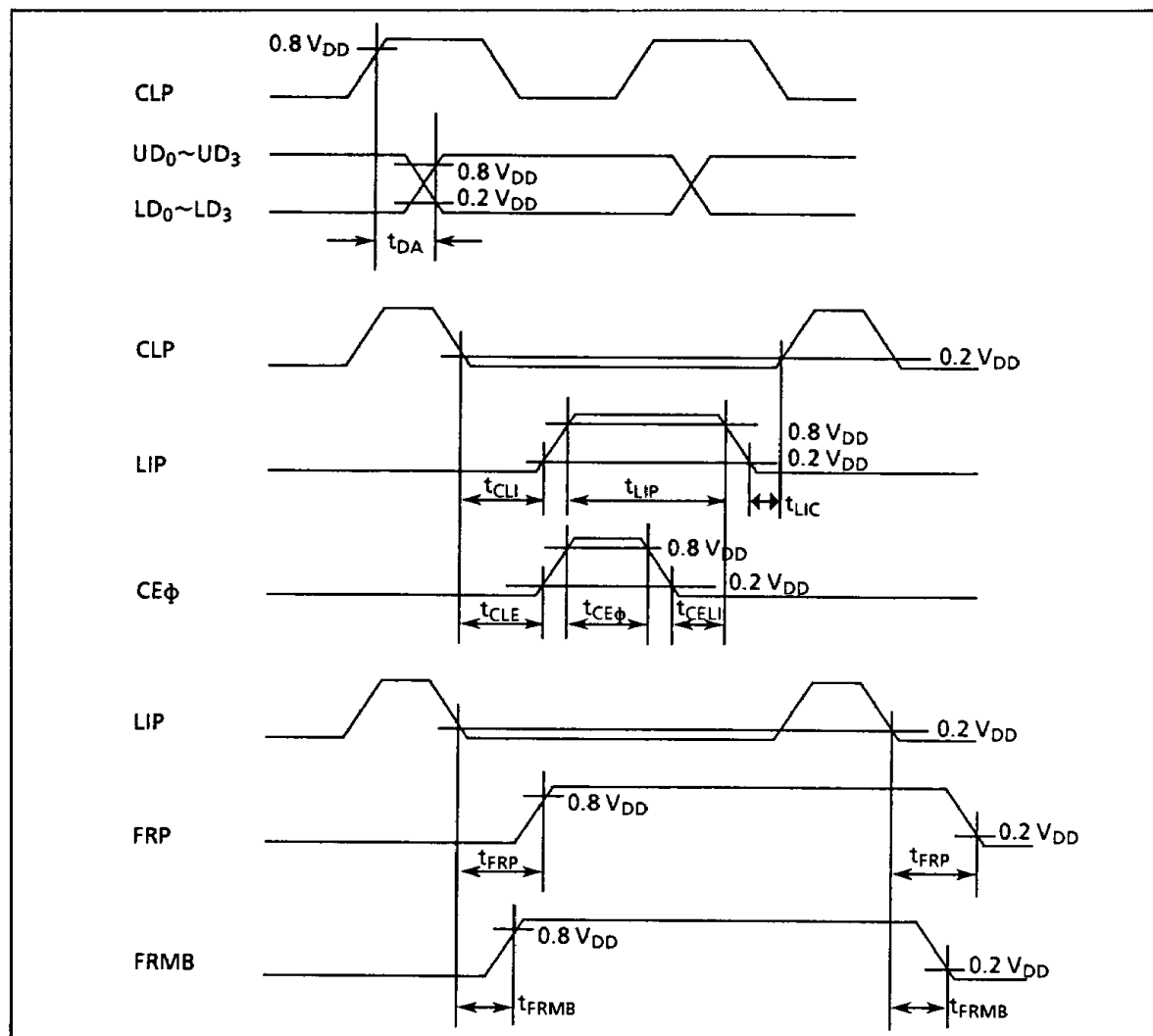
● Operating Frequency

 $V_{DD} = 5V \pm 10\%$, $T_a = -20 \sim 85^\circ\text{C}$

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Oscillation frequency	$f_{(OSC)}$	—	—	11	MHz	Crystal oscillation
External clock frequency	f_{IN}	—	—	11	MHz	External clock
Clock rise and fall times	t_R t_F	—	—	50 50	ns ns	Crystal oscillation
Clock duty	Duty	40	50	60	%	External clock



LCD DRIVER INTERFACE TIMING CHARACTERISTICS

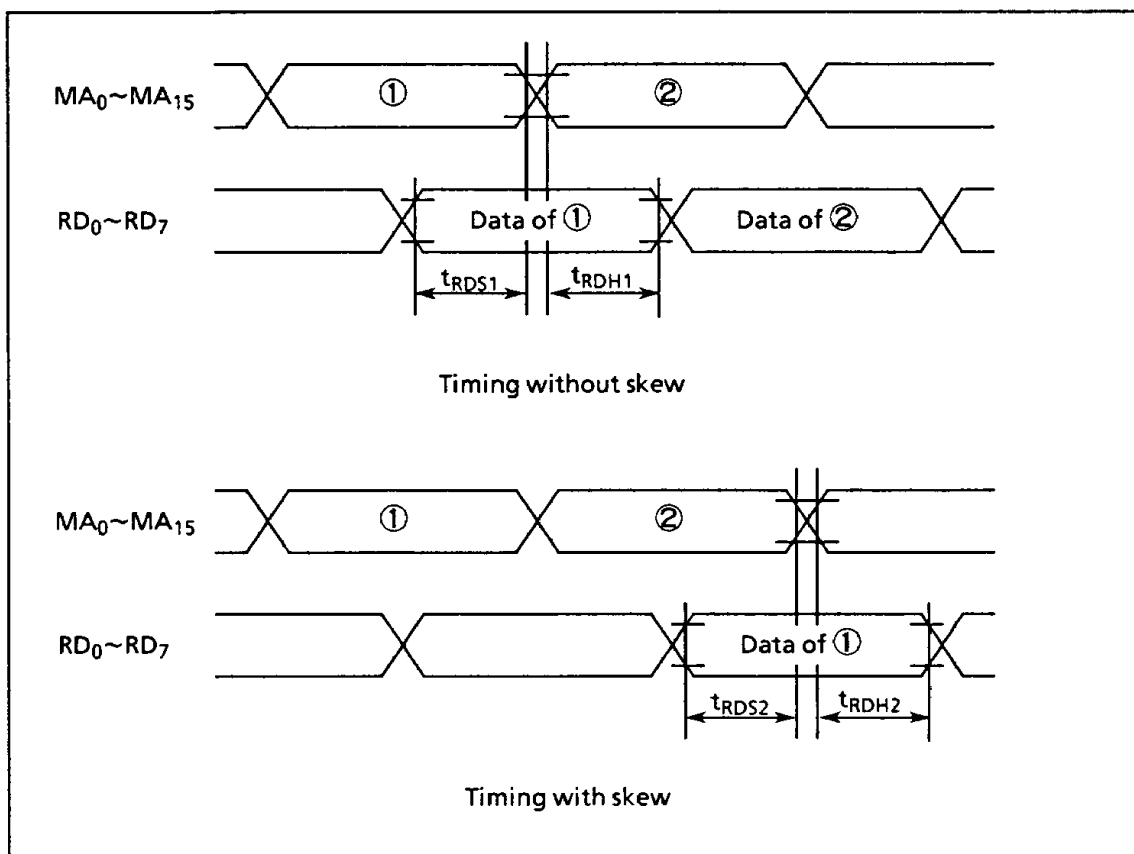


($C_L = 30\text{PF}$, $V_{DD} = 5\text{V} \pm 10\%$, $T_a = -20 \sim 85^\circ\text{C}$)

Parameter	Symbol	MIN	TYP	MAX	Unit
Data delay time	t_{DA}	0		50	ns
CLP→LIP time	t_{CLI}	—	$t_{CH\phi}/2$	—	ns
LIP→CIP time	t_{LIC}	—	$t_{CH\phi}/4$, $t_{CH\phi}/2$ (Note)	—	ns
Latch signal "H" time	t_{LIP}	—	$t_{CH\phi}/2$	—	ns
CLP→CE ϕ time	t_{CLE}	—	$t_{CH\phi}/2$	—	ns
Chip enable "H" time	$t_{CE\phi}$	—	$t_{CH\phi}/4$	—	ns
CE ϕ →LIP time	t_{CELI}	—	$t_{CH\phi}/2$	—	ns
LIP→FRP time	t_{FRP}	—	$t_{CH\phi}/2$	—	ns
LIP→FRMB time	t_{FRMB}	0		100	ns

Note: $t_{CH\phi}/4$ is in 4bit parallel mode.
 $t_{CH\phi}/2$ is in 8bit parallel mode.

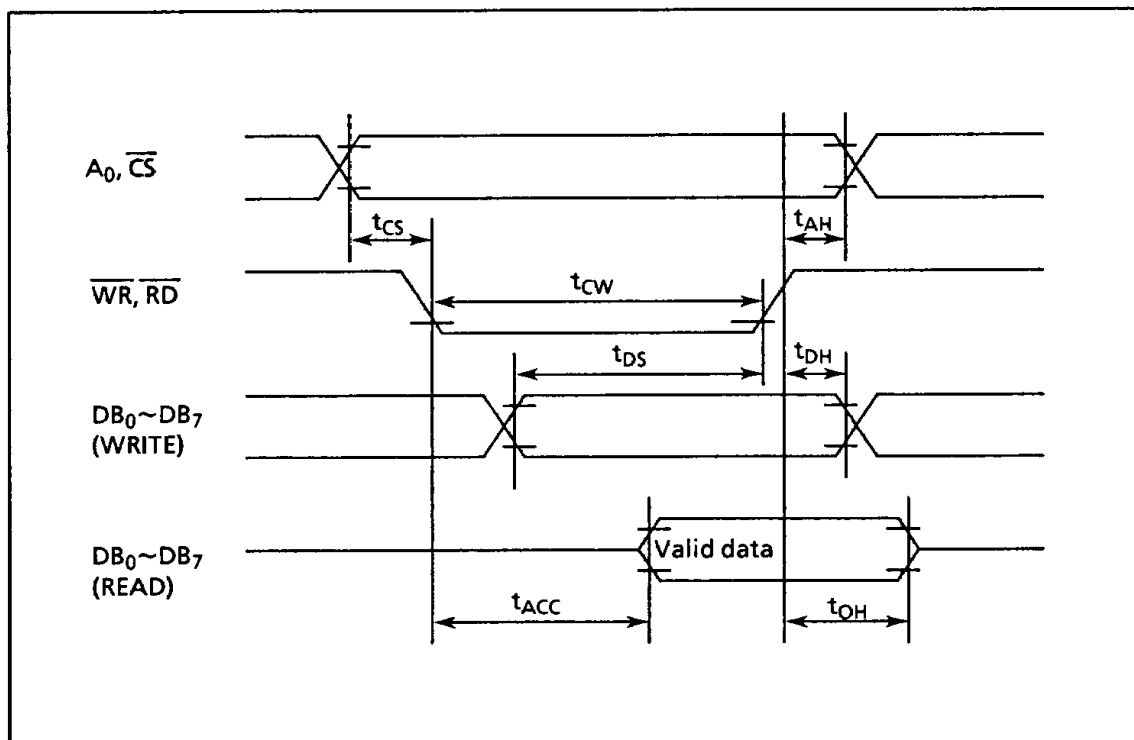
PATTERN DATA TAKE TIMING



($C_L = 30PF$, $V_{DD} = 5V \pm 10\%$, $T_a = -20 \sim 85^\circ C$)

Parameter	Symbol	MIN	TYP	MAX	Unit
Pattern data setup time	t_{RDS}	100	—	—	ns
Pattern data hold time	t_{RDH}	30	—	—	ns

CPU BUS TIMING CHARACTERISTICS

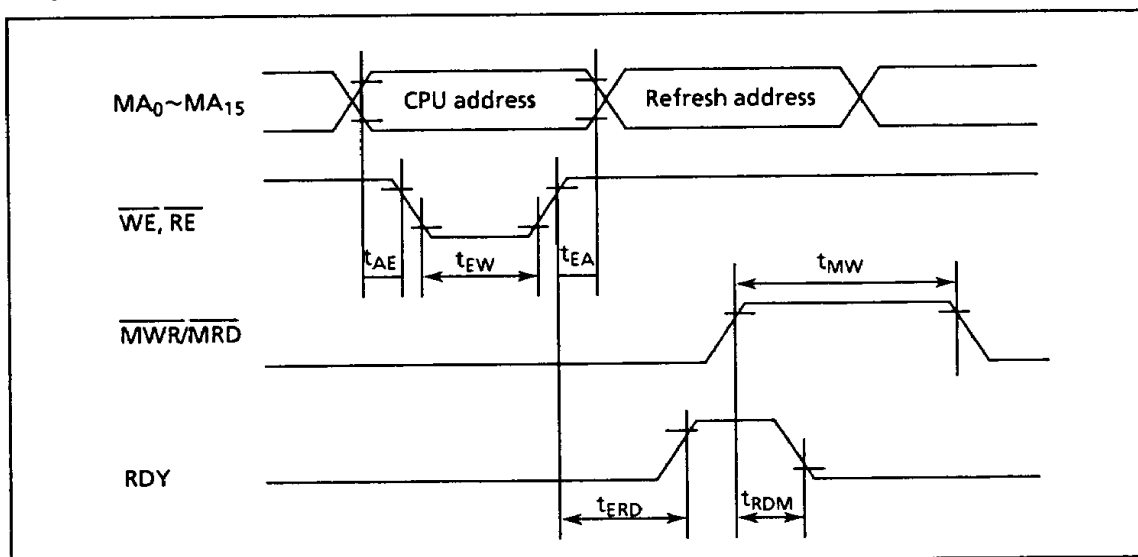


($C_L = 30PF$, $V_{DD} = 5V \pm 10\%$, $T_a = -20 \sim 85^\circ C$)

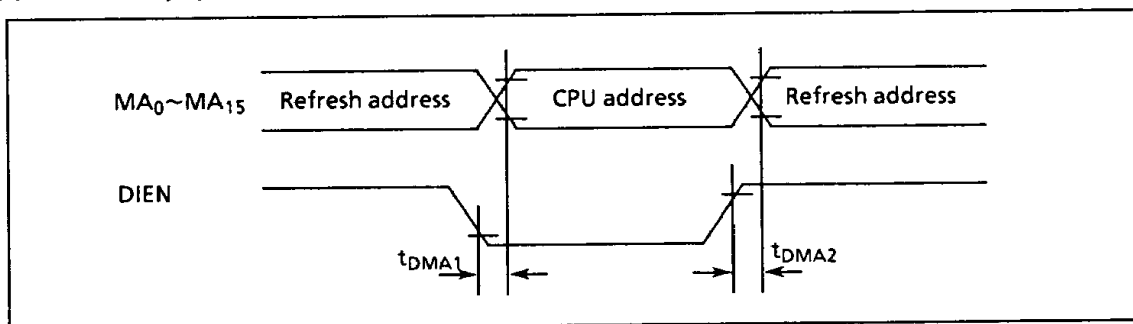
Parameter	Symbol	MIN	TYP	MAX	Unit
A_0 and $\overline{CS}$ setup time	t_{CS}	50	—	—	ns
$\overline{WR}$ and $\overline{RD}$ pulse width	t_{CW}	300	—	—	ns
Address hold time	t_{AH}	20	—	—	ns
Data setup time	t_{DS}	200	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
Output disable time	t_{OH}	0	—	40	ns
Access time	t_{ACC}	0	—	200	ns

ADDRESS BUS SWITCH TIMING

(1) Synchronized Access System



(2) CPU Priority System

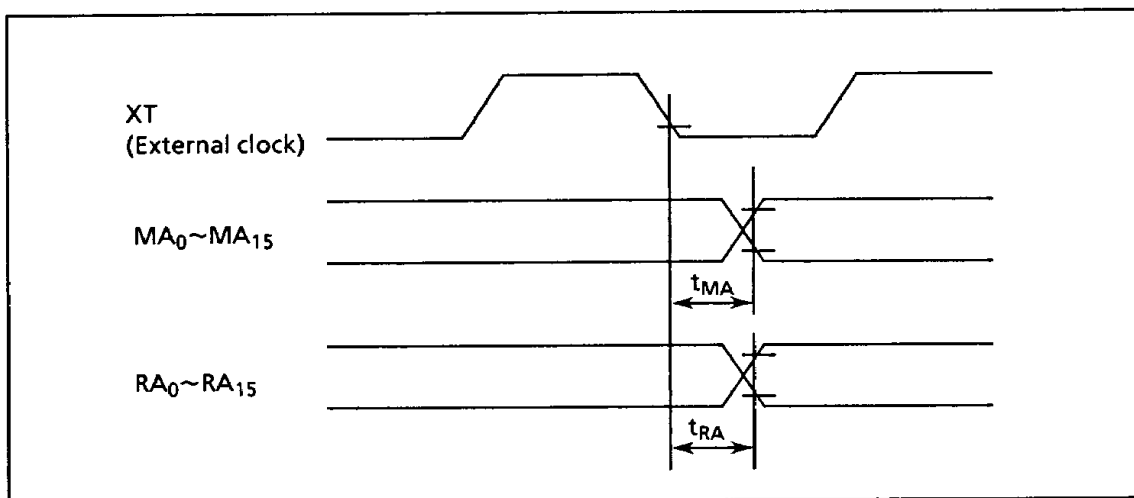


($C_L = 50\text{PF}$, $V_{DD} = 5\text{V} \pm 10\%$, $T_a = -20 \sim 85^\circ\text{C}$)

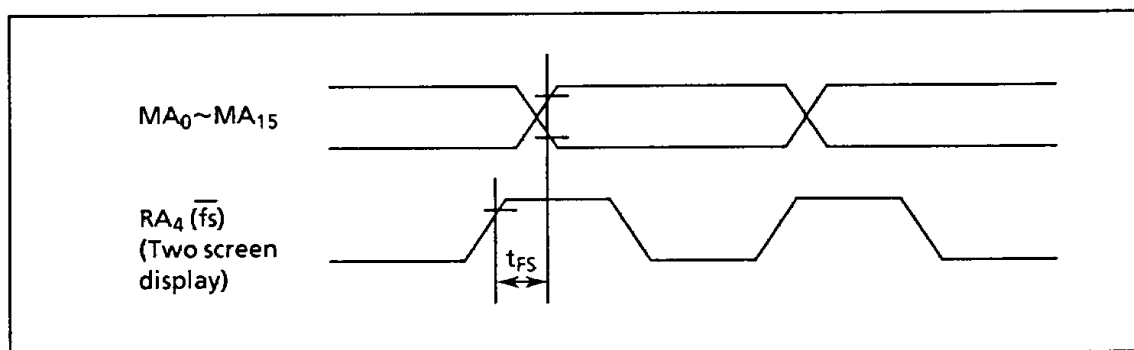
Parameter	Symbol	MIN	TYP	MAX	Unit
CPU address→ $\overline{\text{WE}}/\overline{\text{RE}}$ time	t_{AE}	-10	—	40	ns
$\overline{\text{WE}}/\overline{\text{RE}}$ →CPU address time	t_{EA}	0	—	50	ns
$\overline{\text{WE}}/\overline{\text{RE}}$ pulse width (two screen display)	t_{EW}	$t_{\text{CH}\phi}/4-60$	—	$t_{\text{CH}\phi}/4$	ns
$\overline{\text{WE}}/\overline{\text{RE}}$ pulse width (one screen display)		$t_{\text{CH}\phi}/2-60$	—	$t_{\text{CH}\phi}/2$	ns
$\overline{\text{WE}}/\overline{\text{RE}}$ →RDY time	t_{ERD}	0	—	50	ns
$\overline{\text{MWR}}/\overline{\text{MRD}}$ →RDY time	t_{RDM}	0	—	50	ns
CPU address delay time	t_{DMA1}	0	—	100	ns
Refresh address delay time	t_{DMA2}	0	—	100	ns
$\overline{\text{MWR}}/\overline{\text{MRD}}$ pulse width	t_{MW}	$t_{\text{CH}\phi}$	—	—	ns

MEMORY ADDRESS TIMING CHARACTERISTICS

(1) Without Skew



(2) CPU Priority System



($C_L = 30PF$, $V_{DD} = 5V \pm 10\%$, $T_a = -20 \sim 85^\circ C$)

Parameter	Symbol	MIN	TYP	MAX	Unit
Memory address delay time	t_{MA}	0	—	110	ns
Raster address delay time	t_{RA}	0	—	110	ns
RA ₄ →memory address time	t_{FS}	0	—	100	ns

PIN DESCRIPTION

Classification	Pin Name	I/O	Function			
Power source	V _{DD}	I	Connect to + 5V power source			
	V _{SS}	I	Connect to 0V			
LCD driver	UD ₀ ~UD ₃	O		One screen display		Two screen display
				4 bit parallel	8bit parallel	8bit parallel
	LD ₀ ~LD ₃	O	UD ₀ ~UD ₃		Display data output terminal	Upper screen display terminal
			LD ₀ ~LD ₃	Display data output terminal	Display data output terminal	Lower screen display terminal
	LIP	O	The latch clock for display data			
	CLP	O	The shift clock for display data			
	FRMB	O	Liquid crystal drive output AC signal			
	FRP	O	Frame signal			
	CE ϕ	O	The chip enable clock of the segment driver			
Display memory	MA ₀ ~MA ₁₅	O	Address output for display RAM			
	RA ₀ ~RA ₄	O	Raster address output			
	RD ₀ ~RD ₇	I	Input of the character dot data and bit map data			
	$\overline{\text{WE}}$	O	Control signal for writing of the display RAM			
	$\overline{\text{RE}}$	O	Latch clock for reading the display RAM			
CPU	$\overline{\text{CS}}$	I	Chip select input. It is possible to read from and write to the internal register of LCDC during "L" level.			
	$\overline{\text{RD}}$	I	The data reading from the internal register is possible during "L" level.			
	$\overline{\text{WR}}$	I	The writing to the internal register is carried out on the rise edge.			
	$\overline{\text{MRD}}$	I	The read signal input of the display RAM			
	$\overline{\text{MWR}}$	I	The write signal input of the display RAM			
	RDY	O	Ready output. After the $\overline{\text{WE}}$ signal is output at normal "L" level, the level becomes "H" level.			
	$\overline{\text{RES}}$	I	Reset input. The internal counter of LCDC is reset at "L" level. Refer to the "RESET" for details.			
	DB ₀ ~DB ₇	I/O	8 bit data bus -- Input/output common terminal			
	A ₀ ~A ₁₅	I	CPU address input of the memory address			
	DIEN	I	The switch over signal input of the CPU address and refresh address bus inside LCDC. This is effective when switching over the direct address bus using the external signal without using the cycle steal bus.			
Signal source	XT	I	Crystal oscillator connection terminal. When using the external clock, input to XT terminal, and disconnect $\overline{\text{XT}}$.			
	$\overline{\text{XT}}$	I				

LIST OF LCDC INTERNAL REGISTERS

The internal register has one unit of instruction register (IR) and 16 units of the data register (Rn).
The selection of the instruction register and data register is to be carried out by using A₀ terminal.

Table 1 The Internal Registers of MSM6355

CS	A ₀	IR bit				Register	Register Name	R/W	Rn bit							
		3	2	1	0				7	6	5	4	3	2	1	0
1	*	*	*	*	*		Invalid									
0	1	*	*	*	*	IR	Instruction register	R/W	*	*	*	*				
0	0	0	0	0	0	R ₀	Mode control I	W	*					*		
0	0	0	0	0	1	R ₁	Character pitch	R/W					*	*	*	*
0	0	0	0	1	0	R ₂	Number of characters (horizontal)	R/W								
0	0	0	0	1	1	R ₃	Number of duty	W								
0	0	0	1	0	0	R ₄	Character cursor form	R/W								
0	0	0	1	0	1	R ₅	Start address (lower)	R/W								
0	0	0	1	1	0	R ₆	Start address (upper)	R/W								
0	0	0	1	1	1	R ₇	Cursor address (lower)	R/W								
0	0	1	0	0	0	R ₈	Cursor address (upper)	R/W								
0	0	1	0	0	1	R ₉	Graphic cursor form (horizontal)	W								
0	0	1	0	1	0	R ₁₀	Graphic cursor form (vertical)	W	*	*	*					
0	0	1	0	1	1	R ₁₁	Horizontal imaginary screen	W								
0	0	1	1	0	0	R ₁₂	VP value extension	R/W				*	*	*	*	*
0	0	1	1	0	1	R ₁₃	Number of horizontal stops	W	*	*	*	*	*			
0	0	1	1	1	0	R ₁₄	Mode control II	W	*							
0	0	1	1	1	1	R ₁₅	Test	W	*	*	*	*	*	*		

Note 1: Mark * means the invalid data bit.

Note 2: The R/W shows whether only write from the CPU to the register is possible or both read and write are possible.

W : Only write is possible.

R/W: Both write and read are possible.

INTERNAL REGISTER

To select one unit of data register out of 16 units of data registers, it is necessary to write the address of the data register to be selected on the instruction register. The CPU carries out data transmission to the data register corresponding to the written address.

The array of the data registers is the same as MSM6255 from R₀ to R₈ so that software is compatible with that of MSM6255. The newly provided data registers are R₉ to R₁₅.

● Instruction Register (IR)

This register is used to specify the register number when accessing each data register.

This register is cleared when $\overline{\text{RES}}$ input is at "L" level. (That is, R₀ register is to be specified.)

● Mode Control I Register (R₀)

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Mode control I	0	*					*		

D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Output system	Mode
t B i n k O N / O F F	B i n k C u r s o r	B i n k C u r s o r	O N / O F F	D i s p l a y	0	0	8 bit parallel	Character
					1	0	4 bit parallel	Character
					0	1	8 bit parallel	Graphic
					1	1	4 bit parallel	Graphic

[查询"MSM6355"供应商](#)

● Horizontal Character Number Register (R2)

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Horizontal character number register	0	HN-1							

This register is used to specify the number of horizontal display characters (HN). A single character consists of eight dots. HN can be set up for 2 to 256 characters, so the maximum total number of horizontal dots is 256 characters x 8 dots/character = 2048 dots.

● Duty Number Register (R3)

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Duty number register	0	DN-1							

This register is set depending on the duty cycle of the LCD panel. The duty number (DN) can be set up for 2 to 256 and this can be extended up to 1024. Two bits of D₃ and D₄ of R₁₄ are prepared for extending the number of duty.

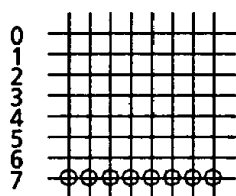
Note: Note that both the horizontal display character number and duty number must be set within the range of the maximum operating frequency of LCDC.

● Character Cursor Form Register (R4)

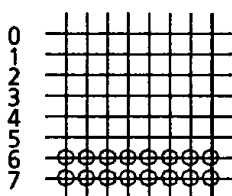
Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Character cursor form register	0	Cpu-1				Cpd-1			

In case of character mode, the cursor is displayed from the Cpu_{th} line to the Cpd line. The length of the cursor in the horizontal direction is equal to 8-pitch in the horizontal direction.

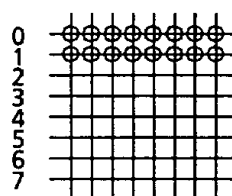
<Cursor form when VP = 8>



Cpu = 8
Cpd = 8



Cpu = 7
Cpd = 8



Cpu = 1
Cpd = 2

Note 1: Cpu, Cpd > Vp can not be set

Note 2: The cursor signal and pattern data are displayed after EX-OR is carried out.

Note 3: When extending Vp up for 17 to 32 (when the newly provided register R₁₂ is used), Cpu and Cpd values are used by using combination of D₇ and D₆ with register R₄.

- **Start Address (Lower) Register (R₅)**
Start Address (Upper) Register (R₆)

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Start address (lower) register	0	Start address (lower)							
Start address (upper) register	0	Start address (upper)							

This register is used to specify the read top address of the display memory. It is possible to carry out scrolling and paging by rewriting the register content.

- **Cursor Address (Lower) Register (R₇)**
Cursor Address (Upper) Register (R₈)

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Cursor address (lower) register	0	Cursor address (lower)							
Cursor address (upper) register	0	Cursor address (upper)							

This register is used to specify the cursor display position. The cursor appears at the position where the cursor address is matched with the memory address.

- **Graphic Cursor Register (Horizontal Direction) Register (R₉)**

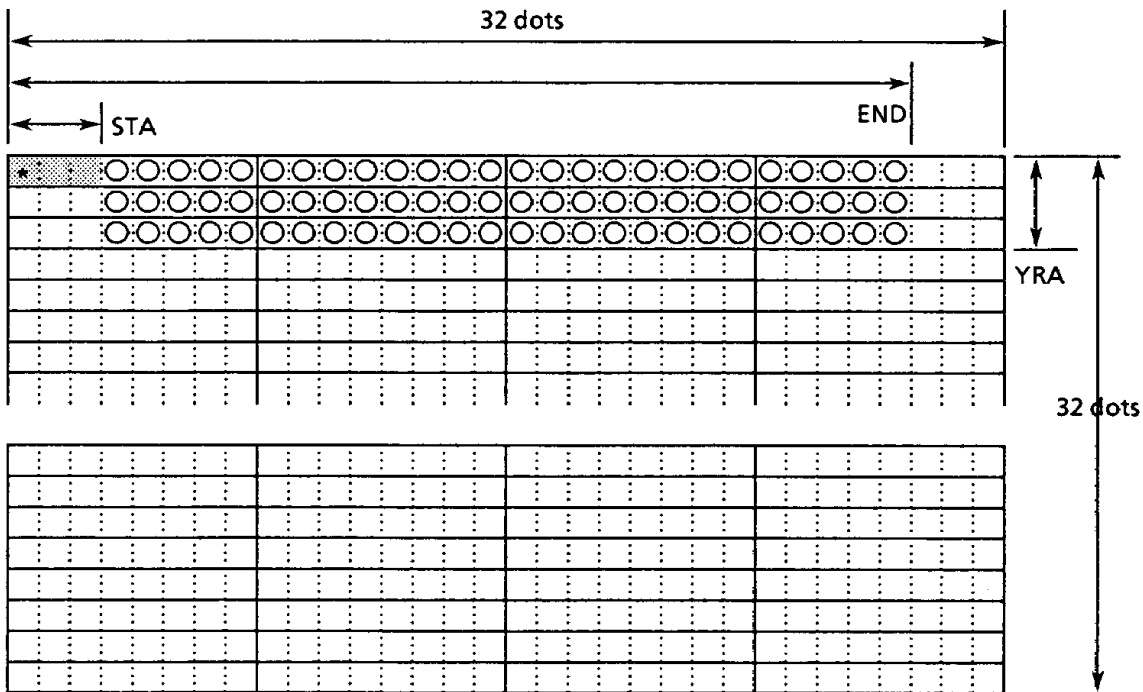
Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Graphic cursor form	0	END-1					STA-1		

This register is used to define the size of the cursor in the horizontal direction. It is possible to display the cursor in graphic mode. The cursor can be displayed with dots ranging from the STA dot to the END dot. The maximum number STA dot to the END dot of display dots in the horizontal direction is 32 (dots).

- **Graphic Cursor Register (Horizontal Direction) Register (R₉)**

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Graphic cursor form	0	*	*	*	YRA-1				

This register is used to define the size of the cursor in the horizontal direction. It is possible to display the cursor in the graphic mode. The cursor can be displayed with dots ranging from the STA dot to the END dot. The maximum number STA dot to the END dot of display dots in the horizontal direction is 32 (dots).



The example of the graphic cursor display (STA = 4, END = 27, YRA = 3)

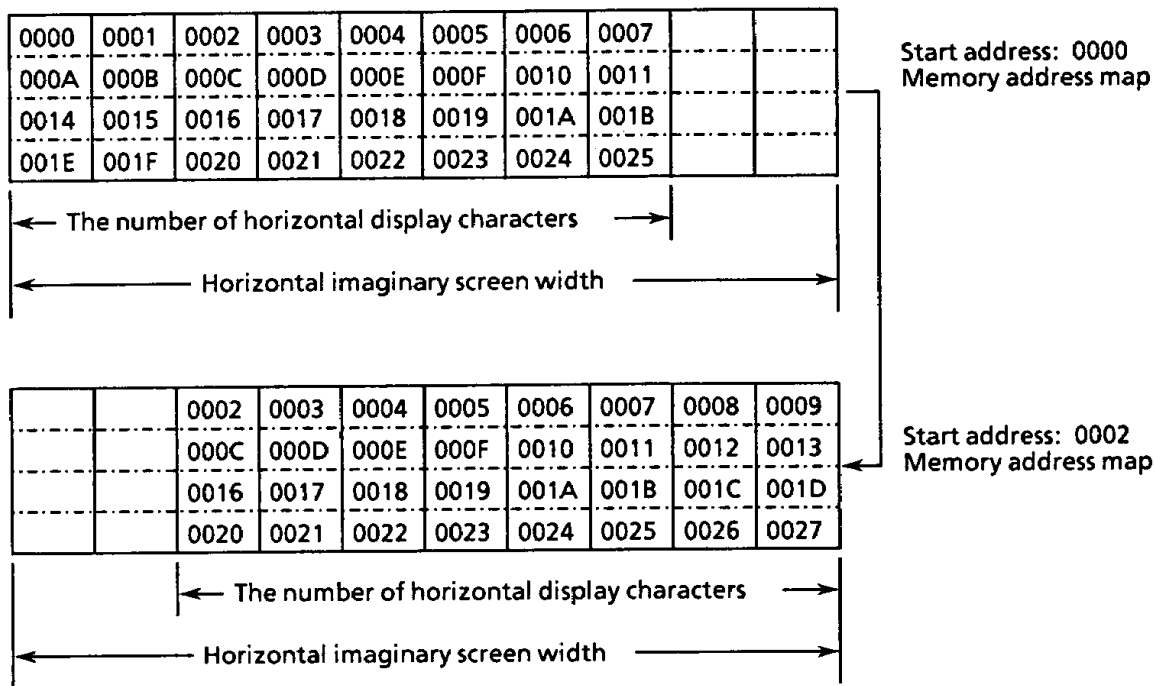
The above figure shows the example in which E3 is set to register R₉ to 02 to register R₁₀.

Note: The graphic cursor can be displayed only in two screen display mode and can not be displayed in one screen display mode.

● Horizontal Imaginary Screen Register (R₁₁)

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Horizontal imaginary register	0	HIN-1							

This register is used to specify the top address of the next line by setting the screen width in the horizontal direction on the character unit basis. It is possible to scroll the display in the horizontal direction by setting the horizontal imaginary screen larger than the display width.



This figure shows the example of horizontal scrolling in case of horizontal display characters; 8, horizontal imaginary screen width; 10 characters, number of duty; 4, and in one screen display mode.

● VP Value Extension Register (R₁₂)

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
VP value extension register	0	Cpu4	Cpd4	Vp4	0	0	0	0	0

(1) Cpu4 and Cpd4

It is possible to extend the cursor form using bits D₇ and D₆. This register is used by combination with register R₄ when the VP value is more than 17.

(2) Vp4

It is possible to extend the VP value using bit D₅.

Vp4 : 1 VP = 17~32

Vp4 : 0 VP = 1~16

Note: The "0" must be written into bits D₄ to D₀ each. If data except "0" is written, the character cursor can not be displayed at a correct position.

● **Horizontal Stops Number Register (R₁₃)**

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Horizontal stops register	0	*	*	*	*	*	HST-1		

This register is used to set the shift clock stop duration (HST) in the horizontal direction on the character unit basis. It is possible to carry out fine adjustment of the frame frequency by setting HST optionally up for 1 to 8 characters.

● **Mode Control II Register (R₁₄)**

Register Name	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Mode control II register	0	*	HS	Vpj	Du9	Du8	Skew	U/L	Steal

(1) HS

This is the bit for setting the horizontal imaginary screen width:

HS:1 When setting the horizontal imaginary screen width, it is necessary to set HS = 1.

HS:0 Even if the horizontal imaginary screen width is set, it is invalid, and the set value on the number of horizontal characters has top priority.

(2) Vpj

This bit is set when the display screen has odd number of lines in character mode:

Vpj:1 To be set for odd number of lines on the display screen.

Vpj:0 To be set for even number of lines on the display screen (Note that in case of one screen display, it is unnecessary to specify the bit.)

(3) Du9, Du8

This bit is set in combination with register R₃ when extending the number of duty.

Du9	Du8	Duty
0	0	2 ~ 256
0	1	257 ~ 512
1	0	513 ~ 768
1	1	769 ~ 1024

(4) Skew

This bit is used to set whether the skew function is to be provided or not:

Skew:0 The skew function is provided

Skew:0 The skew function is not provided

Refer to "Skew Function" for details

(5) U/L

This bit is used to specify whether vertical division of the LCD panel is to be provided or not.

U/L:1 One screen display

U/L:0 Two screen display

Note: In case of 8 bit parallel output system, only one screen display is possible. Even if two screen display mode is set, the IC automatically selects one screen to be displayed.

(6) Steal

This bit is used to set whether the cycle steal function is to be provided or not:

Steal:1 The cycle steal function is provided

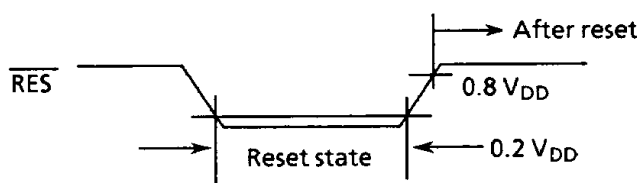
Steal:0 Input the switch over signal of the address bus to DIEN input terminal from external.

Note 1: When using the cycle steal function, connect DIEN terminal to V_{DD} or GND.

Note 2: When using no cycle steal function, connect MRD and MWR terminals to V_{DD} or GND.

RESET

The $\overline{RES}$ terminal is used to determine the internal state of LCDC including the counter, register and so on. Since the data register of MSM6355 contains the test mode, it is needed to reset LCDC basically. When $\overline{RES}$ terminal is not used, it is needed to write zero(0) into bits D_1 and D_0 of register R_{15} .



● The Reset State of the Register

The newly provided data register is affected by reset. The reset state of the data register is shown below.

- (1) Graphic cursor form(horizontal) (R_9) = 38(H)
End = 8 and STA = 1 are set.
- (2) Graphic cursor form(vertical) (R_{10}) = 00(H)
YRA = 1 is set.
- (3) Horizontal imaginary screen(R_{11}) = (R_2)
HIN = HN is set.
- (4) VP valu extension (R_{12}) = 00(H)
Cpu4 = 0 and Cpd = 0 are set.
- (5) Number of horizontal stops(R_{13}) = 07(H)
HST = 8 is set.
- (6) Mode control II(R_{14}) = 00(H)
Two screen diaplay is set.
- (7) Test(R_{15}) = 00(H)
- (8) Instruction (IR) = 00(H)
Mode control(I) is specified.

● The Reset State of the Output Terminal

- (1) To be fixed at "L" level.
FRMB, LIP, FRP, $CE\phi$, $RA_0 \sim RA_4$, RDY, $MA_0 \sim MA_{15}$, $UD_3 \sim UD_0$, $LD_3 \sim LD_0$, CLP
- (2) To be fixed at "H" level.
 $\overline{WE}$, $\overline{RE}$
- (3) Not to be affected
 $DB_7 \sim DB_0$

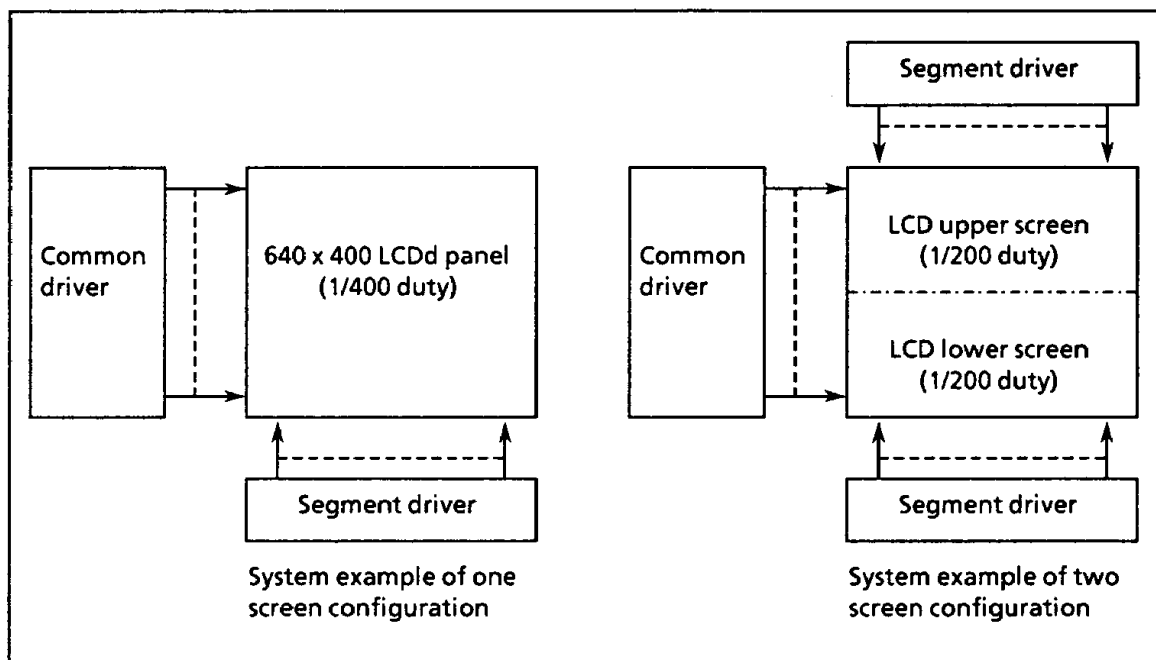
LCD DISPLAY SYSTEM CONFIGURATION

The LCDC provides the following modes as the system configuration of the LCD display.

- (1) Screen configuration: One or two screen display
- (2) Data transmission: 4 or 8bit data transmission

● Screen Configuration

The one screen configuration requires only half of the segment drivers for the two screen configuration. So, the system configuration is achieved at low cost. But, in case of a large number of display dots in the vertical direction, the duty cycle is low resulting in limit of cost reduction. In this case, the two screen configuration is more effective

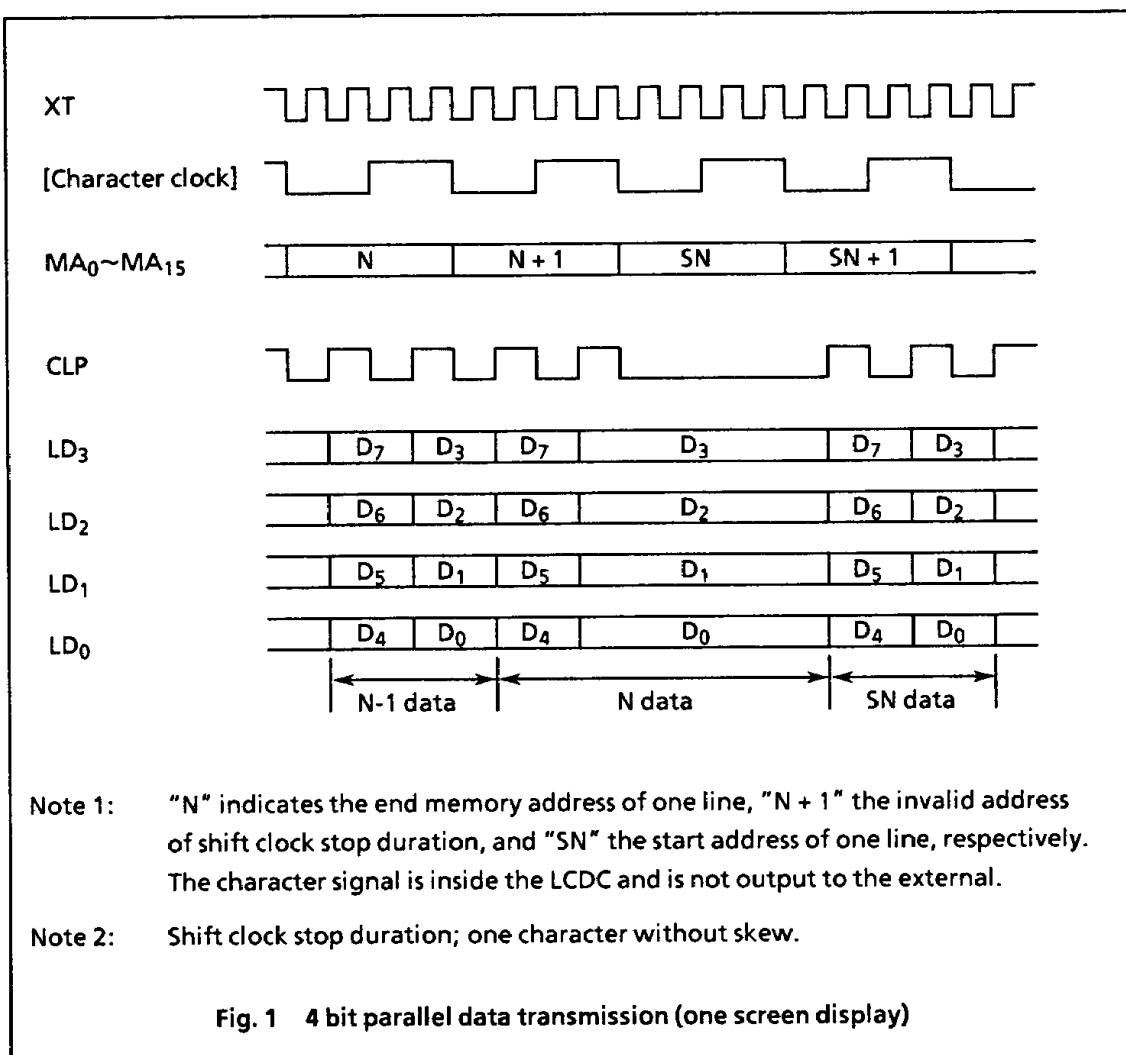


● Data Transmission

When transmitting the data to the segment driver, there are two kinds of transmission systems, 4bit parallel data transmission and 8bit parallel transmission. The 8bit parallel data transmission is half the speed compared with the 4 bit parallel data transmission.

● The Power Down Function of the LCD Driver

It is possible to select the MSM5279GS chip by connecting the output terminal of $CE\phi$ to the ECLK input of MSM5279GS. It is unnecessary to connect it to the MSM5299BGS which counts the internal shift clock of LCD driver.



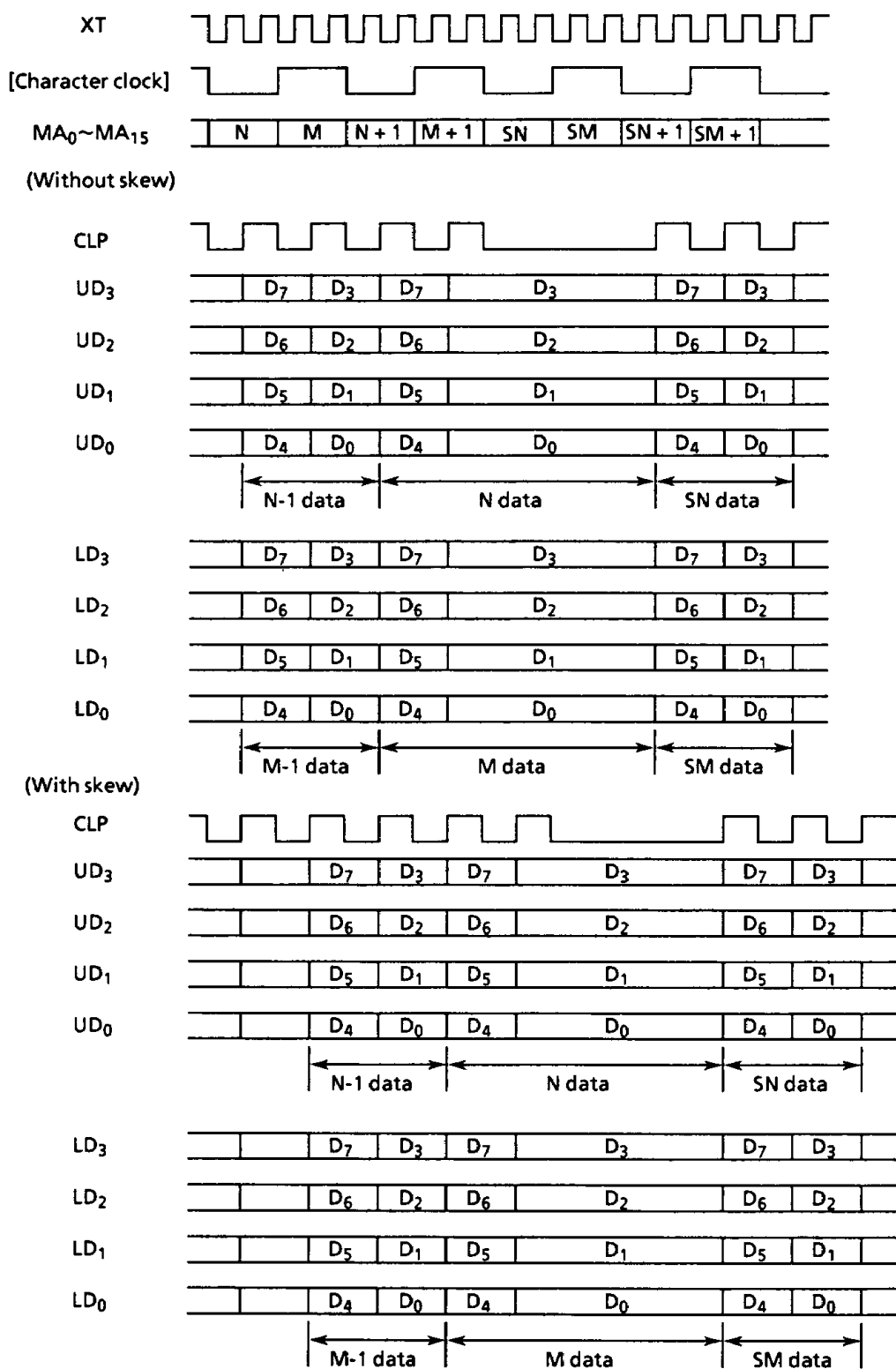
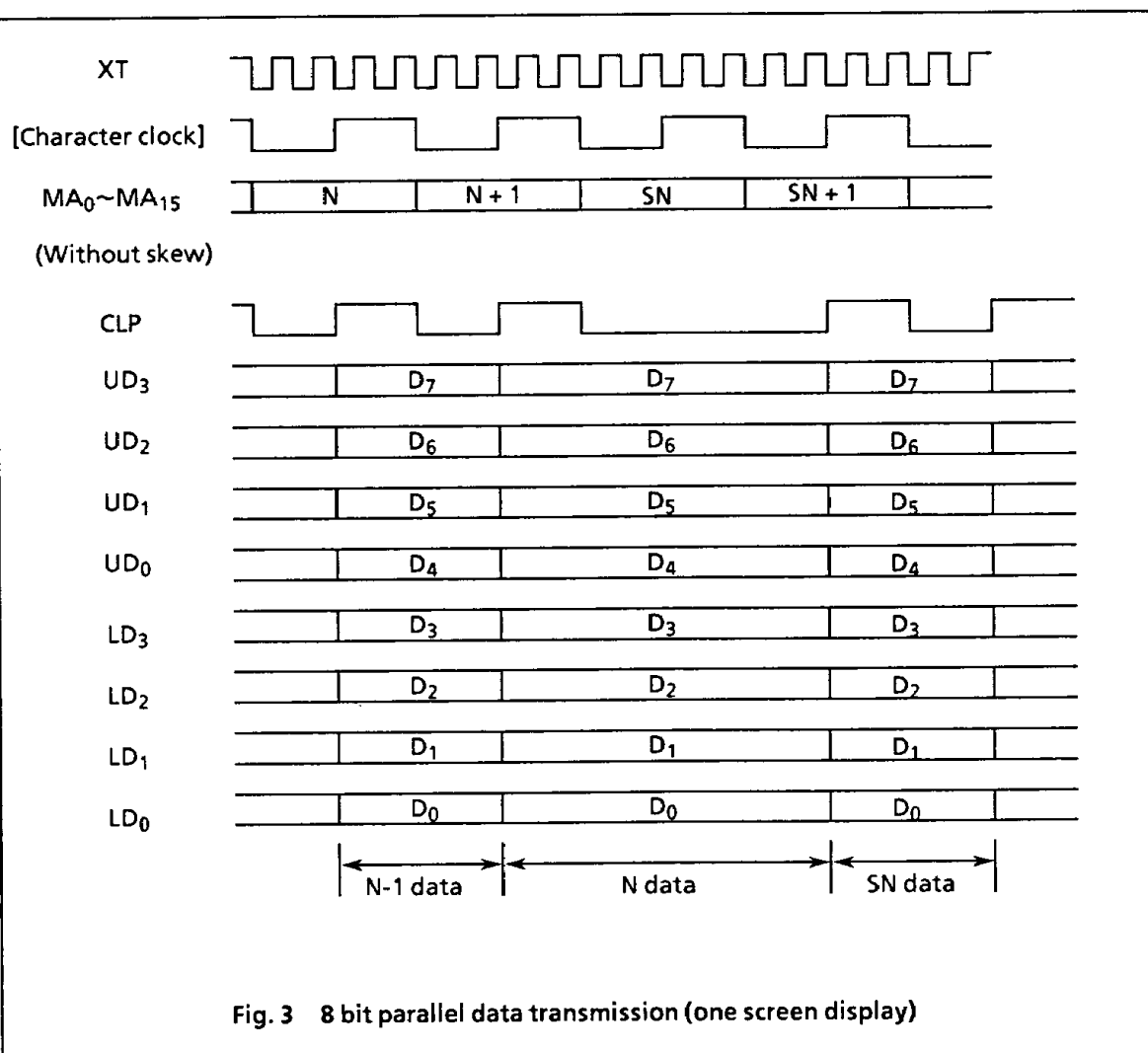
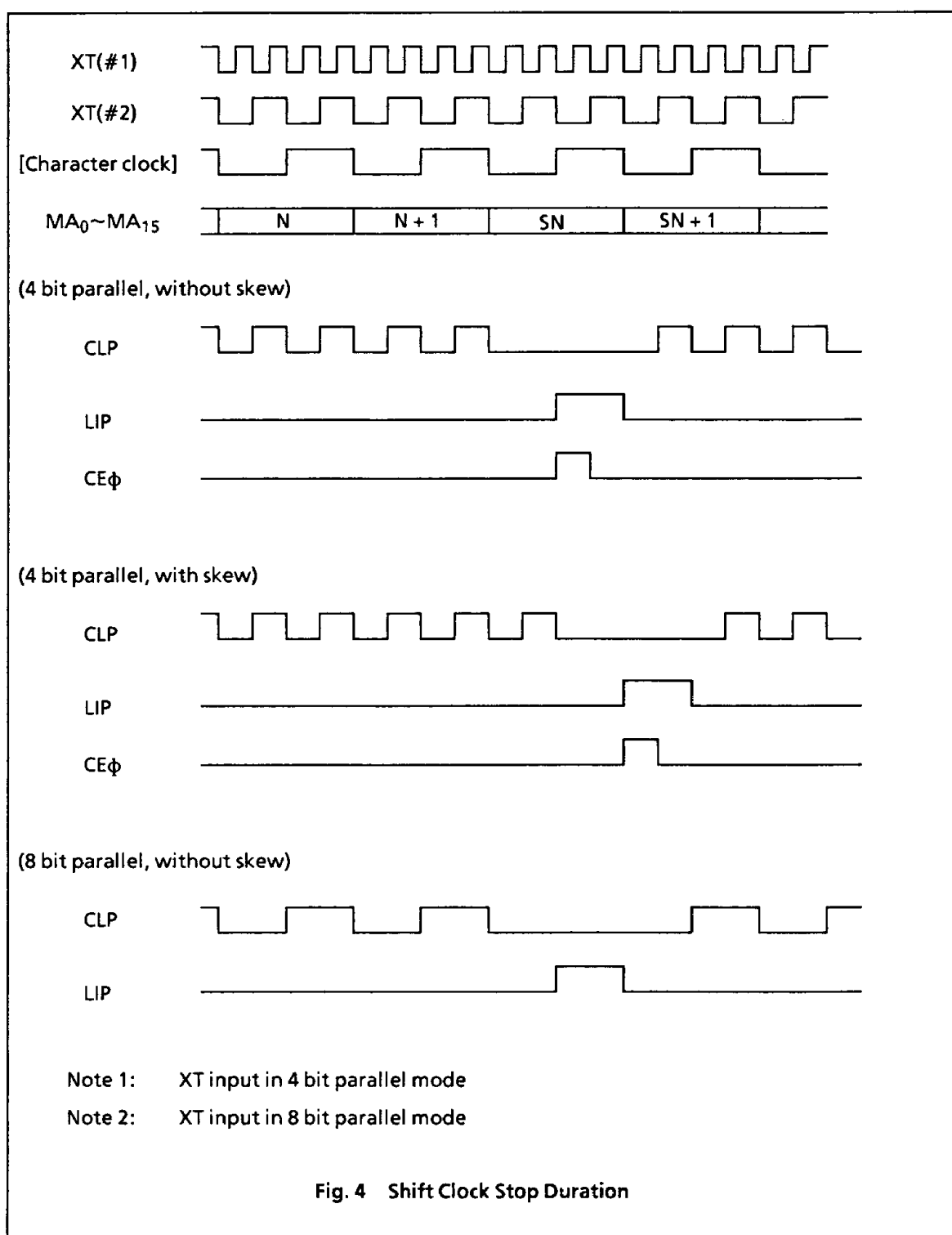
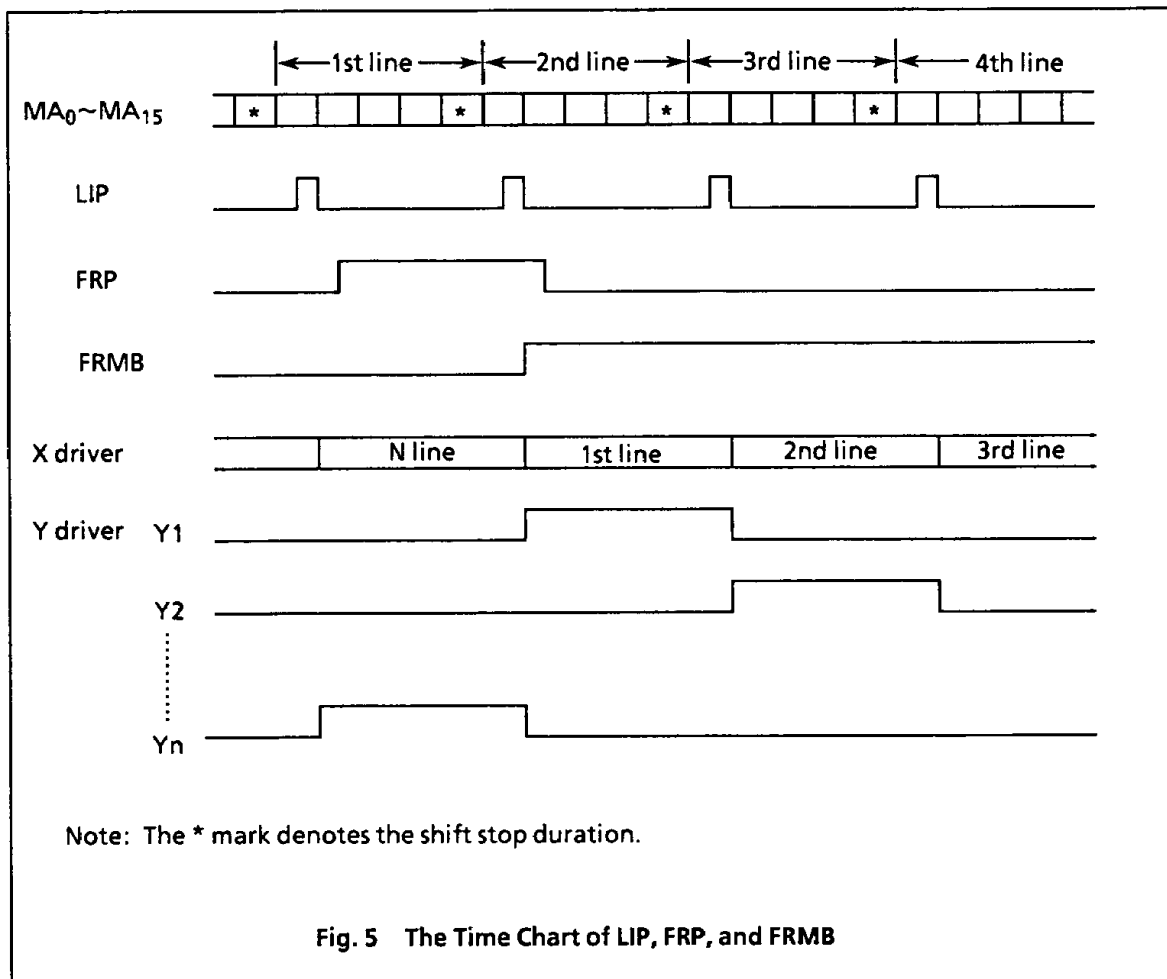


Fig. 2 4 bit parallel data transmission (two screen display)





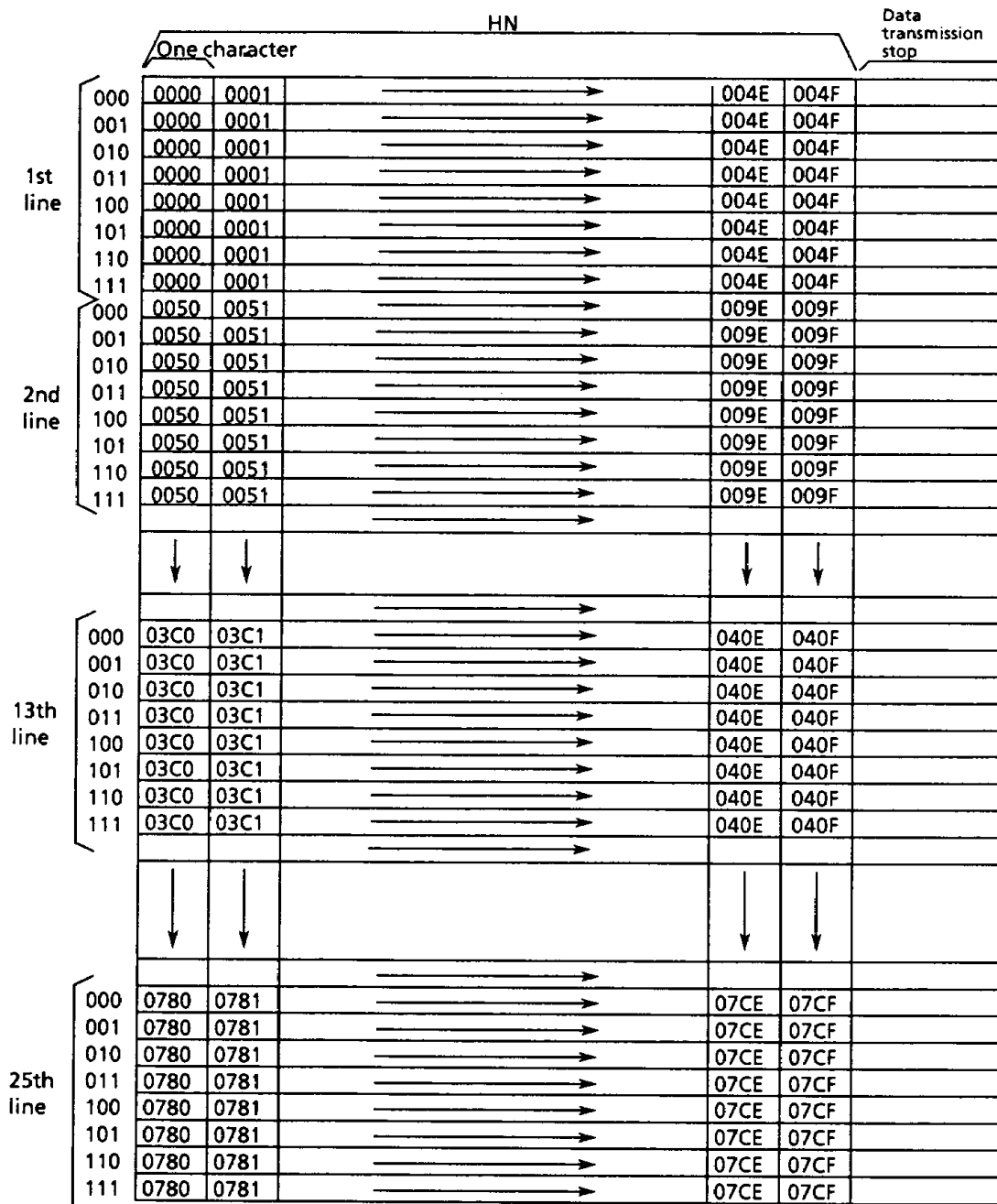


OPERATION OF REFRESH MEMORY ADDRESS (MA₀~MA₁₅)

MA_x is counted up even over the number of horizontal display characters, but this does not affect the display because of the data transmission is stop duration.

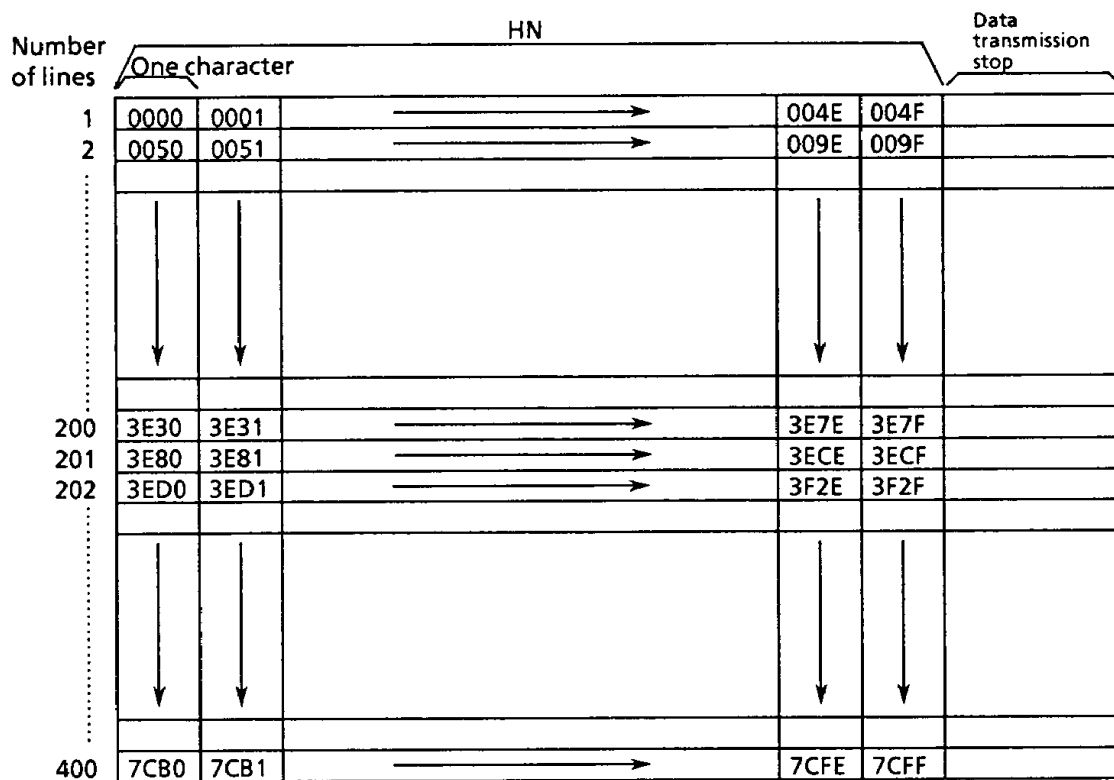
The data transmission stop duration is 1 character to 8 characters, and after the duration one cycle ends and the next cycle starts.

The figure 6 shows the memory address in character mode, and the figure 7 the memory address in graphic mode.



Note: Start address: 0000, HN: 80 characters, DN: 100 or 200, VP: 8

Fig. 6 Character Mode (80 characters x 25 lines)



Note: Start address: 0000, HN: 80 characters, DN: 200 (two screen display) or 400 (one screen display)

Fig. 7 The Memory Address in Graphic Mode (640 x 400)

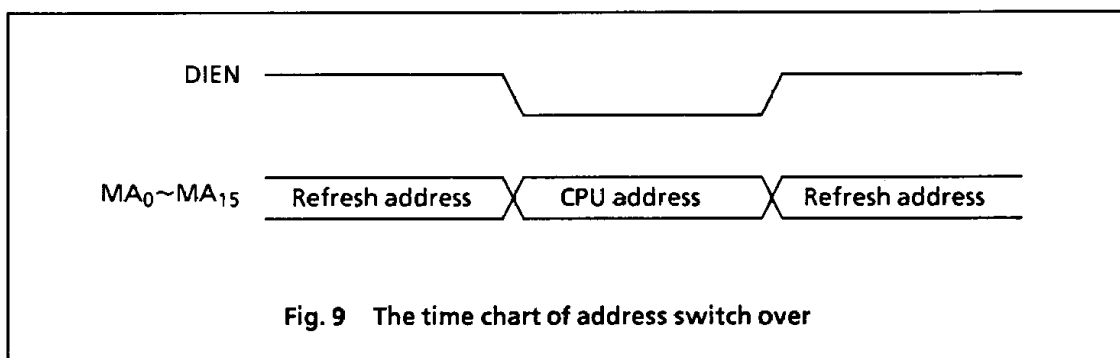
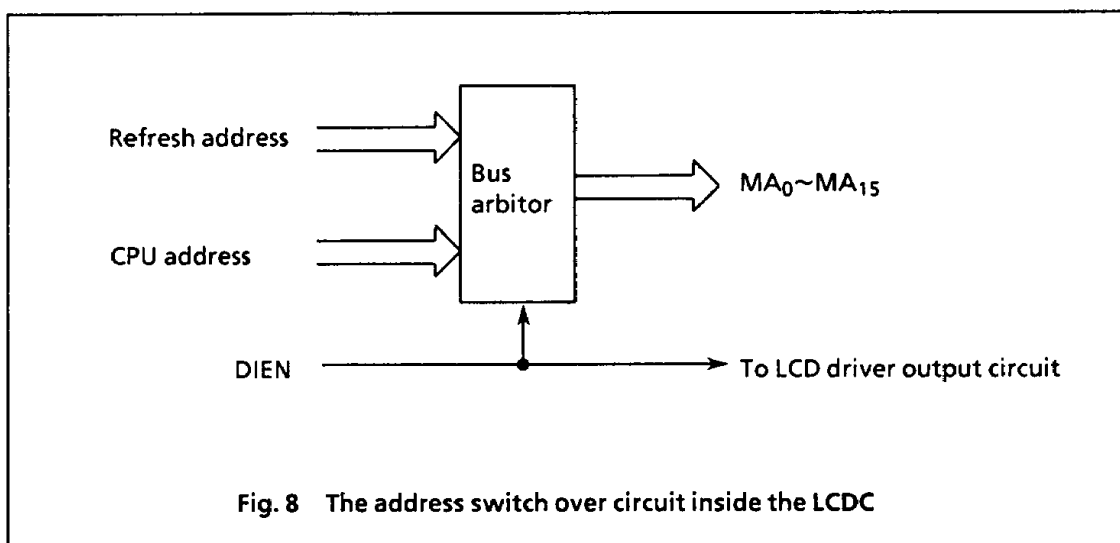
ACCESSING THE DISPLAY RAM

When accessing the display RAM from CPU, there are two kinds of access methods; the CPU priority method and the synchronized access method (cycle steal).

● CPU Priority Method

This method is to access the display RAM directly from CPU regardless of the refresh operation of LCD controller. In this case, the address of the display RAM is switched over to the CPU address during display, so frequent access to the display RAM may cause flickering of the display.

Set D_0 of register R_{14} to "0" and switch over the address bus using DIEN terminal.



The switch-over between the refresh address and the CPU address is carried out using DIEN signal. When DIEN terminal goes "L" level, the CPU address is output to MA_0 through MA_{15} terminals, and the output circuit is controlled so that the display is turned off while DIEN signal is being at "L" level. This is done to reduce the effects on the display.

● Synchronized Access Method

(1) Outline

This method is used to synchronize the CPU access to the display RAM with the LCD controller refresh access cycles. The LCD controller outputs the $\overline{WE}$, $\overline{RD}$ and address signals to the display RAM without affecting the refresh access. This allows an uninterrupted flow of data to the display panel which provides a clean flicker free display.

To set the synchronized access mode, set bit D0 of register R14 to "1". Table 2 shows the necessary signals for synchronized access.

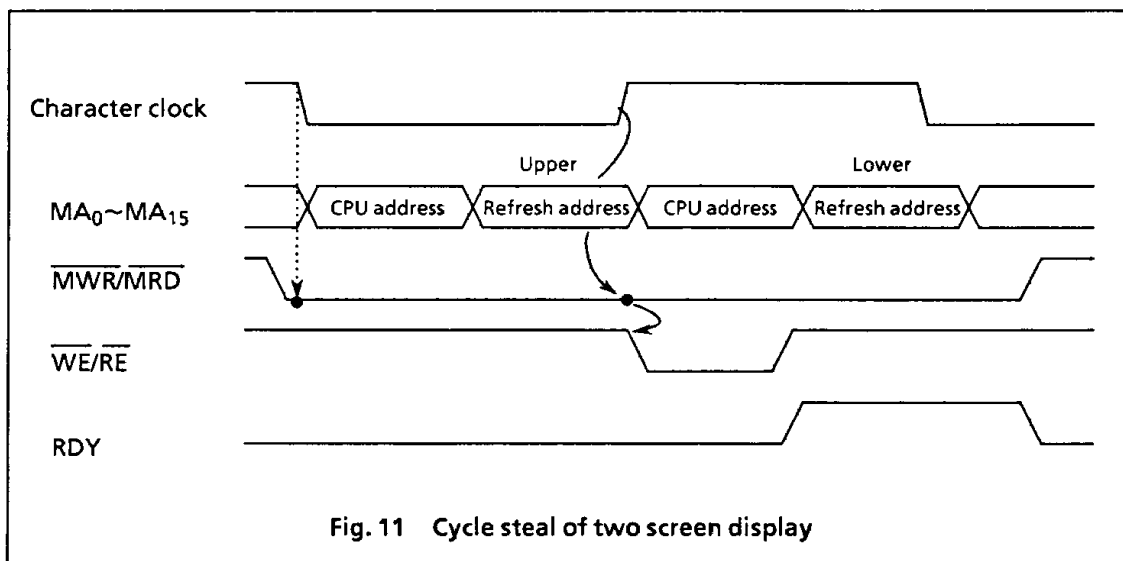
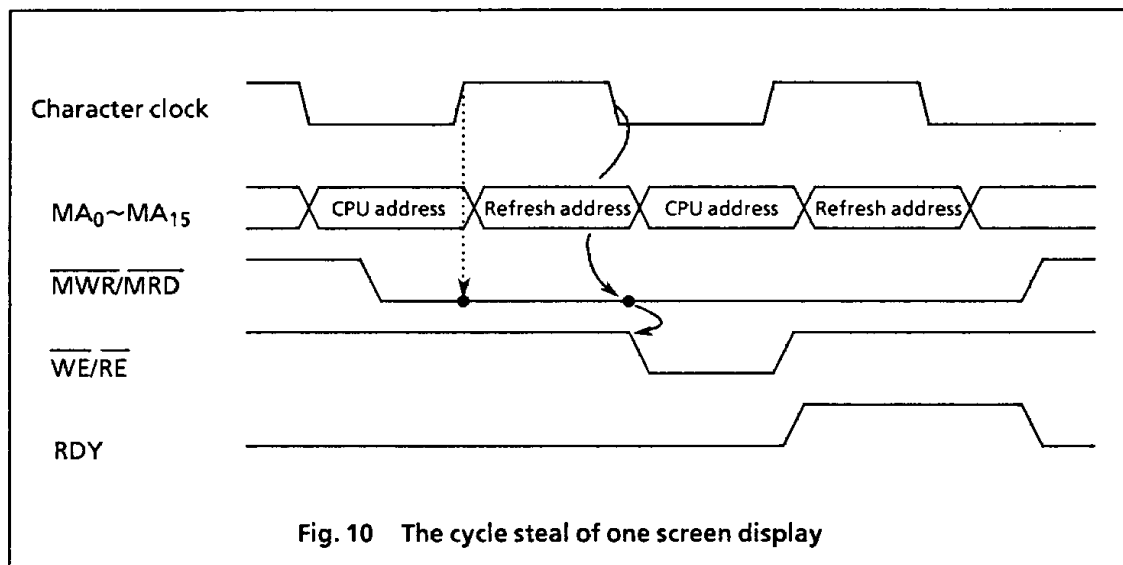
Table 2 The signals required for synchronized access

$\overline{MWR}$	Display RAM write signal input from the CUP. Connect to VDD or GND when not used.
$\overline{MRD}$	Display RAM read signal input from the CPU. Connect to VDD or GND when not used.
$\overline{WE}$	Display RAM write signal output to the display memory. The $\overline{MWR}$ input is regenerated gets gated on this pin during the proper time for synchronized access.
$\overline{RE}$	Display RAM read signal output to the display memory. The $\overline{MRD}$ input is regenerated and gets gated on this pin during the proper time for synchronized access.
RDY	Ready output to the CPU. This signal is used to tell the CPU to return from its needed wait state after the access cycle has completed.

(2) Description of operation

When the LCD controller is set to the cycle steal mode, it maintains active refresh cycles from the display RAM to the display panel. A synchronized access cycle is initiated by the CPU when activating the $\overline{MWR}$ or $\overline{MRD}$ signal. For a single screen display the CPU access cycle is 1/2 of the character clock cycle. For a two screen display the CPU access cycle is 1/4 of the character clock cycle.

If the $\overline{MWR}/\overline{MRD}$ is brought to "L" level by the CPU the LCD controller synchronizes the $\overline{WE}$, $\overline{RE}$ and address signals to the display RAM with the character clock. At the end of the cycle $\overline{WE}/\overline{RE}$ return to "H" level and the RDY signal outputs a "H" level to the CPU enabling the CPU to resume from the wait. The RDY signal returns low after the CPU brings $\overline{MWR}/\overline{MRD}$ back to "H" level. The $\overline{WE}/\overline{RE}$ signals can also be used for the proper gating required by an external 8-bit data buffer which is needed for the display memory data Buss.



Note: In the one screen display, "L" level of the $\overline{\text{MWR}}/\overline{\text{MRD}}$ signal is detected when the character clock rises, and "L" level is output to the $\overline{\text{WE}}/\overline{\text{RE}}$ terminal when the next character clock falls.

In the two screen display, "L" level of the $\overline{\text{MWR}}/\overline{\text{MRD}}$ signal is detected when the character clock falls, and "L" level is output to the $\overline{\text{WE}}/\overline{\text{RE}}$ terminal when the next character clock rises.

"H" level of $\overline{\text{MWR}}/\overline{\text{MRD}}$ needs one more cycle of the character clock.

SKEW FUNCTION

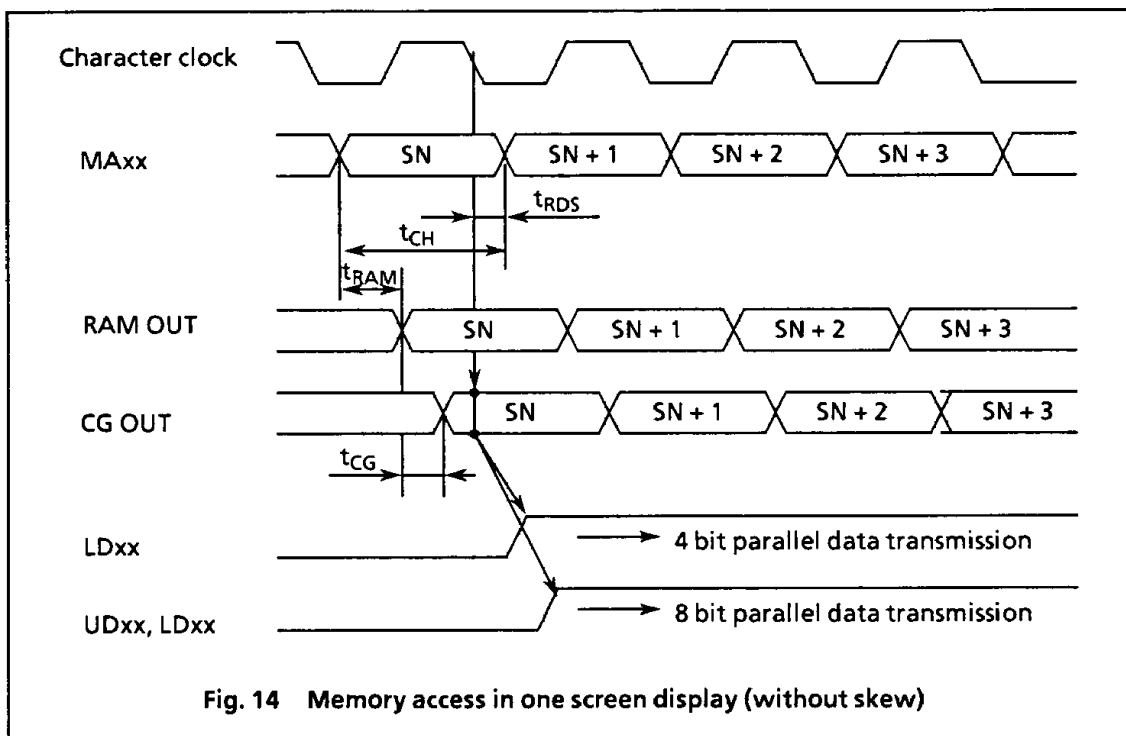
In the system that controls the large screen LCD panel, it is difficult to access both the display RAM and CGROM within the horizontal one character time since one cycle of the character clock is short.

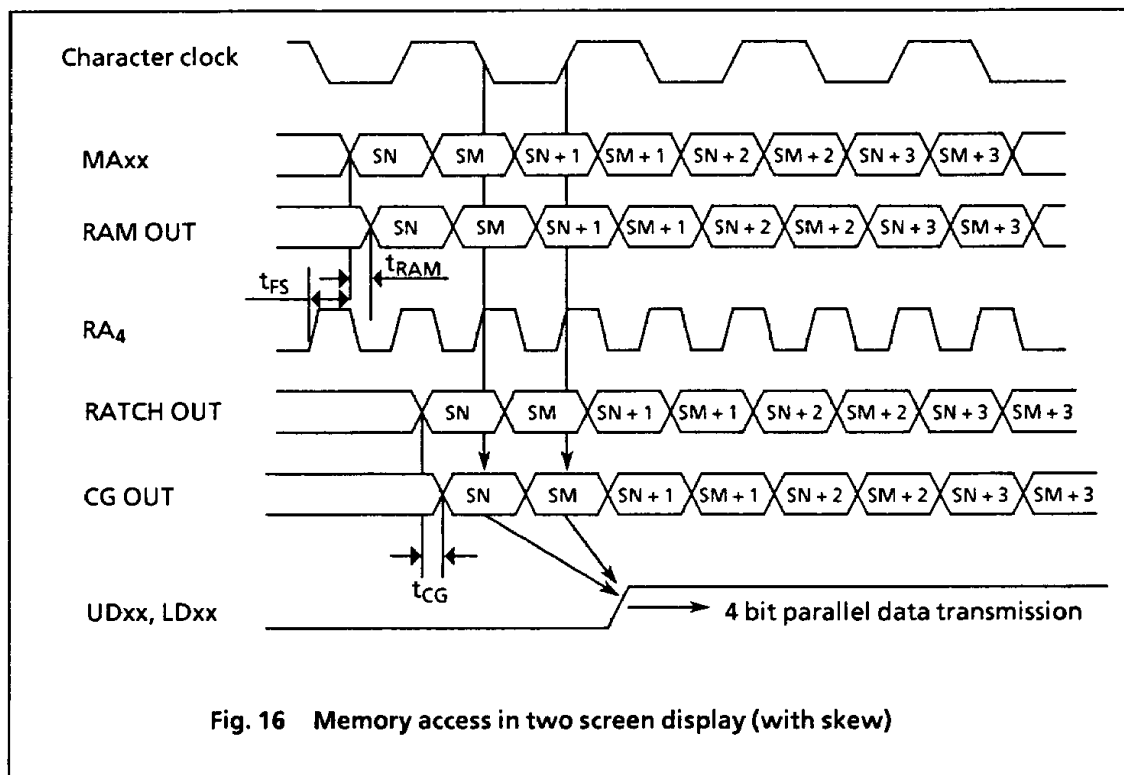
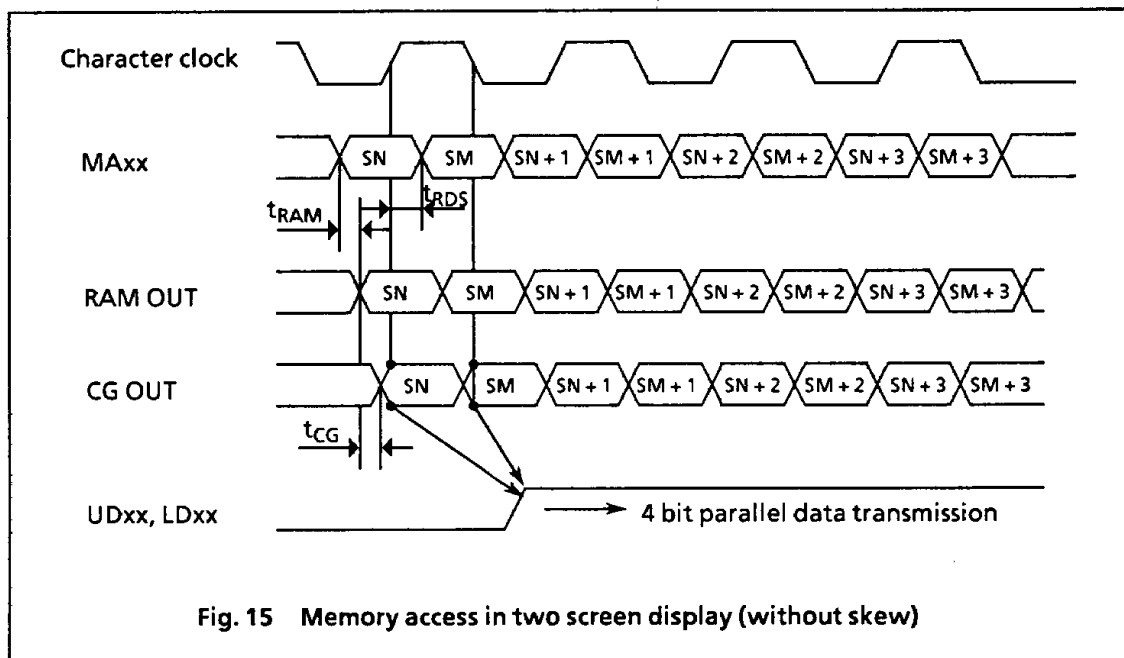
In this case, as shown in the figure 13 the method that latches the data on the display RAM once and accesses CGROM in the next cycle(skew function) is used. Since the signal for latching is output from RA₄, the maximum value of VP is limited to 16 when skew function is used. The calculation to judge whether the skew function is to be used or not is done based on the calculation formulas in the Table 3.

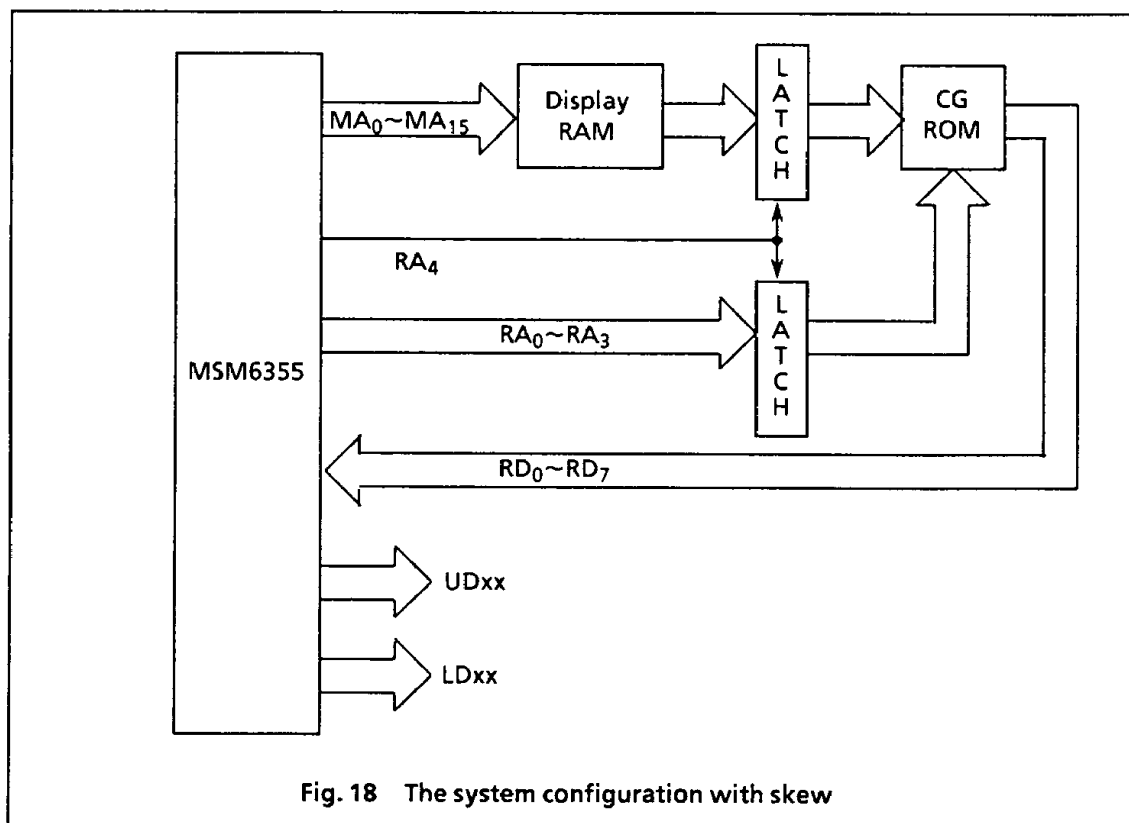
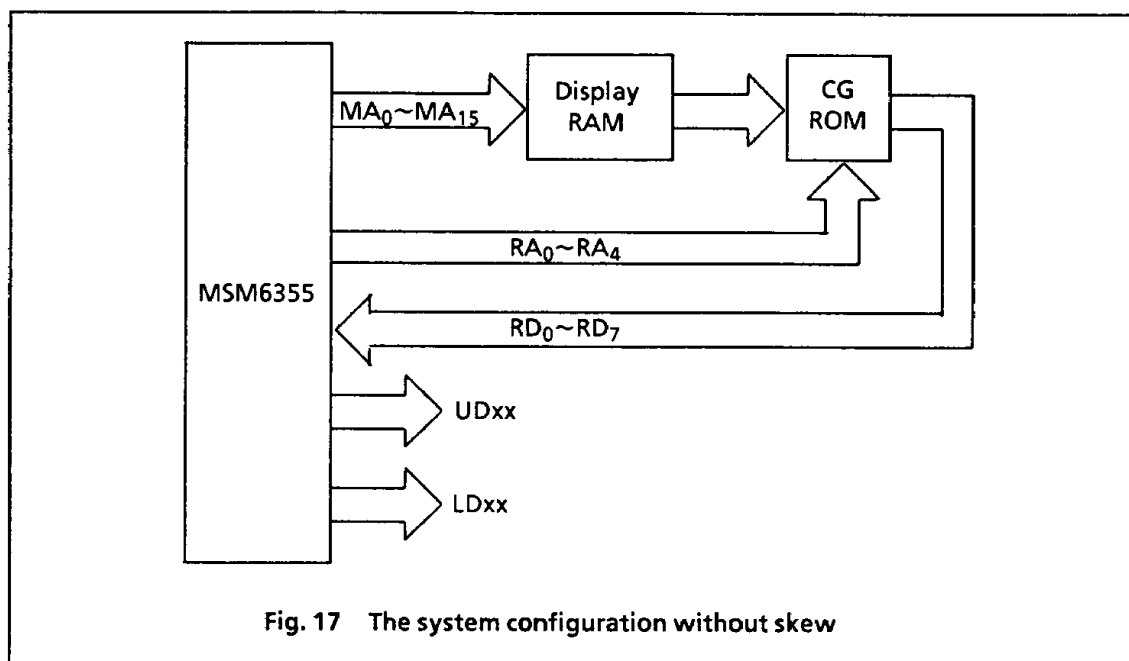
Table 3 Calculation formulas of memory time

Skew funciton	Calculation formula	Screen configuration
Not provided	$t_{CH} > t_{RAM} + t_{CG} + t_{RDS}$	One screen display
	$t_{CH}/2 > t_{RAM} + t_{CG} + t_{RDS}$	Two screen display
Provided	$t_{CH}/2 > t_{RAM} + t_{FS}$ $t_{CH}/2 > t_{CG}$	Two screen display

Note: The setup time and delay time of latch are disregarded.
When choosing one screen display, the skew function can not be used.







CALCULATION OF THE BASE OSCILLATION FREQUENCY (f_{OSC})

The base oscillation frequency is the same regardless of whether crystal oscillation is used or when an external clock is used.

Table 4 Base oscillation calculation formulas

Output system	Formula f_{OSC}	Calculation example (MHz)
4 bit parallel	$FRP \times (HN + HST) \times DN \times 4$	9.856
8 bit parallel	$FRP \times (HN + HST) \times DN \times 2$	4.928

Note: The calculation examples in Table 4 are based on $FRP = 70$ Hz, $HN = 80$ characters, $HST = 8$ characters, and $DN = 400$.

CALCULATION OF THE SHIFT CLOCK (CLP)

The calculation formulas of the shift clock for display data re shown in Table 5.

Table 5 Shift clock frequency calculation formulas

Output system	Formula f_{OSC}	Calculation example (MHz)
4 bit parallel	$FRP \times (HN + HST) \times DN \times 2$	4.928
8 bit parallel	$FRP \times (HN + HST) \times DN$	2.464

Note: The calculation examples in Table 5 are based on $FRP = 70$ Hz, $HN = 80$ characters, $HST = 8$ characters, and $DN = 400$.

CALCULATION OF CHARACTER CLOCK (CHO)

The character clock is the basic internal IC clock which is used as the clock of the refresh memory address counter.

In the system that displays a large screen LCD panel, it is necessary to calculate the frequency of the character clock in order to judge whether it is possible to access the display RAM and CGRAM sufficiently. The formula for calculating the frequency of the character clock is shown below.

$$f(\text{CH}\phi) = \text{FRP} \times (\text{HN} + \text{HST}) \times \text{DN}$$

The calculation examples are shown in Table 6.

Table 6 Calculation examples of character clock

$f(\text{CH}\phi)$ (MHz)	FRP (Hz)	HN (character)	HST (character)	DN
0.567	70	80	1	100
1.134	70	80	1	200
2.268	70	80	1	400

Note: The same calculation formula of character clock is used for both the 4 bit parallel and 8 bit parallel modes.

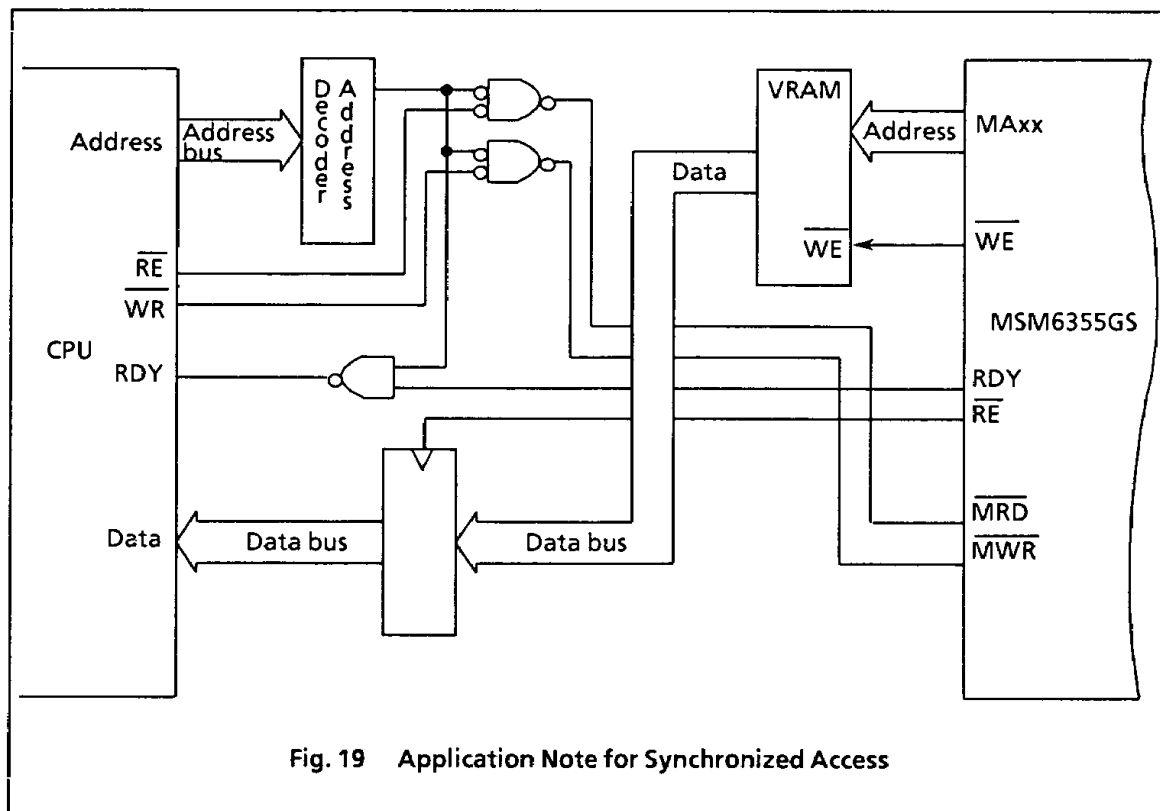


Fig. 19 Application Note for Synchronized Access