19-5450; Rev 0; 7/10

3.3V, 8Mb, Nonvolatile SRAM with Clock

General Description

The DS3065WP consists of a static RAM, a nonvolatile (NV) controller, and a real-time clock (RTC). These components are packaged on a surface-mount substrate and require post-assembly attachment of a DS9034I-PCX+ battery cap. Whenever V_{CC} is applied to the module, it powers the clock and SRAM from the external power source, and allows the contents of the clock registers or SRAM to be modified. When V_{CC} is powered down or out of tolerance, the controller write protects the memory contents and powers the clock and SRAM from the battery.

Applications

RAID Systems and Servers/Gaming

POS Terminals/Fire Alarms

Industrial Controllers/PLCs

Data-Acquisition Systems

Routers/Switches

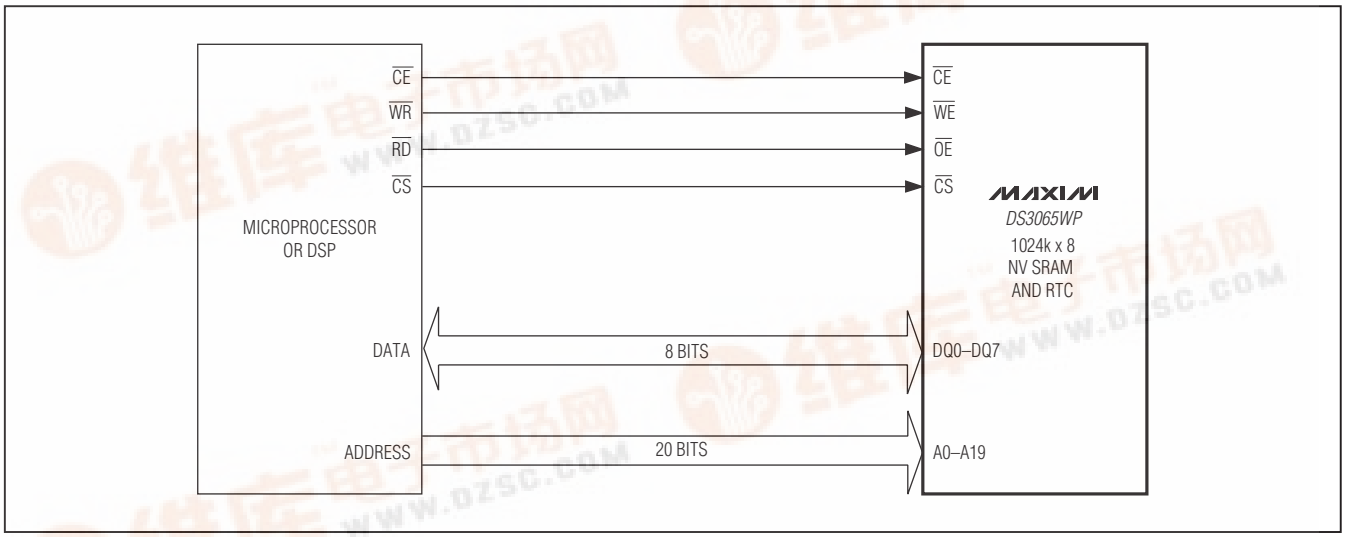
Features

- **Reflowable, 34-Pin PowerCap Package**
- **Integrated RTC**
- **Unconditionally Write Protects the Clock and SRAM When V_{CC} is Out of Tolerance**
- **Automatically Switches to Battery Supply When V_{CC} Power Failures Occur**
- **Extended Industrial Temperature Range (-40°C to +85°C)**
- **Underwriters Laboratories Recognized**

Ordering Information

PART	TEMP RANGE	SPEED (ns)	SUPPLY VOLTAGE (V)	PIN-PACKAGE
DS3065WP-100IND+	-40°C to +85°C	100	3.3 ±0.3	34 PowerCap Module

Typical Operating Circuit



3.3V, 8Mb, Nonvolatile SRAM with Clock

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground ....-0.3V to +4.6V
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+260°C
(intended for minor rework/touchup purposes only)
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Logic 1 Input	V_{IH}		2.2		V_{CC}	V
Logic 0 Input	V_{IL}		0.0		0.4	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}		-1.0		+1.0	µA
I/O Leakage Current	I_{IO}	$V_{\overline{CE}} = V_{\overline{CS}} = V_{CC}$	-1.0		+1.0	µA
Output-Current High	I_{OH}	V_{OH} = 2.4V	-1.0			mA
Output-Current Low	I_{OL}	V_{OL} = 0.4V	2.0			mA
Standby Current	I_{CCS1}	$V_{\overline{CE}} = V_{\overline{CS}}$ = 2.2V		0.6	2.0	mA
	I_{CCS2}	$V_{\overline{CE}} = V_{\overline{CS}} = V_{CC}$ - 0.2V		0.6	1.5	
Operating Current	I_{CCO1}	t_{RC} = 200ns, outputs open			50	mA
Write-Protection Voltage	V_{TP}		2.8	2.9	3.0	V

PIN CAPACITANCE

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}	Not production tested		15		pF
Input/Output Capacitance	C_{OUT}	Not production tested		15		pF

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle Time	t_{RC}		100			ns
Access Time	t_{ACC}				100	ns
$\overline{OE}$ to Output Valid	t_{OE}				50	ns
RTC $\overline{OE}$ to Output Valid	t_{OEC}				60	ns
$\overline{CE}$ or $\overline{CS}$ to Output Valid	t_{CO}				100	ns
$\overline{OE}$ or $\overline{CE}$ or $\overline{CS}$ to Output Active	t_{COE}	(Note 2)	5			ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V ±0.3V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Impedance from Deselection	t_{OD}	(Note 2)			40	ns
Output Hold from Address	t_{OH}		5			ns
Write Cycle Time	t_{WC}		100			ns
Write Pulse Width	t_{WP}	(Note 3)	75			ns
Address Setup Time	t_{AW}		0			ns
Write Recovery Time	t_{WR1}	(Note 4)	5			ns
	t_{WR2}	(Note 5)	20			
Output High Impedance from $\overline{WE}$	t_{ODW}	(Note 2)			40	ns
Output Active from $\overline{WE}$	t_{OEW}	(Note 2)	5			ns
Data Setup Time	t_{DS}	(Note 6)	40			ns
Data Hold Time	t_{DH1}	(Note 4)	0			ns
	t_{DH2}	(Note 5)	20			
Chip-to-Chip Setup Time	t_{CCS}		40			ns

POWER-DOWN/POWER-UP TIMING

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fail Detect to $\overline{CE}$, $\overline{CS}$, and $\overline{WE}$ Inactive Time	t_{PD}	(Note 7)			1.5	µs
V_{CC} Slew from V_{TP} to 0V	t_F		150			µs
V_{CC} Slew from 0V to V_{TP}	t_R		150			µs
V_{CC} Valid to $\overline{CE}$, $\overline{CS}$, and $\overline{WE}$ Inactive	t_{PU}				2	ms
V_{CC} Valid to End of Write Protection	t_{REC}				125	ms

DATA RETENTION

(T_A = +25°C, unless otherwise noted.)

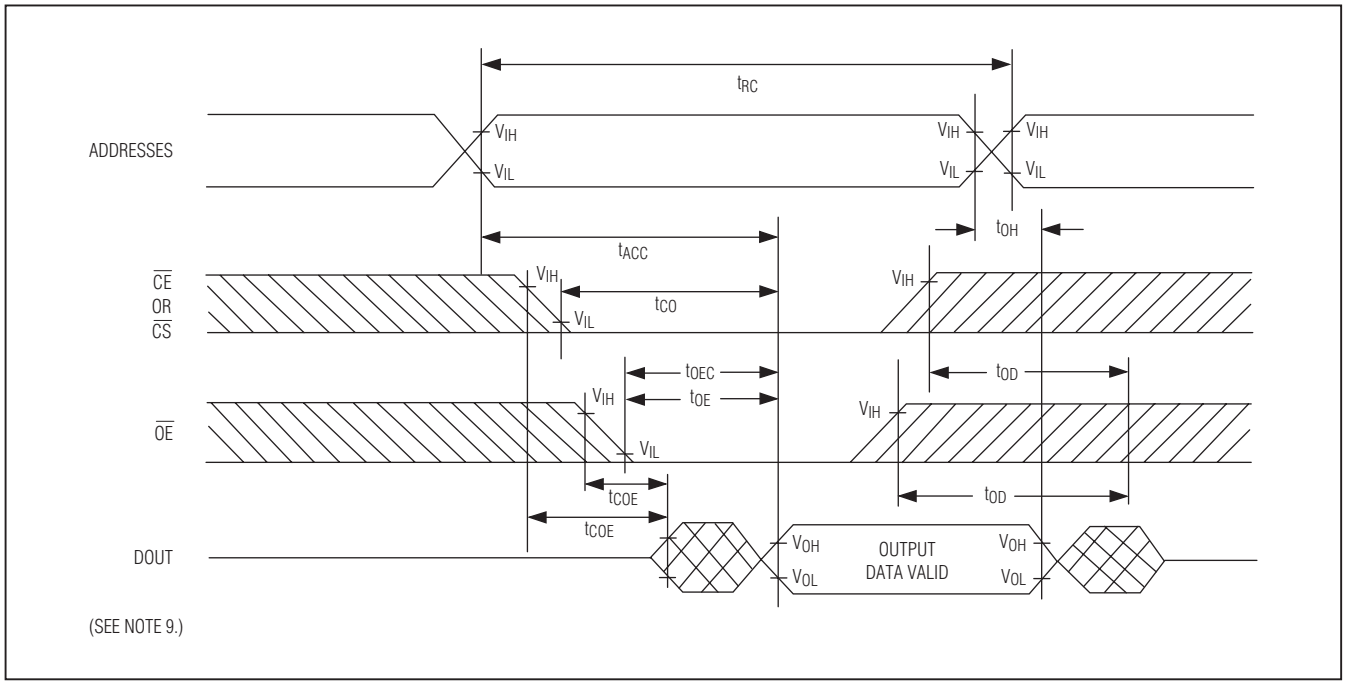
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Expected Data-Retention Time	t_{DR}	(Notes 7, 8)	10			Years

AC TEST CONDITIONS

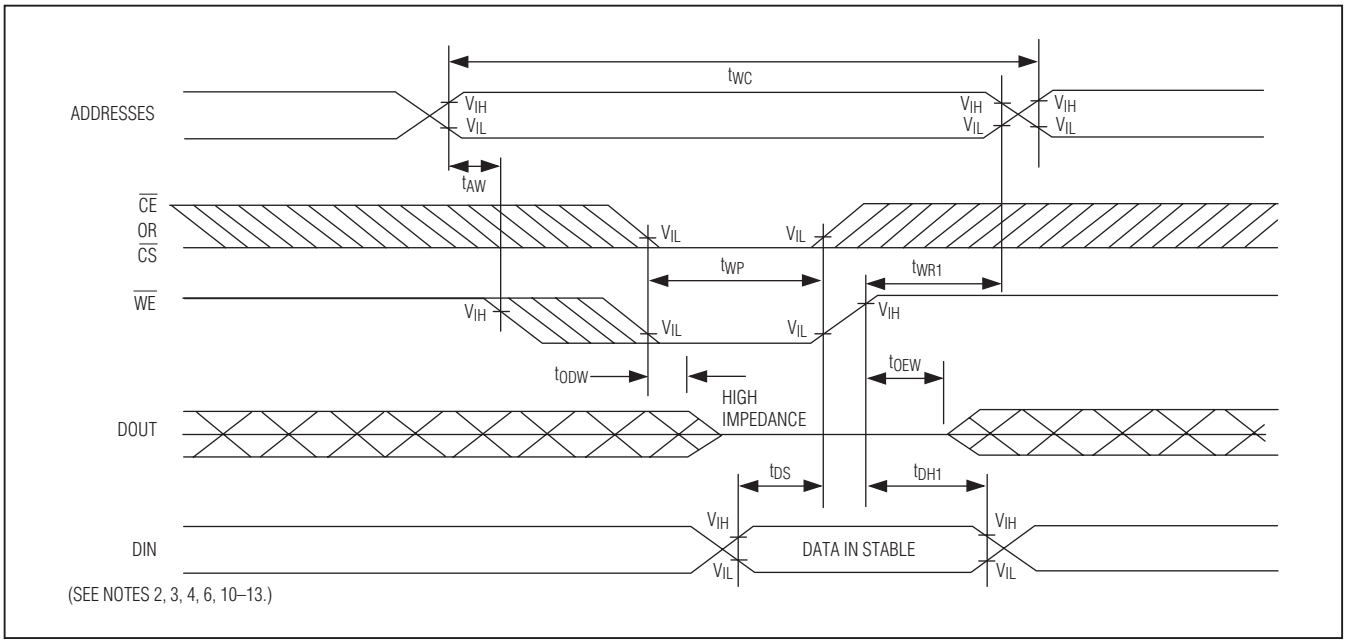
Voltage Range on Any Pin Relative to Ground: -0.3V to +4.6V
Input Pulse Levels: V_{IL} = 0V, V_{IH} = 2.7V
Input Pulse Rise and Fall Times: 5ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1 TTL Gate + C_L (100pF) including scope and jig

3.3V, 8Mb, Nonvolatile SRAM with Clock

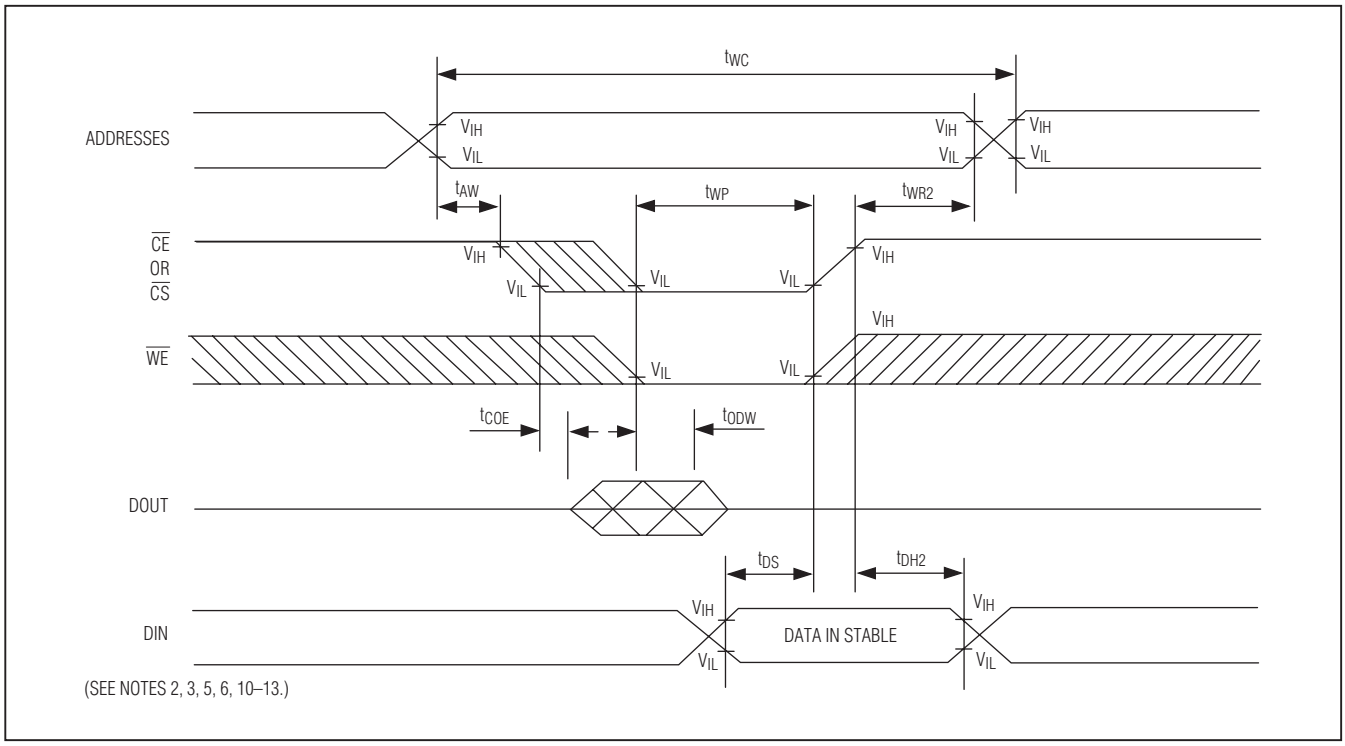
Read Cycle



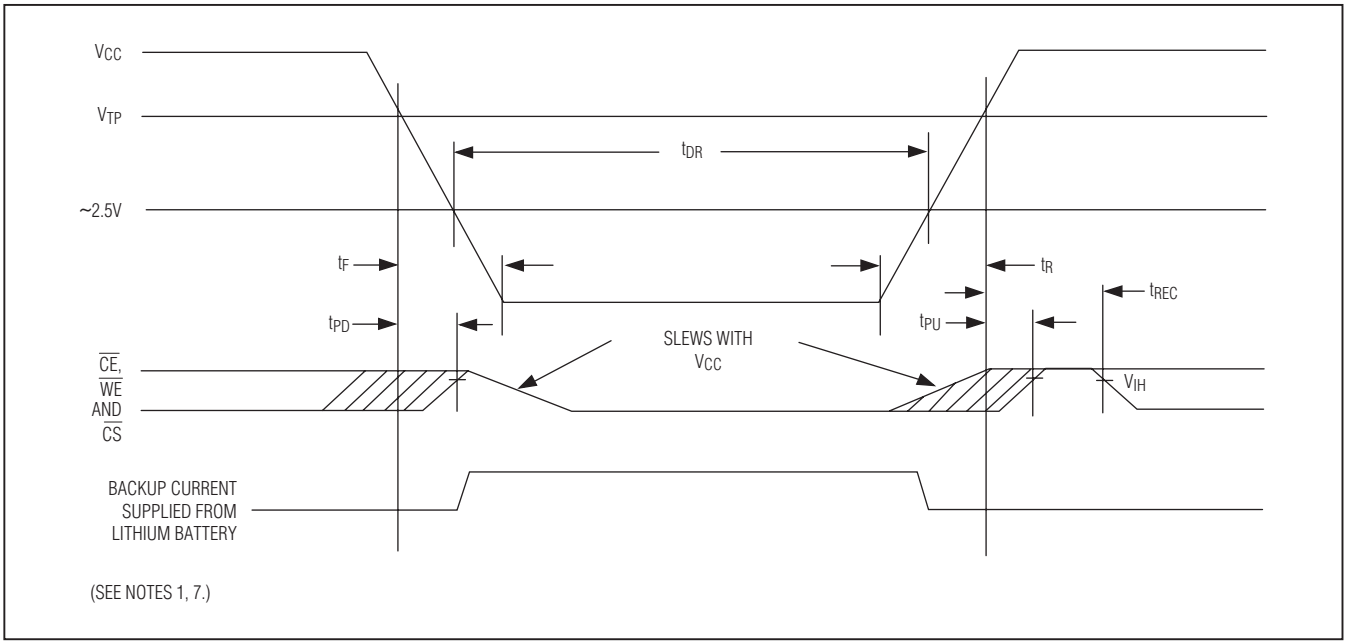
Write Cycle 1



Write Cycle 2



Power-Down/Power-Up Condition



Note 1: All voltages are referenced to ground.

Note 2: These parameters are sampled with a 5pF load and are not 100% tested.

Note 3: t_{WP} is specified as the logical AND of $\overline{CE}$ with $\overline{WE}$ for SRAM writes, or $\overline{CS}$ with $\overline{WE}$ for RTC writes. t_{WP} is measured from the later of the two related edges going low to the earlier of the two related edges going high.

Note 4: t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.

Note 5: t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high for SRAM writes or $\overline{CS}$ going high for RTC writes.

Note 6: t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high for SRAM writes, or from the earlier of $\overline{CS}$ or $\overline{WE}$ going high for RTC writes.

Note 7: In a power-down condition, the voltage on any pin cannot exceed the voltage on V_{CC}.

Note 8: The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user. Minimum expected data-retention time is based upon a single convection reflow exposure, followed by an attachment of a new DS9034I-PCX+. This parameter is assured by component selection, process control, and design. It is not measured directly during production testing.

Note 9: $\overline{WE}$ is high for any read cycle.

Note 10: $V_{\overline{OE}} = V_{IH}$ or V_{IL}. If $V_{\overline{OE}} = V_{IH}$ during write cycle, the output buffers remain in a high-impedance state.

Note 11: If the $\overline{CE}$ or $\overline{CS}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.

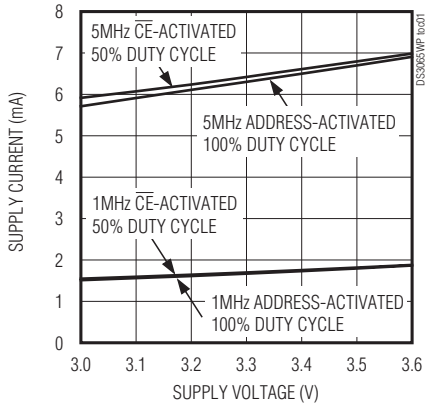
Note 12: If the $\overline{CE}$ or $\overline{CS}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.

Note 13: If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the related $\overline{CE}$ or $\overline{CS}$ low transition, the output buffers remain in a high-impedance state during this period.

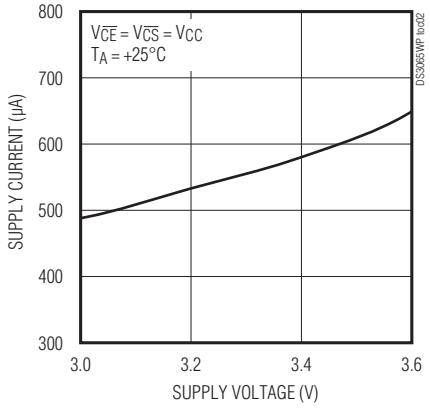
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

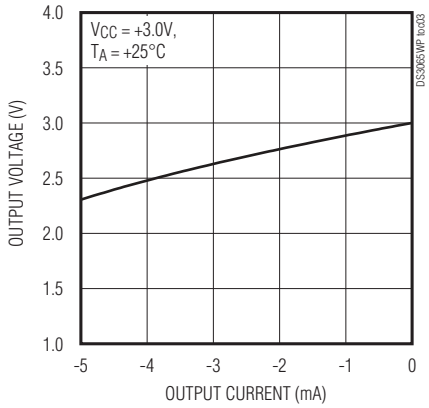
POWER-SUPPLY CURRENT vs. POWER-SUPPLY VOLTAGE



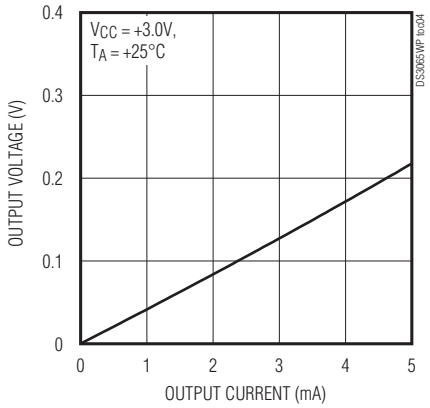
POWER-SUPPLY CURRENT vs. POWER-SUPPLY VOLTAGE



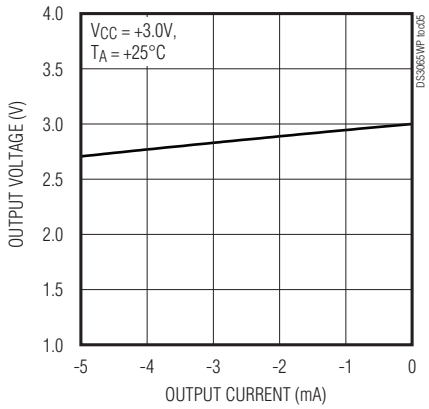
SRAM OUTPUT-VOLTAGE HIGH vs. OUTPUT CURRENT



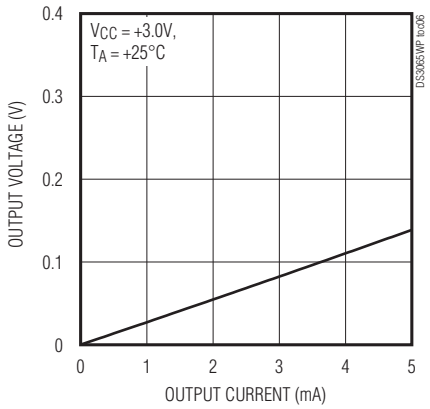
SRAM OUTPUT-VOLTAGE LOW vs. OUTPUT CURRENT



RTC OUTPUT-VOLTAGE HIGH vs. OUTPUT CURRENT

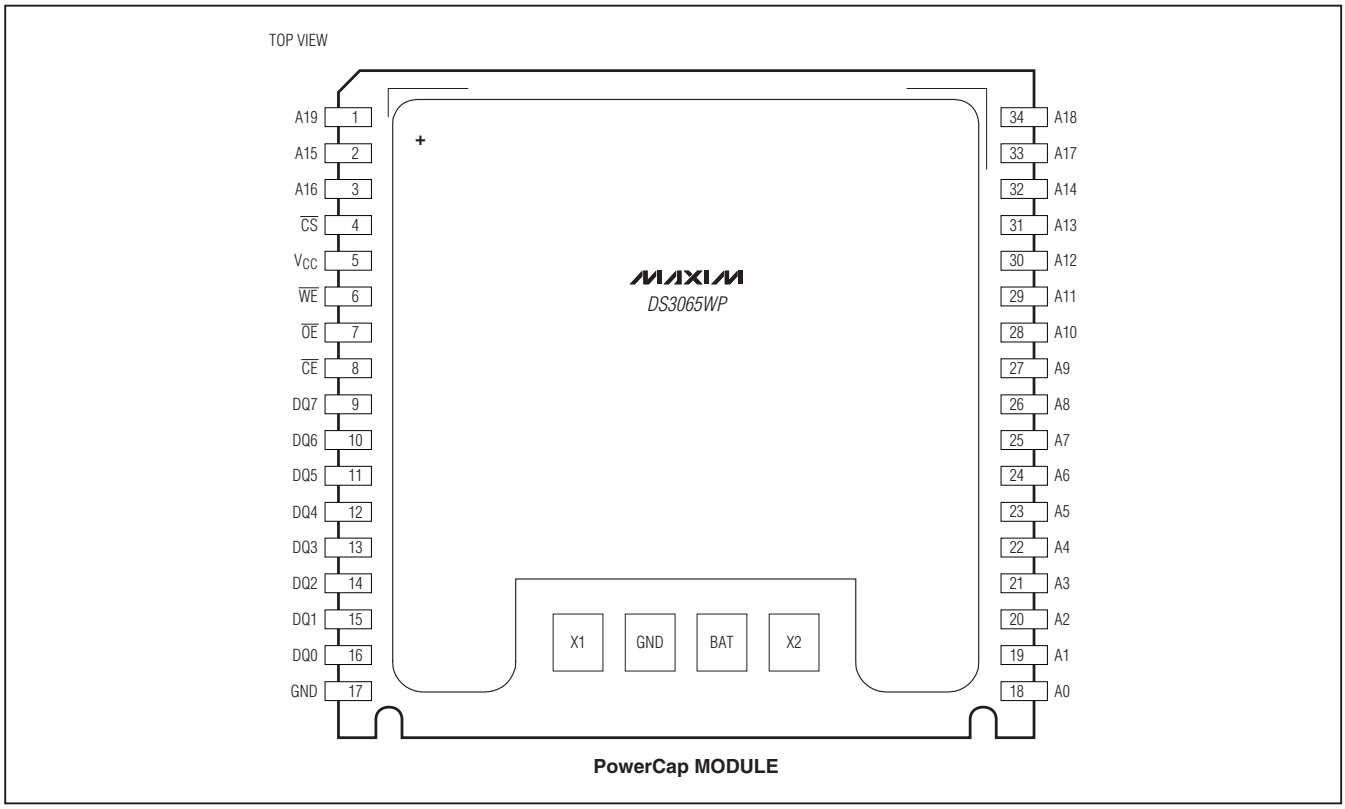


RTC OUTPUT-VOLTAGE LOW vs. OUTPUT CURRENT



3.3V, 8Mb, Nonvolatile SRAM with Clock

Pin Configuration

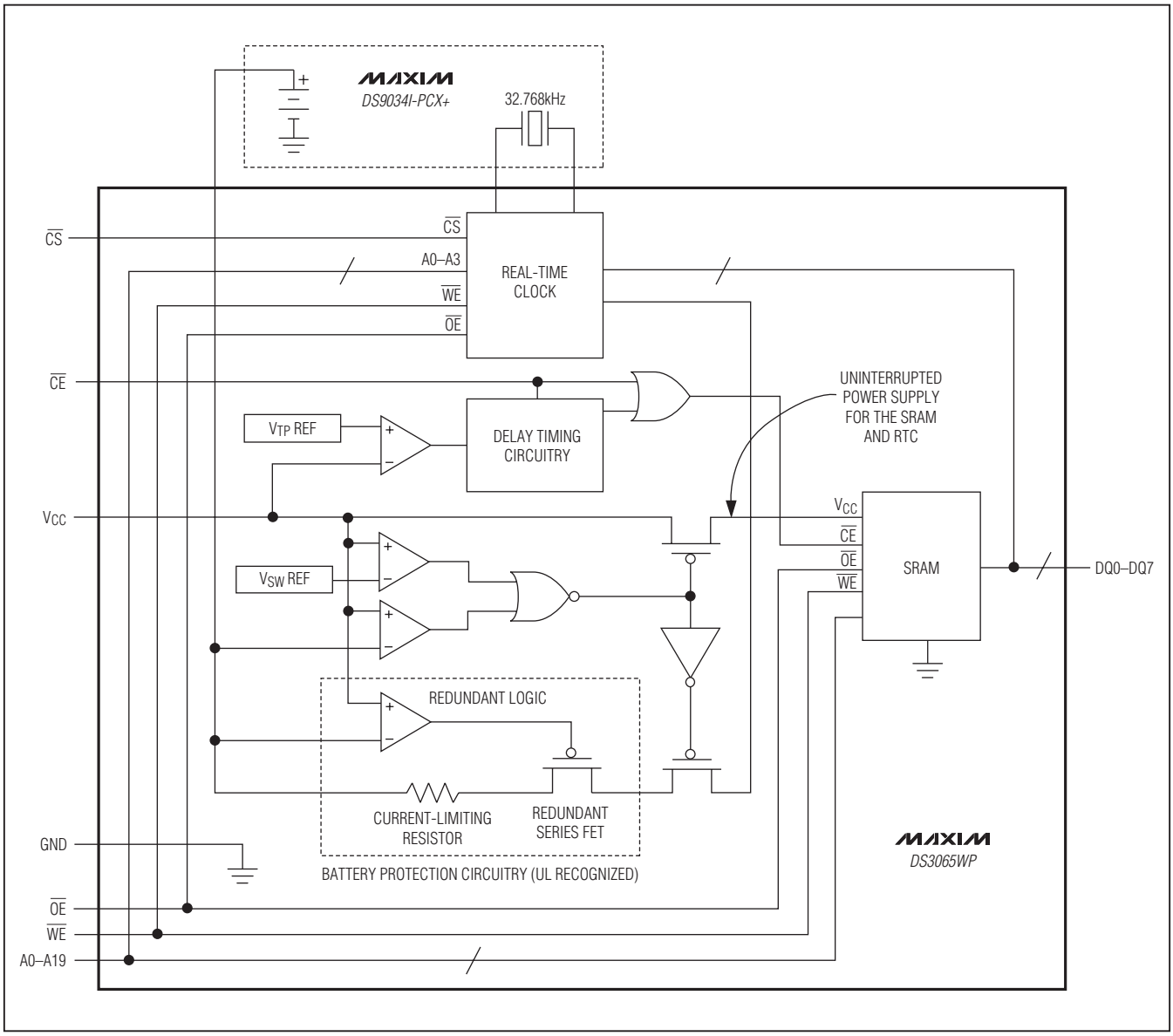


Pin Description

PIN	NAME	FUNCTION
1	A19	Address Input 19
2	A15	Address Input 15
3	A16	Address Input 16
4	$\overline{CS}$	Active-Low RTC Chip-Select Input
5	VCC	Supply Voltage
6	$\overline{WE}$	Active-Low Write-Enable Input
7	$\overline{OE}$	Active-Low Output-Enable Input
8	$\overline{CE}$	Active-Low SRAM Chip-Enable Input
9	DQ7	Data Input/Output 7
10	DQ6	Data Input/Output 6
11	DQ5	Data Input/Output 5
12	DQ4	Data Input/Output 4
13	DQ3	Data Input/Output 3
14	DQ2	Data Input/Output 2
15	DQ1	Data Input/Output 1
16	DQ0	Data Input/Output 0
17	GND	Ground

PIN	NAME	FUNCTION
18	A0	Address Input 0
19	A1	Address Input 1
20	A2	Address Input 2
21	A3	Address Input 3
22	A4	Address Input 4
23	A5	Address Input 5
24	A6	Address Input 6
25	A7	Address Input 7
26	A8	Address Input 8
27	A9	Address Input 9
28	A10	Address Input 10
29	A11	Address Input 11
30	A12	Address Input 12
31	A13	Address Input 13
32	A14	Address Input 14
33	A17	Address Input 17
34	A18	Address Input 18

Functional Diagram



3.3V, 8Mb, Nonvolatile SRAM with Clock

Detailed Description

The DS3065WP is an 8Mb (1024k x 8 bits), fully static, nonvolatile (NV) memory similar in function and organization to the DS1265W NV SRAM, but containing an RTC. The device NV SRAM constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit to the number of write cycles that can be executed, and no additional support circuitry is required for microprocessor interfacing. This device can be used in place of SRAM, EEPROM, or flash components.

User access to either the SRAM or the RTC registers is accomplished with a byte-wide interface and discrete control inputs, allowing for a direct interface to many 3.3V microprocessor devices.

The RTC contains a full-function clock/calendar with an RTC alarm, battery monitor, and power monitor. RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in a 24-hour BCD format. Corrections for day of the month and leap year are made automatically.

The RTC registers are double-buffered into an internal and external set. The user has direct access to the external set. Clock/calendar updates to the external set of registers can be disabled and enabled to allow the user to access static data. Assuming the internal oscillator is on, the internal registers are continually updated, regardless of the state of the external registers, assuring that accurate RTC information is always maintained.

The device constantly monitors the voltage of the internal battery. The battery-low flag (BLF) in the RTC FLAGS register is not writable and should always be a 0 when read. Should a 1 ever be present, the battery voltage is below ~ 2V and the contents of the clock and SRAM are questionable.

The device module is constructed on a standard 34-pin PowerCap substrate.

SRAM Read Mode

The device executes an SRAM read cycle whenever $\overline{CS}$ (RTC chip select) and $\overline{WE}$ (write enable) are inactive (high) and $\overline{CE}$ (SRAM chip enable) is active (low). The unique address specified by the 20 address inputs (A0–A19) defines which of the 1,048,576 bytes of SRAM data is to be accessed. Valid data is available to the eight data-output drivers within t_{ACC} (access time) after the last address input signal is stable, provided that $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied.

If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied, data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$), and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

SRAM Write Mode

The device executes an SRAM write cycle whenever $\overline{CS}$ is inactive (high) and the $\overline{CE}$ and $\overline{WE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ determines the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{CS}$ and $\overline{OE}$ control signal should be kept inactive (high) during SRAM write cycles to avoid bus contention. However, if the output drivers have been enabled ($\overline{CE}$ and $\overline{OE}$ active), $\overline{WE}$ disables the outputs in t_{ODW} from its falling edge.

Table 1. RTC/Memory Operational Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	MODE	ICC	OUTPUTS
0	1	1	0	RTC Read	Active	Active
0	1	1	1	RTC Read	Active	High Impedance
0	0	1	X	RTC Write	Active	High Impedance
1	1	0	0	SRAM Read	Active	Active
1	1	0	1	SRAM Read	Active	High Impedance
1	0	0	X	SRAM Write	Active	High Impedance
1	X	1	X	Standby	Standby	High Impedance
0	X	0	X	Invalid (see Figure 2)	Active	Invalid

X = Don't care.

Clock Operations

RTC Read Mode

The device executes an RTC read cycle whenever $\overline{CE}$ (SRAM chip enable) and $\overline{WE}$ (write enable) are inactive (high) and $\overline{CS}$ (RTC chip select) is active (low). The least significant four address inputs (A0–A3) define which of the 16 RTC registers is to be accessed (see Table 3). Valid data is available to the eight data-output drivers within t_{ACC} (access time) after the last address input signal is stable, provided that $\overline{CS}$ and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{CS}$ and $\overline{OE}$ access times are not satisfied, data access must be measured from the later-occurring signal ($\overline{CS}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CS}$ or t_{OEC} for $\overline{OE}$ rather than address access.

RTC Write Mode

The device executes an RTC write cycle whenever $\overline{CE}$ is inactive (high) and the $\overline{CS}$ and $\overline{WE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CS}$ or $\overline{WE}$ determines the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CS}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{CE}$ and $\overline{OE}$ control signals should be kept inactive (high) during RTC write cycles to avoid bus contention. However, if the output drivers have been enabled ($\overline{CS}$ and $\overline{OE}$ active), $\overline{WE}$ disables the outputs in t_{ODW} from its falling edge.

Clock Oscillator Mode

The oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB of the SECONDS register (B7 of F9h). Setting $\overline{OSC}$ to 1 stops the oscillator; setting $\overline{OSC}$ to 0 starts the oscillator. The initial state of $\overline{OSC}$ is not guaranteed. When power is applied for the first time, the $\overline{OSC}$ bit should be enabled.

Reading the Clock

When reading the RTC data, it is recommended to halt updates to the external set of double-buffered RTC registers. This puts the external registers into a static state, allowing the data to be read without register values changing during the read process. Normal updates to the internal registers continue while in this state.

External updates are halted by writing a 1 to the read bit (R). As long as a 1 remains in the R bit, updating is inhibited. After a halt is issued, the registers reflect the RTC count (day, date, and time) that was current at the moment the halt command was issued. Normal updates to the external set of registers resume within one second after the R bit is set to 0 for a minimum of 500µs. The R bit must be 0 for a minimum of 500µs to ensure the external registers have fully updated.

Setting the Clock

As with a clock read, it is also recommended to halt updates prior to setting new time values. Setting the write bit (W) to 1 halts updates of the external RTC registers 8h–Fh. After setting the W bit to 1, the RTC registers can be loaded with the desired count (day, date, and time) in BCD format. Setting the W bit to 0 then transfers the values written to the internal registers and allows normal clock operation to resume.

Using the Clock Alarm

The alarm settings and control for the device reside within RTC registers 2h–5h. The INTERRUPTS register (6h) contains two alarm-enable bits: alarm flag enable (AE) and alarm in backup-mode enable (ABE).

The alarm can be programmed to activate on a specific day of the month or repeat every day, hour, minute, or second. Alarm mask bits AM[4:1] control the alarm mode (Table 2). Configurations not listed in the table default to the once-per-second mode to notify the user of an incorrect alarm setting.

Table 2. Alarm Mask Bits

AM4	AM3	AM2	AM1	ALARM RATE
1	1	1	1	Once per second
1	1	1	0	When seconds match
1	1	0	0	When minutes and seconds match
1	0	0	0	When hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

3.3V, 8Mb, Nonvolatile SRAM with Clock

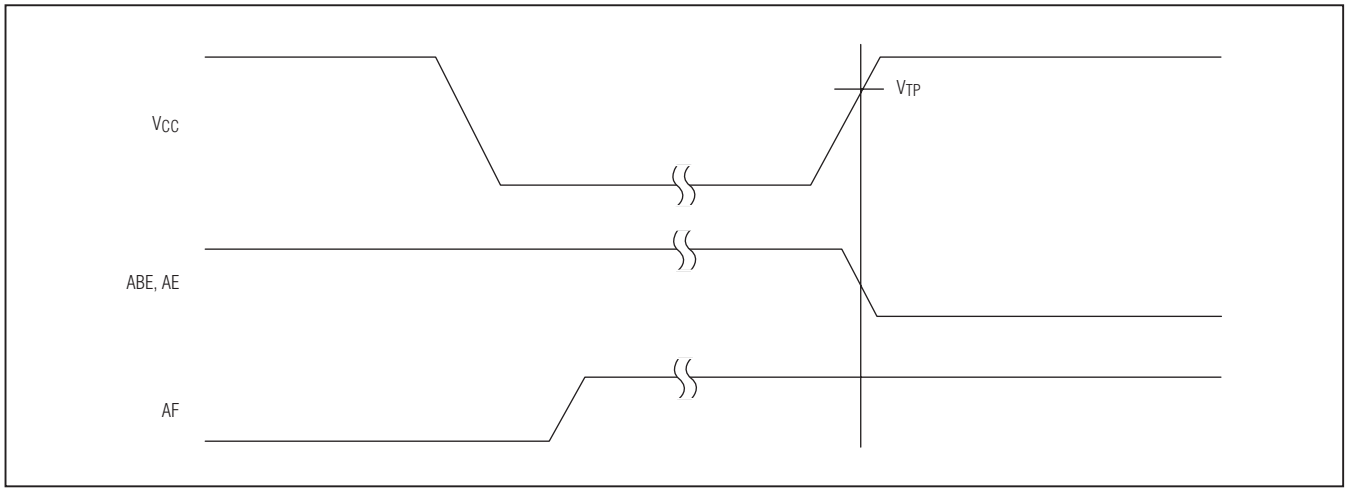


Figure 1. Battery-Backup Mode Alarm Waveforms

When the RTC register values match alarm register settings, the alarm flag (AF) is set to 1.

The AE and ABE bits are reset to 0 during the power-up transition, but an alarm generated during power-up sets AF to 1. Therefore, the AF bit can be read after system power-up to determine if an alarm was generated during the power-up sequence. Figure 1 illustrates alarm timing during battery-backup mode and power-up states.

Clock Accuracy

The DS3065WP and DS9034I-PCX+ are each individually tested for accuracy. Once mounted together, the module typically keeps time accuracy to within ±1.53 minutes per month (35ppm) at +25°C and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. The electrical environment also affects clock accuracy, and caution should be taken to place the component in the lowest level EMI section of the PCB layout. For additional information, refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clocks (RTCs)*.

Power-On Default States

Upon each application of power to the device, the following register bits are automatically set to 0: WDS = 0, BMB[4:0] = 0, RB0 = 0, RB1 = 0, AE = 0, ABE = 0. All other RTC bits are undefined.

Data-Retention Mode

The device provides full functional capability for V_{CC} greater than 3.0V and write protects by 2.8V. Data is maintained in the absence of V_{CC} without additional support circuitry. The NV SRAM constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write protects itself. All inputs become don't care, and all data outputs become high impedance. As V_{CC} falls below approximately 2.5V (V_{SW}), the power-switching circuit connects the lithium energy source to the clock and SRAM to maintain time and retain data. During power-up, when V_{CC} rises above V_{SW}, the power-switching circuit connects external V_{CC} to the clock and SRAM and disconnects the lithium energy source. Normal clock or SRAM operation can resume after V_{CC} exceeds V_{TP} for a minimum duration of t_{REC}.

Freshness Seal

When the DS9034I-PCX+ battery cap is first attached to a DS3065WP base, the RTC oscillator is disabled and the lithium battery is electrically disconnected, guaranteeing that no battery capacity has been consumed during transit or storage.

When V_{CC} is first applied at a level greater than V_{TP}, the lithium battery is enabled for backup operation. The user is required to enable the oscillator (MSB of the SECONDS register) and initialize the required RTC registers for proper timekeeping operation.

Table 3. RTC Register Map

ADDR	DATA								FUNCTION	RANGE
	B7	B6	B5	B4	B3	B2	B1	B0		
xxxxFh	10 YEAR				YEAR				YEAR	00–99
xxxxEh	X	X	X	10 MO	MONTH				MONTH	01–12
xxxxDh	X	X	10 DATE		DATE				DATE	01–31
xxxxCh	X	FT	X	X	X	DAY			DAY	01–07
xxxxBh	X	X	10 HOUR		HOUR				HOUR	00–23
xxxxAh	X	10 MINUTES			MINUTES				MINUTES	00–59
xxxx9h	$\overline{OSC}$	10 SECONDS			SECONDS				SECONDS	00–59
xxxx8h	W	R	10 CENTURY		CENTURY				CONTROL	00–39
xxxx7h	Y	Y	Y	Y	Y	Y	Y	Y	Unused	—
xxxx6h	AE	Y	ABE	Y	Y	Y	Y	Y	INTERRUPTS	—
xxxx5h	AM4	Y	10 DATE		DATE				ALARM DATE	01–31
xxxx4h	AM3	Y	10 HR		HOURS				ALARM HOURS	00–23
xxxx3h	AM2	10 MINUTES			MINUTES				ALARM MINUTES	00–59
xxxx2h	AM1	10 SECONDS			SECONDS				ALARM SECONDS	00–59
xxxx1h	Y	Y	Y	Y	Y	Y	Y	Y	Unused	—
xxxx0h	WF	AF	0	BLF	0	0	0	0	FLAGS	—

x = Don't care address bits
X = Unused; read/writable under write and read bit control
Y = Unused; read/writable without write and read bit control
0 = Reads as 0 and cannot be changed
FT = Frequency test bit
$\overline{OSC}$ = Oscillator start/stop bit
W = Write bit
R = Read bit
AE = Alarm flag enable
ABE = Alarm in backup-mode enable
AM[4:1] = Alarm mask bits
WF = Watchdog flag
AF = Alarm flag
BLF = Battery-low flag

3.3V, 8Mb, Nonvolatile SRAM with Clock

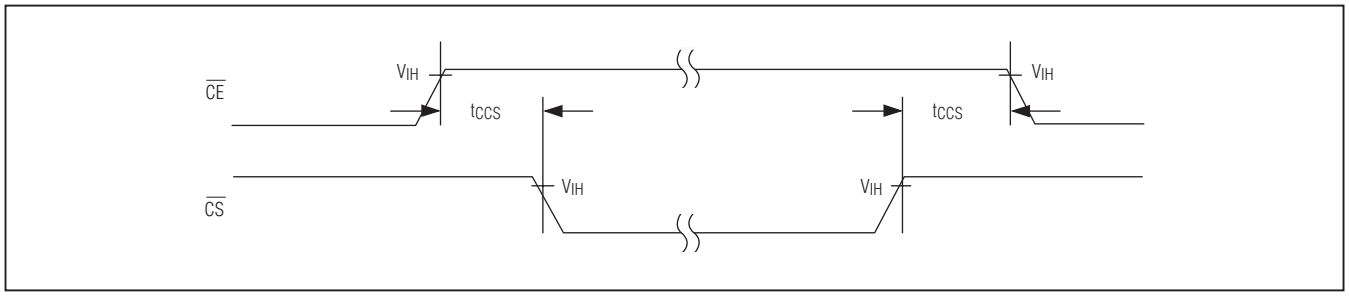


Figure 2. SRAM/RTC Data Bus Control

Applications Information

Power-Supply Decoupling

To achieve the best results when using the device, decouple the power supply with a 0.1µF capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Avoiding Data Bus Contention

Care should be taken to avoid simultaneous access of the SRAM and RTC devices (see Figure 2). Any chip-enable overlap violates t_{CCS} and can result in invalid and unpredictable behavior.

Recommended Cleaning Procedures

The device can be cleaned using aqueous-based cleaning solutions. No special precautions are needed when cleaning boards containing a DS3065WP module, provided that the cleaning and subsequent drying process is completed prior to the DS9034I-PCX+ attachment.

DS3065W modules are recognized by Underwriters Laboratories (UL) under file E99151.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
34 PCAP	—	**21-0246**	See the outline no. 21-0246

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/10	Initial release	—