SMH4803A

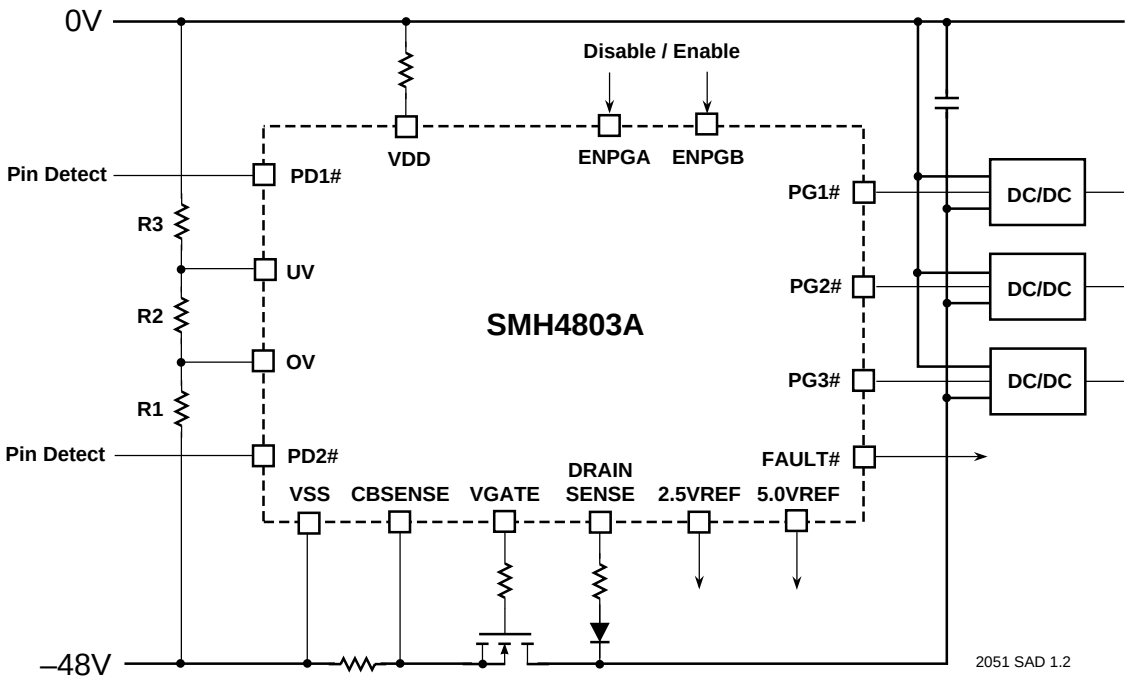
Distributed Power Hot Swap Controller

Preliminary

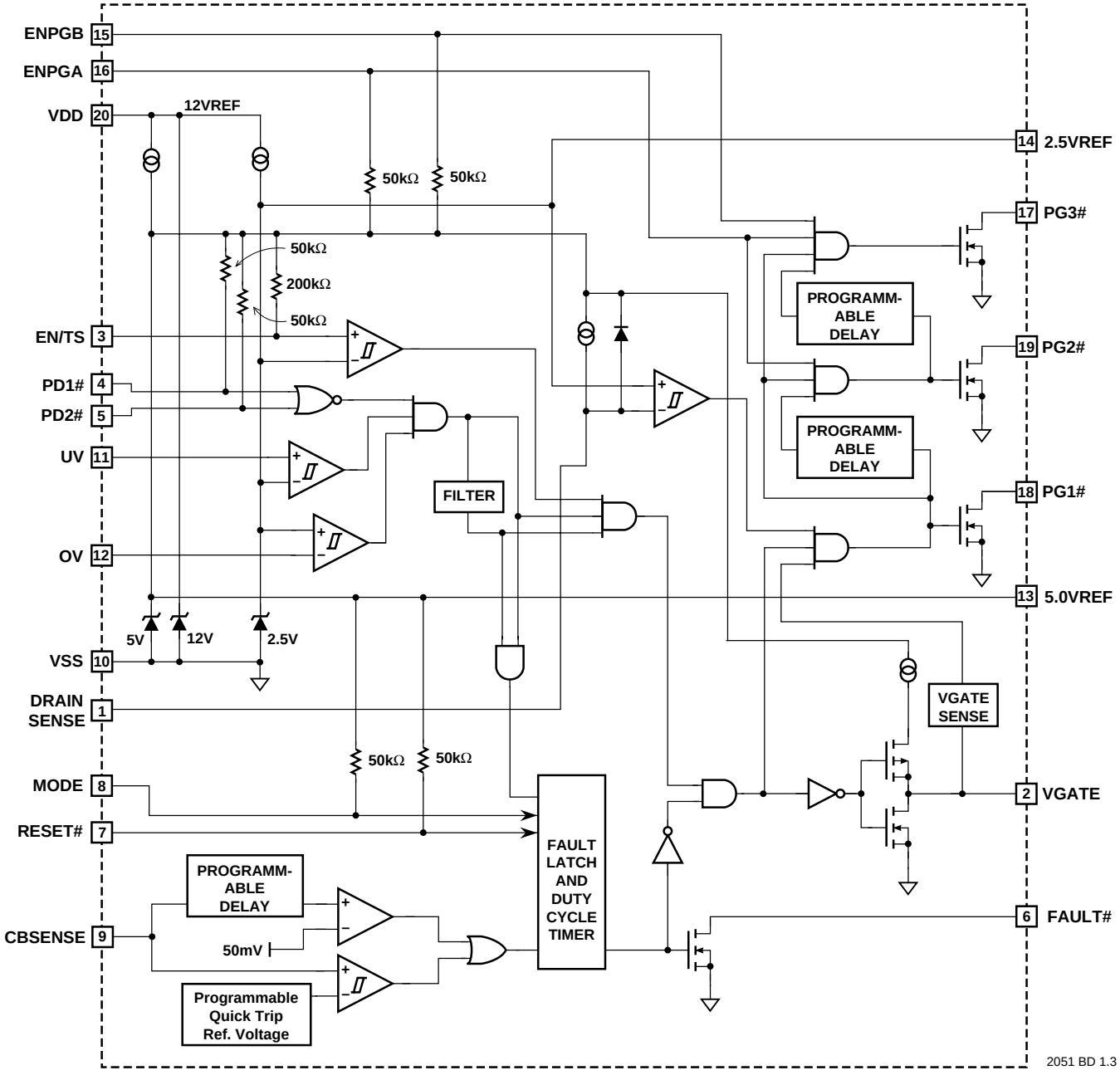
FEATURES

- Soft Starts Main Power Supply on Card Insertion or System Power Up
- Senses Card Insertion via Short Pins or Ejector Switches
- Master Enable to Allow System Control of Power Up or Down
  - Can be used as a Temperature Sense Input
- Programmable Independent Controls of 3 DC/DC Converters
  - Not Enabled until Host Supply Fully Soft Started
  - Programmable Time Delay Between each Enable Signal
  - Available Input to hold off Dependant Enables until Conditions are Satisfied
- Highly Programmable Circuit Breaker
  - Programmable Quick-Trip™ Values
  - Programmable Current Limiting
  - Programmable Circuit Breaker Mode: Latched (Volatile or Nonvolatile)
  - Programmable Duty Cycle Times
  - Programmable Over-current Filter
- Programmable Host Voltage Fault Monitoring
  - Programmable Under- voltage Hysteresis
  - Programmable UV/OV Voltage Filter
  - Programmable Fault Mode: Latched or Duty Cycle
- Nonvolatile Programming to Customize Features
  - Available Pre-programmed from Summit
- 2.5V and 5.0V Reference Outputs
  - Eliminates the Need or Other Primary Voltages
  - Easy Expansion of External Monitor Functions
- Supply Range ±20VDC to >±500VDC

SIMPLIFIED APPLICATION DRAWING



FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

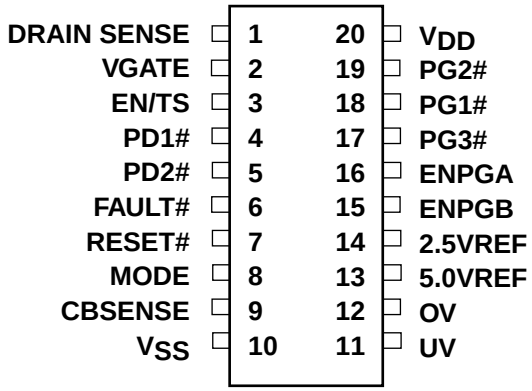
The SMH4803A is an integrated solution for high reliability systems to monitor and react to events that could have a detrimental effect on a system. It can contain or limit faults to a single circuit board before that fault propagates to the system. Its programmability lets a single board satisfy multiple circuit demands while customized to meet special requirements.

The SMH4803A monitors and controls the primary voltage in a distributed power system while providing for both hot-swapping and secondary voltage sequencing in multi-supply systems. The primary power source can be shut down if events are sensed that could result in damage to either the circuit board or the system supply. An external FET switch is used to soft start the primary voltage once normal operating conditions are met. The external FET also uses an external shunt to monitor current for the circuit breaker function.

The SMH4803A sequences secondary voltage by timed or externally controlled outputs that enable DC/DC converters. Its reference voltages provide isolation between primary and secondary voltages, but allow expansion of its features.

PIN CONFIGURATION

20-Pin SOIC



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PIN DESCRIPTIONS

DRAIN SENSE (1)

The DRAIN SENSE input monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. An internal 10µA source pulls the DRAIN SENSE signal towards the 5V reference level. DRAIN SENSE must be held below 2.5V to enable the PG outputs.

VGATE (2)

The VGATE output activates an external power MOSFET switch. This signal supplies a constant current output (100µA typical), which allows easy adjustment of the MOSFET turn on slew rate.

EN/TS (3)

The Enable/Temperature Sense input is the master enable input. If EN/TS is less than 2.5V, VGATE will be disabled. This pin has an internal 200kΩ pull-up to 5V.

PD1# and PD2# (4 & 5)

These are logic level active low inputs that can optionally be employed to enable VGATE and the PG outputs when they are at V_{SS}. These pins each have an internal 50kΩ pull-up to 5V.

FAULT# (6)

This is an open-drain, active-low output that indicates the fault status of the device.

RESET# (7)

Reset# is used to clear latched fault conditions. When this pin is held low the VGATE and PG outputs are disabled. Refer to the Circuit Breaker Operation and the associated timing diagrams for detailed characteristics. This pin has an internal 50kΩ pull-up to 5V.

MODE (8)

The state of the MODE signal determines how fault conditions are cleared. The device is in the latched mode when the signal is held at V_{SS}, and the cycle mode when held at 5V or left floating. This pin has an internal 50kΩ pull-up to 5V.

CBSENSE (9)

The circuit breaker sense input is used to detect overcurrent conditions across an external, low value sense resistor (R_S) tied in series with the Power MOSFET. A voltage drop of greater than 50mV across the resistor for longer than t_{CBD} will trip the circuit breaker. A programmable Quick-Trip™ sense point is also available.

UV (11)

The UV pin is used as an under-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE will be disabled if UV is less than 2.5V. Programmable internal hysteresis is available on the UV input, adjustable in increments of 62.5mV. Also available is a filter delay on the UV input.

OV (12)

The OV pin is used as an over-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE will be disabled if OV is greater than 2.5V. A filter delay is available on the OV input.

5.0VREF & 2.5VREF (13 & 14)

These are precision 5V and 2.5V output reference voltages that may be use to expand the logic input functions on the SMH4803A. The reference outputs are with respect to V_{SS}.

ENPGA (16)

This is an active high input that controls the PG2# and PG3# outputs. When ENPGA is pulled low the PG2# and PG3# outputs are immediately placed in a high impedance state. When ENPGA is driven high or left floating then PG2# will be driven low at a time period of t_{PGD} after PG1# has been active. This pin has an internal 50kΩ pull-up to 5V.

ENPGB (15)

This is an active high input that controls the PG3# output. When ENPGB is pulled low the PG3# output is immediately placed in a high impedance state. When ENPGB is driven high or left floating then PG3# will be driven low at a time period of t_{PGD} after PG2# has been active. This pin has an internal 50kΩ pull-up to 5V.

PG1#, PG2#, & PG3# (18, 19, & 17)

The PGn# pins are open-drain, active-low outputs with no internal pull-up resistor. They can be used to switch a load or enable a DC/DC converter. PG1# is enabled immediately after VGATE reaches $V_{DD} - V_{GT}$ and the DRAIN SENSE voltage is less than 2.5V. Each successive PG output is enabled t_{PGD} after its predecessor, provided also that the appropriate ENPG input(s) are high. Voltage on these pins cannot exceed 12V, as referenced to V_{SS}.

V_{DD} (20)

V_{DD} is the positive supply connection. An internal shunt regulator limits the voltage on this pin to approximately 12V with respect to VSS. A resistor must be placed in series with the V_{DD} pin to limit the regulator current (R_D in the application illustrations).

V_{SS} (10)

V_{SS} is connected to the negative side of the supply.

RECOMMENDED OPERATING CONDITIONS

Temperature –40°C to 85°C.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10s) ..... 300°C
Terminal Voltage with Respect to V_{SS}:
VGATE ..... V_{DD} + 0.5V
UV, OV, CBSENSE, DRAIN SENSE, FAULT#, PG1#, PG2#, and PG3# ..... –0.5V to V_{DD} + 0.5V
PD1#, PD2#, MODE, RESET#, ENPGA, ENPGB, EN/TS 10V

*Comment

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to V_{SS}, except V_{GT}**)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	I_{DD} = 3mA	11	12	13	V
5.0VREF	5V reference output	I_{DD} = 3mA	4.75	5.00	5.25	V
I_{LOAD5}	5V reference output current	I_{DD} = 3mA	–1		1	mA
2.5VREF	2.5V reference output	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
		I_{DD} = 3mA	2.425	2.500	2.575	V
$I_{LOAD2.5}$	2.5V reference output current	I_{DD} = 3mA	–0.2		1	mA
I_{DD}	Power supply current	Output enabled	2		10	mA
V_{UV}	Under-Voltage threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
		I_{DD} = 3mA	2.425	2.500	2.575	V
V_{UVHYST}	Under-Voltage hysteresis	I_{DD} = 3mA		10		mV
V_{OV}	Over-Voltage threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
		I_{DD} = 3mA	2.425	2.500	2.575	V
V_{OVHYST}	Over-Voltage hysteresis	I_{DD} = 3mA		10		mV
V_{VGATE}	VGATE output voltage				V_{DD}	V
I_{VGATE}	VGATE current output			100		µA
V_{SENSE}	DRAIN SENSE threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
		I_{DD} = 3mA	2.425	2.500	2.575	V
I_{SENSE}	DRAIN SENSE current output	$V_{SENSE} = V_{SS}$ (1)	9	10	11	µA
V_{CB}	Circuit breaker threshold	I_{DD} = 3mA	40	50	60	mV
V_{QCB}	Programmable Quick Trip circuit breaker threshold			200		mV
				100		mV
				60		mV
		Off				—
V_{ENTS}	EN/TS threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
		I_{DD} = 3mA	2.425	2.500	2.575	V
$V_{ENTSHYST}$	EN/TS hysteresis	I_{DD} = 3mA		10		mV
V_{IH}	Input high voltage: ENPGA/B, MODE, RESET#		2		5.0VREF	V
V_{IL}	Input low voltage: ENPGA/B, MODE, RESET#		–0.1		0.8	V
V_{OL}	Output low voltage: FAULT#	I_{OL} = 2mA	0		0.4	V
	Output low voltage: PG1#/2#/3#	I_{SINK} = 2mA	0		0.4	V
V_{GT}	Gate threshold		0.7	1.8	3.0	V

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(1) TA = 25°C.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The SMH4803A is an integrated power controller for hot swappable add-in cards. The device operates from a wide supply range and generates the signals necessary to drive isolated output DC/DC converters. As a typical add-in board is inserted into the powered backplane physical connections must first be made with the chassis to discharge any electrostatic voltage potentials. The board then contacts the long pins on the backplane that provide power and ground. As soon as power is applied the device starts up, but does not immediately apply power to the output load. Under-voltage and over-voltage circuits inside the controller check to see that the input voltage is within a user-specified range, and pin detection signals determine whether the card is seated properly.

These requirements must be met for a Pin Detect Delay period of t_{PDD}, after which time the hot-swap controller enables VGATE to turn on the external power MOSFET switch. The VGATE output is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. During the controlled turn-on period the V_{DS} of the MOSFET is monitored by the drain sense input. When drain sense drops below 2.5V, and VGATE gets above $V_{DD} - V_{GT}$, the power good outputs can begin turning on the DC/DC controllers. Power Good Enable inputs may be used to activate or deactivate specific output loads.

Steady state operation is maintained as long as all conditions are normal. Any of the following events may cause the device to disable the DC/DC controllers by shutting down the power MOSFET: an under-voltage or over-voltage condition on the host power supply; an over-current event detected on the CBSENSE input; a failure of the power MOSFET sensed via the DRAIN SENSE pin; the pin detect signals becoming invalid; or the master enable (EN/TS) falling below 2.5V. The SMH4803A may be configured so that after any of these events occur the VGATE output shuts off and either latches into an off state or recycles power after a cooling down period, t_{CYC}.

Powering V_{DD}

The SMH4803A contains a shunt regulator on the V_{DD} pin that prevents the voltage from exceeding 12V. It is necessary to use a dropper resistor (R_D) between the host power supply and the V_{DD} pin in order to limit current into the device and prevent possible damage. The dropper resistor allows the device to operate across a wide range of system supply voltages, and also helps protect the device against common-mode power surges. Refer to the Applications Section for help on calculating the R_D resistance value.

System Enables

There are several enabling inputs, which allow a host system to control the SMH4803A. The Pin Detect pins (PD1# & PD2#) are two active low enables that are generally used to indicate that the add-in circuit card is properly seated. This is typically done by clamping the inputs to V_{SS} through the implementation of an injector switch, or alternatively through the use of a staggered pins at the card-cage interface. Two shorter pins arrayed at opposite ends of the connector force the card to be fully seated (not canted) before both pin detects are enabled. Care must be taken not to exceed the maximum voltage rating of these pins during the insertion process. Refer to details in the Applications Section for proper circuit implementation.

The EN/TS input provides an active high comparator input that may be used as a master enable or temperature sense input. These inputs must be held low for a period of t_{PDD} before a power-up sequence may be initiated.

Under-/Over-Voltage Sensing

The Under-Voltage (UV) and Over-Voltage (OV) inputs provide a set of comparators that act in conjunction with an external resistive divider ladder to sense when the host supply voltage exceeds the user defined limits. If the input to the UV pin rises above 2.5V, or the input to the OV pin falls below 2.5V for a period of t_{PDD}, the power-up sequence may be initiated. The t_{PDD} filter helps prevent spurious start-up sequences while the card is being inserted. If UV falls below 2.5V or OV rises above 2.5V, the PG and VGATE outputs will be shut down immediately.

Under-/Over-Voltage Filtering

The SMH4803A may also be configured so that an out of tolerance condition on UV/OV will not shut off the output immediately. Instead, a filter delay may be inserted so that only sustained under-voltage or over-voltage conditions will shut off the output. When the UV/OV filter option is enabled an out of tolerance condition on UV/OV for longer than the filter delay time, t_{UOFLTR}, activates the FAULT# output, and the VGATE and PG outputs will be latched in the off state. To initiate another power-up sequence the FAULT# output must first be reset. Refer to the appropriate section on resetting the FAULT# output. The Under-/Over-Voltage Filtering feature is disabled in the default configuration of the device.

Under-Voltage Hysteresis

The Under-Voltage comparator input may be configured with a programmable level of hysteresis. The compare

level may be set in steps (up to 15) of 62.5mV below 2.5V. The default under-voltage hysteresis level is set to 62.5mV.

Soft Start Slew Rate Control

Once all of the preconditions for powering up the DC/DC controllers have been met, the SMH4803A provides a means to soft start the external power FET. It is important to limit in-rush current to prevent damage to the add-in card or disruptions to the host power supply. For example, charging the filter capacitance (normally required at the input of the DC/DC controllers) too quickly may generate very high current. The VGATE output of the SMH4803A is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. The slew rate may be found by dividing I_{VGATE} by the gate-to-drain capacitance placed on the external FET. A complete design example is given in the Applications Section.

Load Control — Sequencing the Secondary Supplies

Once power has been ramped to the DC/DC controllers, two conditions must be met before the PGn# outputs can be enabled: the Drain Sense voltage must be below 2.5V, and the VGATE voltage must be greater than $V_{DD} - V_{GT}$. The Drain Sense input helps ensure that the power MOSFET is not absorbing too much steady state power from operating at a high V_{DS}. This sensor remains active at all times (except during the current regulation period). The VGATE sensor makes sure that the power MOSFET is operating well into its saturation region before allowing the loads to be switched on. Once VGATE reaches $V_{DD} - V_{GT}$ this sensor is latched.

Once the external MOSFET is properly switched on the PGn# outputs may be enabled (if ENPGA and ENPGB are both high). Output PG1# is activated first, followed by PG2# after a delay of t_{PGD}, and PG3# after another t_{PGD} delay. The delays built into the SMH4803A allow timed sequencing of power to the loads. The delay times are factory programmed from 50µs to 160ms.

PG2# and PG3# can be disabled by bringing ENPGA low. Likewise PG#3 is disabled when ENPGB is low. This cascaded control is useful for enabling supplies that have dependencies based on the other voltages in the system.

The PGn# outputs have a 12V withstand capability, so high voltages must not be connected to these pins. Bipolar transistors or opto-isolators can be used to boost the withstand voltage to that of the host supply. See Figures 10 and 11 for connections.

Circuit Breaker Operation

The SMH4803A provides a number of circuit breaker functions to protect against over current conditions. A sustained over-current event could damage the host supply and/or the load circuitry. The board's load current passes through a series resistor (R_S) connected between the MOSFET source (which is tied to CBSENSE) and V_{SS}. The breaker trips whenever the voltage drop across R_S is greater than 50mV for more than t_{CBD} (a factory programmable filter delay ranging from 10µs to 500µs).

Quick-Trip™ Circuit Breaker

Additionally, the SMH4803A provides a Quick-Trip feature that will cause the circuit breaker to trip immediately if the voltage drop across R_S exceeds V_{QCB}. The Quick-Trip level may be factory set to 60mV, 100mV (default), 200mV, or the feature may be disabled.

Current Regulation

The current regulation mode is an optional feature that provides a means to regulate current through the MOSFET for a programmable period of time. If enabled the device will start the internal timer when the voltage at CBSENSE exceeds 50mV. Also, it attempts to limit the voltage at CBSENSE to 60mV by regulating the VGATE output. The circuit breaker will trip if the over-current condition remains after the time-out. However, if CBSENSE drops below 50mV before the timer ends, the timer is reset and VGATE resumes normal operation. If the Quick-Trip level is exceeded then the device will bypass the current regulation timer and shut down immediately. The Current Regulation feature is disabled in the default configuration.

Non-Volatile Fault Latch

The SMH4803A also provides an optional nonvolatile fault latch (NVFL) circuit breaker feature. The nonvolatile fault latch essentially provides a programmable fuse on the circuit breaker. When enabled the nonvolatile fault latch will be set whenever the circuit breaker trips. Once set, it cannot be reset by cycling power or through the use of the RESET# pin.

NOTE: THE DEVICE REMAINS PERMANENTLY DISABLED UNTIL IT IS REPROGRAMMED AT THE FACTORY.

As long as the NVFL is set the FAULT# output will be driven active. The Non-Volatile Fault Latch feature is disabled in the default configuration.

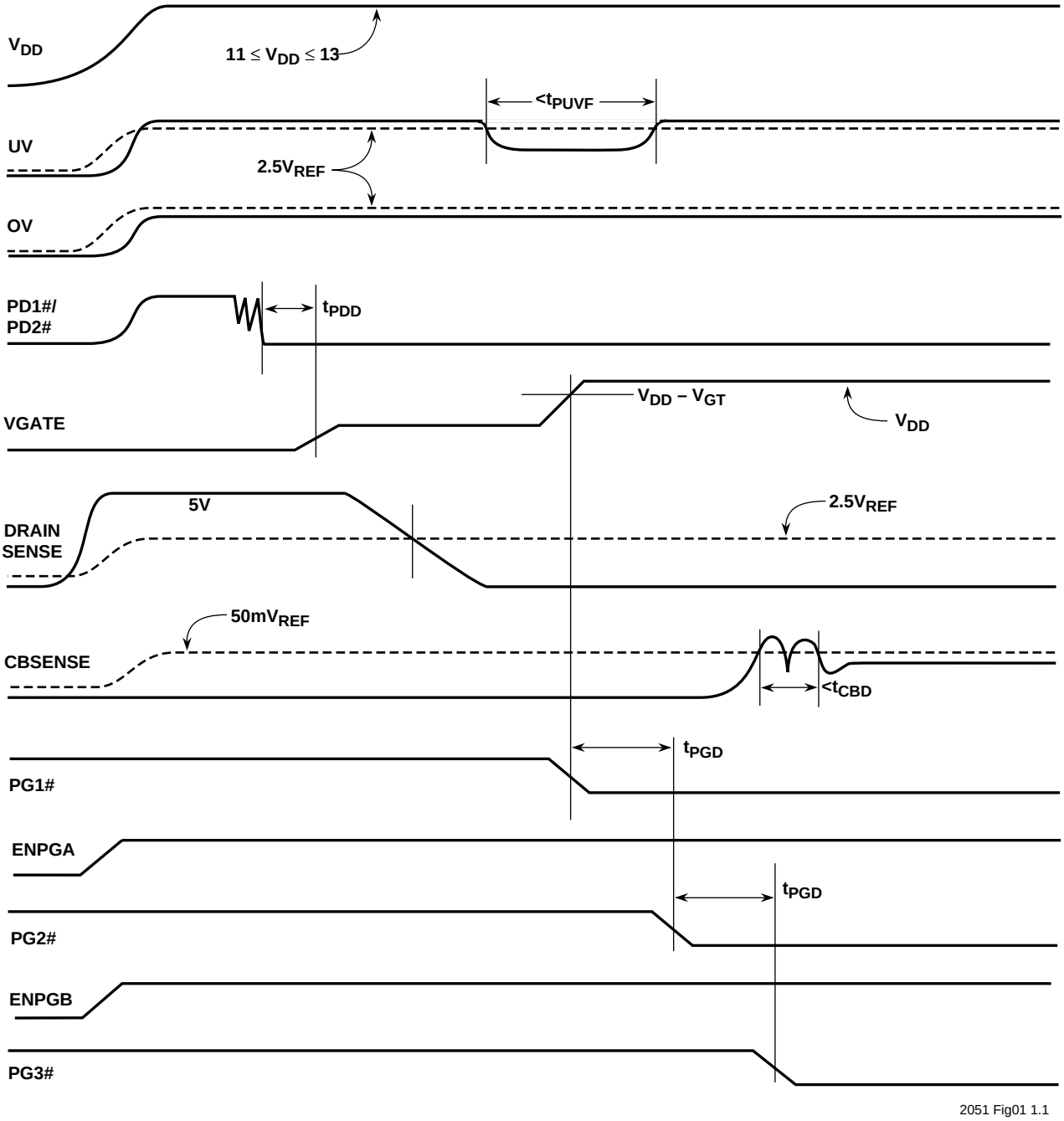

Figure 1. Complete Power On Timing Sequence

TIMING RELATIONSHIPS

Figure 1 illustrates some of the power on sequences, including the UV and OV differentials to their reference, and Power Good cascading.

Figures 2, 3, and 4 indicate the affect on the VGATE signal caused by different Circuit Breaker inputs. In Figure 2 RESET# and MODE are high; in Figure 3 MODE is low. Figure 4 shows the Quick Trip mode.

Resetting FAULT#

When the circuit breaker trips the VGATE output is turned off and FAULT# is driven low. There are two methods to reset the circuit breaker which are selectable with the MODE pin. When MODE is held high or left floating the circuit breaker is in the duty-cycle mode, and the breaker resets automatically after a time of t_{CYC}. When the MODE pin is held low the circuit breaker can be reset by bringing RESET# low. T_{PDD} after bringing RESET# back high again the VGATE output will attempt to restart the MOSFET slew control circuitry. In either case, cycling power to the board will also reset the circuit breaker. If the over current condition still exists after the MOSFET switches back on the circuit breaker will re-trip.

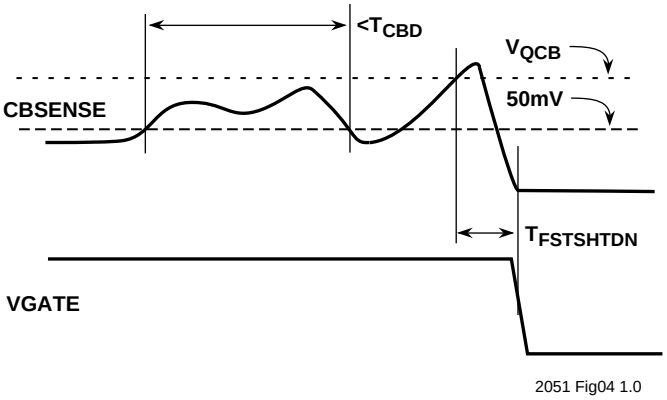

Figure 4. Circuit Breaker Timing — Quick Trip

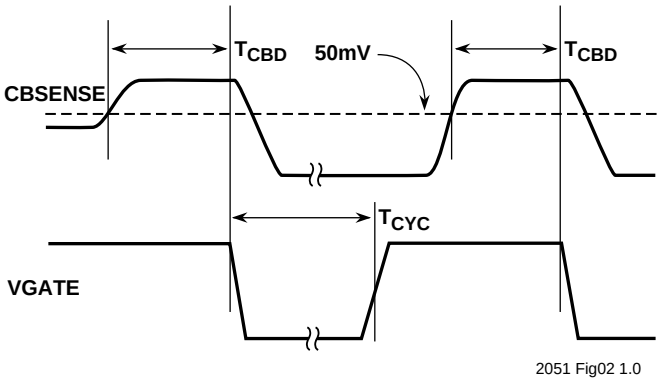

Figure 2. Circuit Breaker Cycle Mode, RESET# High

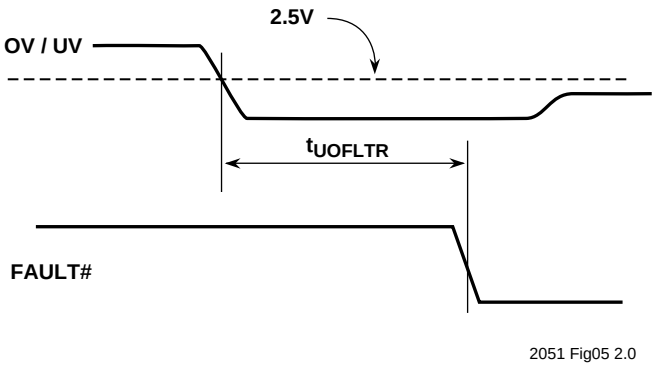

Figure 5. Under-/Over-Voltage Filter Timing

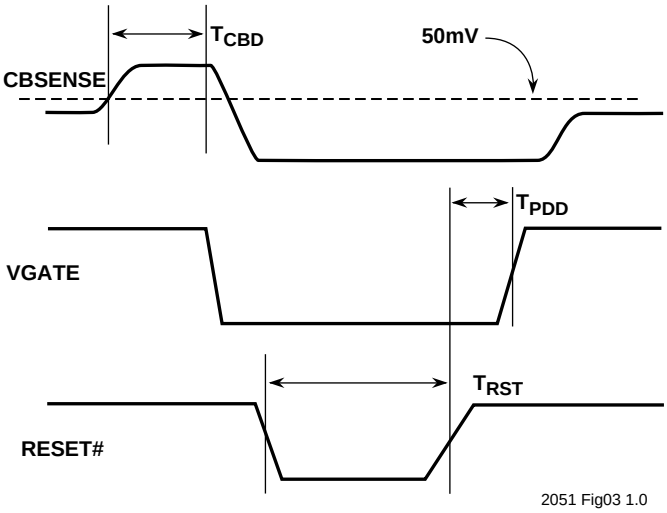

Figure 3. Circuit Breaker Timing — Reset Mode

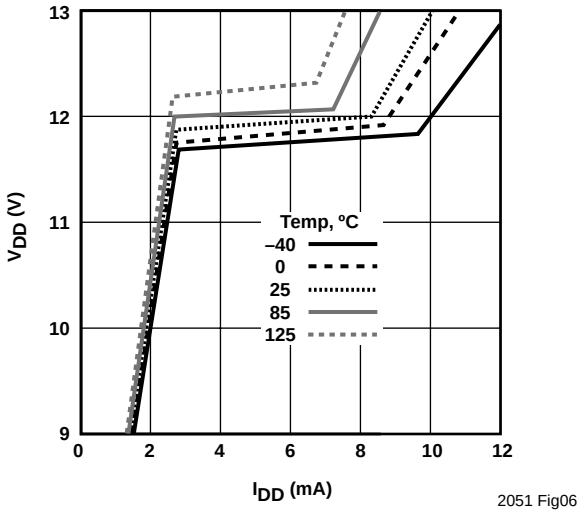

Figure 6. Effect of Temperature on Current Consumption Over Voltage Range

PROGRAMMABLE FEATURES

The SMH4803A has programmable time and voltage functions that can be fine-tuned for a wide variety of applications. Because of this a manufacturer can use a common part type across a wide range of boards that are used on a common host but have different electrical loads, power-on timing requirements, host voltage monitoring needs, *etc*. This ability shifts the focus of design away from designing a new power interface for each board to concentrating on the value added back-end logic. Because the programming is done at final test all combinations (all 128 possibilities) are readily available as off the shelf stock items.

Pin Detect

The Pin Detect function can be enabled or disabled.

Circuit Breaker Delay

The circuit breaker delay defines the period of time the voltage drop across R_S is greater than 50mV but less than V_{QCB} before the VGATE output will be shut down. This is effectively a filter to prevent spurious shutdowns of VGATE.

Power Good Delay

The PG delay timer that controls the delay from PG1# to PG2#, and PG2# to PG3# being asserted.

Quick-Trip Circuit Breaker Threshold

This is the threshold voltage drop across R_S that is placed between V_{SS} and CBSENSE.

Symbol	Description	Min.	Typ.	Max.	Units
t_{CBD}	50mV Circuit Breaker Delay (filter)		400		µs
			150		µs
			50 *		µs
			5		µs
t_{PGD}	Programmable Power Good Delay (PG1 to PG2, PG2 to PG3)		50		µs
			250		µs
			500		µs
			1.5		ms
			5 *		ms
			20		ms
			80		ms
			160		ms
$t_{FSTSHTDN}$	Fast Shut Down delay from fault to VGATE off		200		ns
t_{CYC}	Circuit breaker cycle mode Cycle time		2.5 *		s
			5		s
t_{RST}	RESET# pulse width	200			ns
t_{PUVF}	Programmable Under-Voltage filter		Off *		—
			5		ms
			80		ms
			160		ms
t_{PDD}	Programmable Pin Detect Delay		0.5		ms
			5		ms
			80 *		ms
			160		ms

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Note: * Denotes default configuration setting

APPLICATIONS

Operating at High Voltages

The breakdown voltage of the external active and passive components limits the maximum operating voltage of the SMH4803A hot-swap controller. Components that must be able to withstand the full supply voltage are: the input and output decoupling capacitors, the protection diode in series with the DRAIN SENSE pin, the power MOSFET switch and the capacitor connected between its drain and gate, the high-voltage transistors connected to the power good outputs, and the dropper resistor connected to the controller's V_{DD} pin.

Over-Voltage and Under-Voltage Resistors

In the following examples, the three resistors, R1, R2, and R3, connected to the OV and UV inputs, must be capable of withstanding the maximum supply voltage of several hundred volts. The trip voltage of the UV and OV inputs is 2.5V relative to V_{SS}. As the input impedance of UV and OV is very high, large value resistors can be used in the resistive divider. The divider resistors should be high stability, 1% metal-film resistors to keep the under-voltage and over-voltage trip points accurate.

Telecom Design Example

A hot-swap telecom application may use a 48V power supply with a –25% to +50% tolerance (*i.e.*, the 48V supply can vary from 36V to 72V). The formulae for calculating R1, R2, and R3 follow.

First a peak current, ID_{MAX}, must be specified for the resistive network. The value of the current is arbitrary, but it can't be too high (self-heating in R3 will become a problem), or too low (the value of R3 becomes very large, and leakage currents can reduce the accuracy of the OV and UV trip points). The value of ID_{MAX} should be ≥200µA for the best accuracy at the OV and UV trip points. A value of 250µA for ID_{MAX} will be used to illustrate the following calculations.

With V_{OV} (2.5V) being the over-voltage trip point, R1 is calculated by the formula:

$$R1 = \frac{V_{OV}}{ID_{MAX}}.$$

Substituting:

$$R1 = \frac{2.5V}{250\mu A} = 10k\Omega.$$

Next the minimum current that flows through the resistive divider, ID_{MIN}, is calculated from the ratio of minimum and maximum supply voltage levels:

$$ID_{MIN} = \frac{ID_{MAX} \times VS_{MIN}}{VS_{MAX}}.$$

Substituting:

$$ID_{MIN} = \frac{250\mu A \times 36V}{72V} = 125\mu A.$$

Now the value of R3 is calculated from ID_{MIN}:

$$R3 = \frac{VS_{MIN} - V_{UV}}{ID_{MIN}}.$$

V_{UV} is the under-voltage trip point, also 2.5V. Substituting:

$$R3 = \frac{36V - 2.5V}{125\mu A} = 268k\Omega.$$

The closest standard 1% resistor value is 267kΩ

Then R2 is calculated:

$$(R1 + R2) = \frac{V_{UV}}{ID_{MIN}},$$

or

$$R2 = \frac{V_{UV}}{ID_{MIN}} - R1.$$

Substituting:

$$R2 = \frac{2.5V}{125\mu A} - 10k\Omega = 20k\Omega - 10k\Omega = 10k\Omega.$$

An Excel spread sheet is available on Summit's website (***www.summitmicro.com***) to simplify the resistor value calculations and tolerance analysis for R1, R2, and R3.

Dropper Resistor Selection

The SMH4803A is powered from the high-voltage supply via a dropper resistor, R_D. The dropper resistor must provide the SMH4803A (and its loads) with sufficient operating current under minimum supply voltage condi-

tions, but must not allow the maximum supply current to be exceeded under maximum supply voltage conditions.

The dropper resistor value is calculated from:

$$R_D = \frac{VS_{MIN} - V_{DD_{MAX}}}{I_{DD} + I_{LOAD}},$$

where VS_{MIN} is the lowest operating supply voltage, V_{DDMAX} is the upper limit of the SMH4803A supply voltage, I_{DD} is minimum current required for the SMH4803A to operate, and I_{LOAD} is any additional load current from the 2.5V and 5V outputs and between V_{DD} and V_{SS}.

The min/max current limits are easily met using the dropper resistor, except in circumstances where the input voltage may swing over a very wide range (*e.g.*, input varies between 20V and 100V). In these circumstances it may be necessary to add an 11V zener diode between V_{DD} and V_{SS} to handle the wide current range. The zener voltage should be below the nominal regulation voltage of the SMH4803A so that it becomes the primary regulator.

MOSFET V_{DS}(ON) Threshold

The drain sense input on the SMH4803A monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. When the MOSFET's V_{DS} is below the user-defined threshold the MOSFET switch is considered to be ON. The $V_{DS}(ON)_{THRESHOLD}$ is adjusted using the resistor, R_T, in series with the drain sense protection diode. This protection, or blocking, diode prevents high voltage breakdown of the drain sense input when the MOSFET switch is OFF. A low leakage MMBD1401 diode offers protection up to 100V. For high voltage applications (up to 500V) the Central Semiconductor CMR1F-10M diode should be used. The $V_{DS}(ON)_{THRESHOLD}$ is calculated from:

$$V_{DS}(ON)_{THRESHOLD} = V_{SENSE} - (I_{SENSE} \times R_T) - V_{DIODE},$$

where V_{DIODE} is the forward voltage drop of the protection diode. The $V_{DS}(ON)_{THRESHOLD}$ varies over temperature due to the temperature dependence of V_{DIODE} and I_{SENSE}. The calculation below gives the $V_{DS}(ON)_{THRESHOLD}$ under the worst case condition of 85°C ambient. Using a 68kΩ resistor for R_T gives:

$$V_{DS}(ON)_{THRESHOLD} = 2.5V - (15\mu A \times 68k\Omega) - 0.5V = 1V.$$

The voltage drop across the MOSFET switch and sense resistor, V_{DSS}, is calculated from:

$$V_{DSS} = I_D (R_S + R_{ON}),$$

where I_D is the MOSFET drain current, R_S is the circuit breaker sense resistor, and R_{ON} is the MOSFET on resistance.

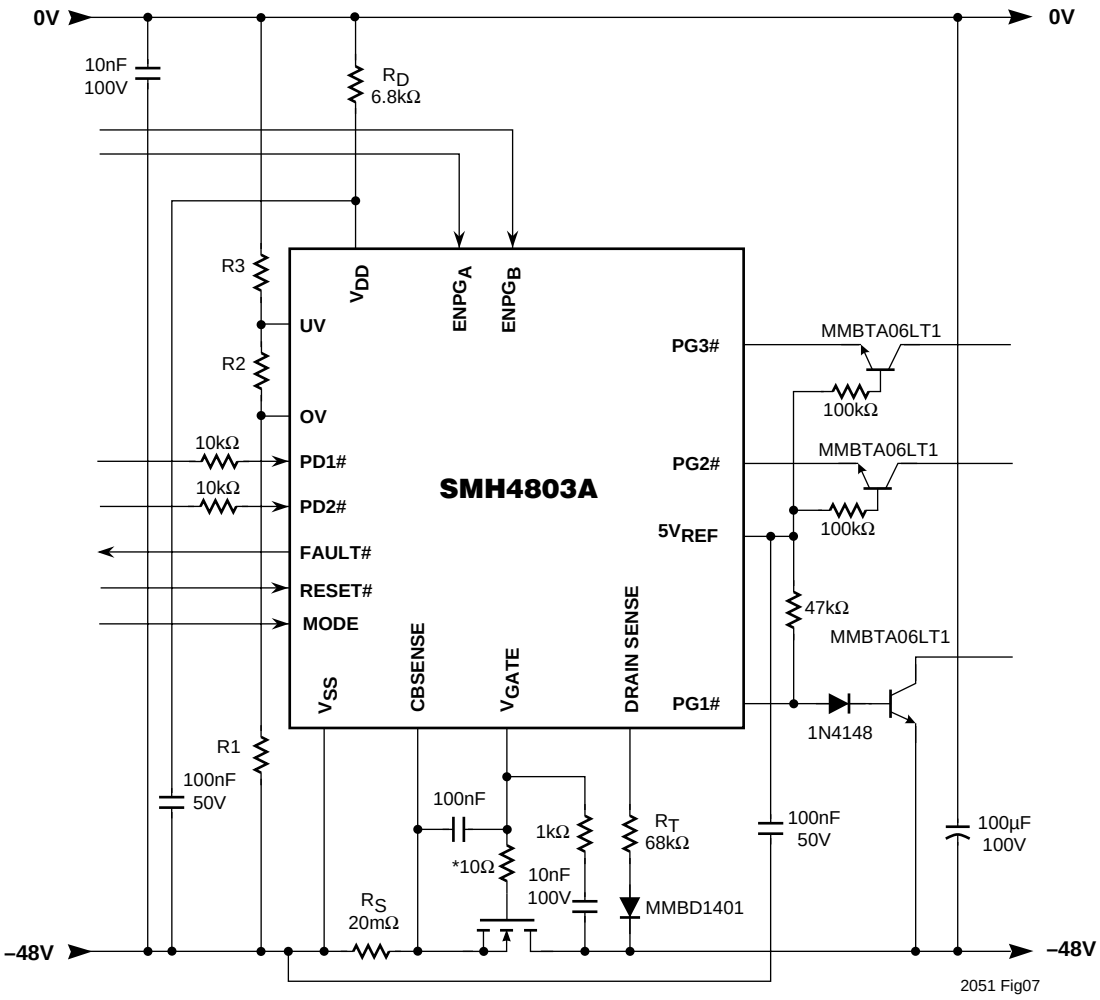

Figure 7. Changing Polarity of Power Good Output PG1#

Note: Figures 7 through 11 — the *10Ω resistor must be located as close as possible to the MOSFET

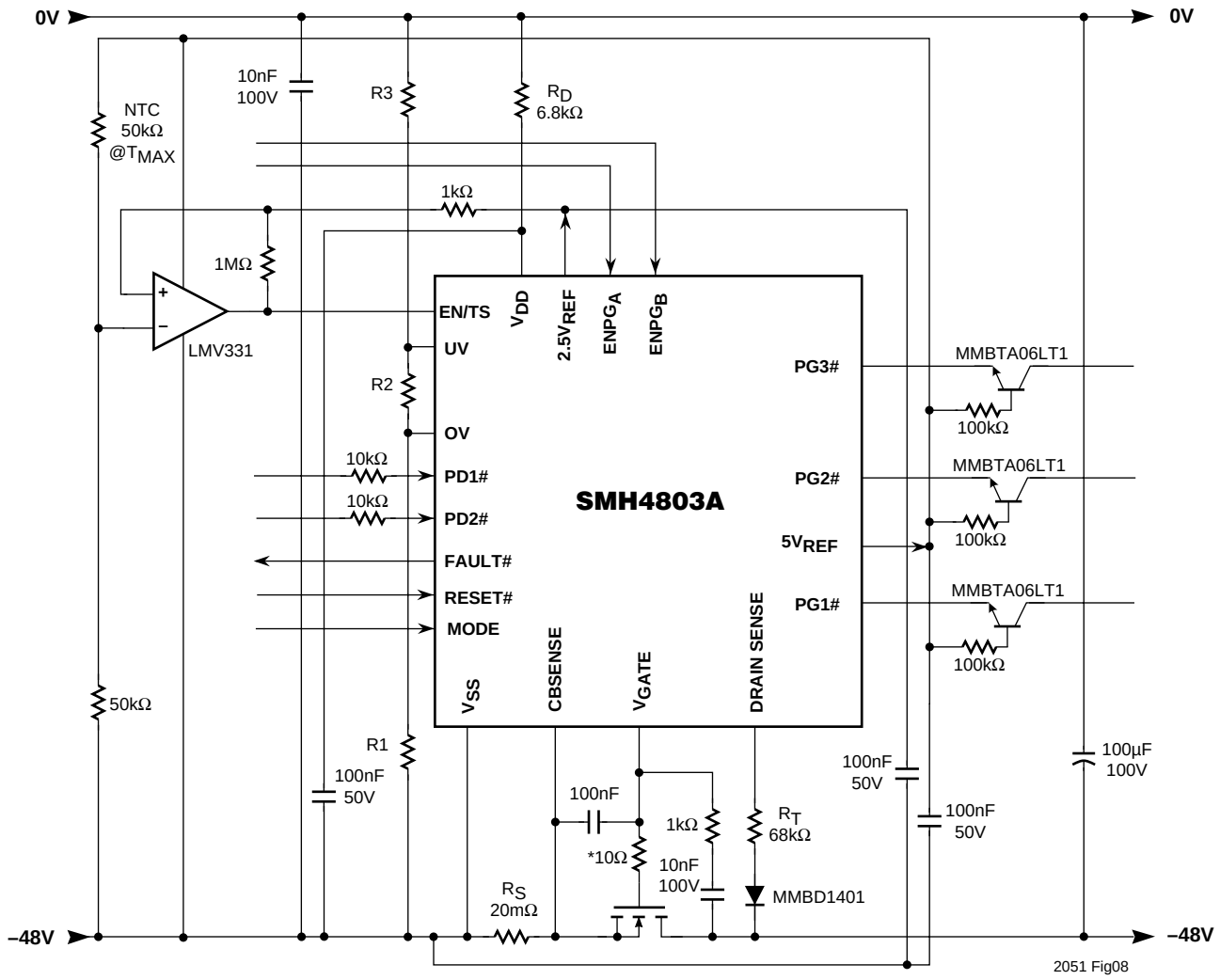

Figure 8. Overtemperature Shutdown

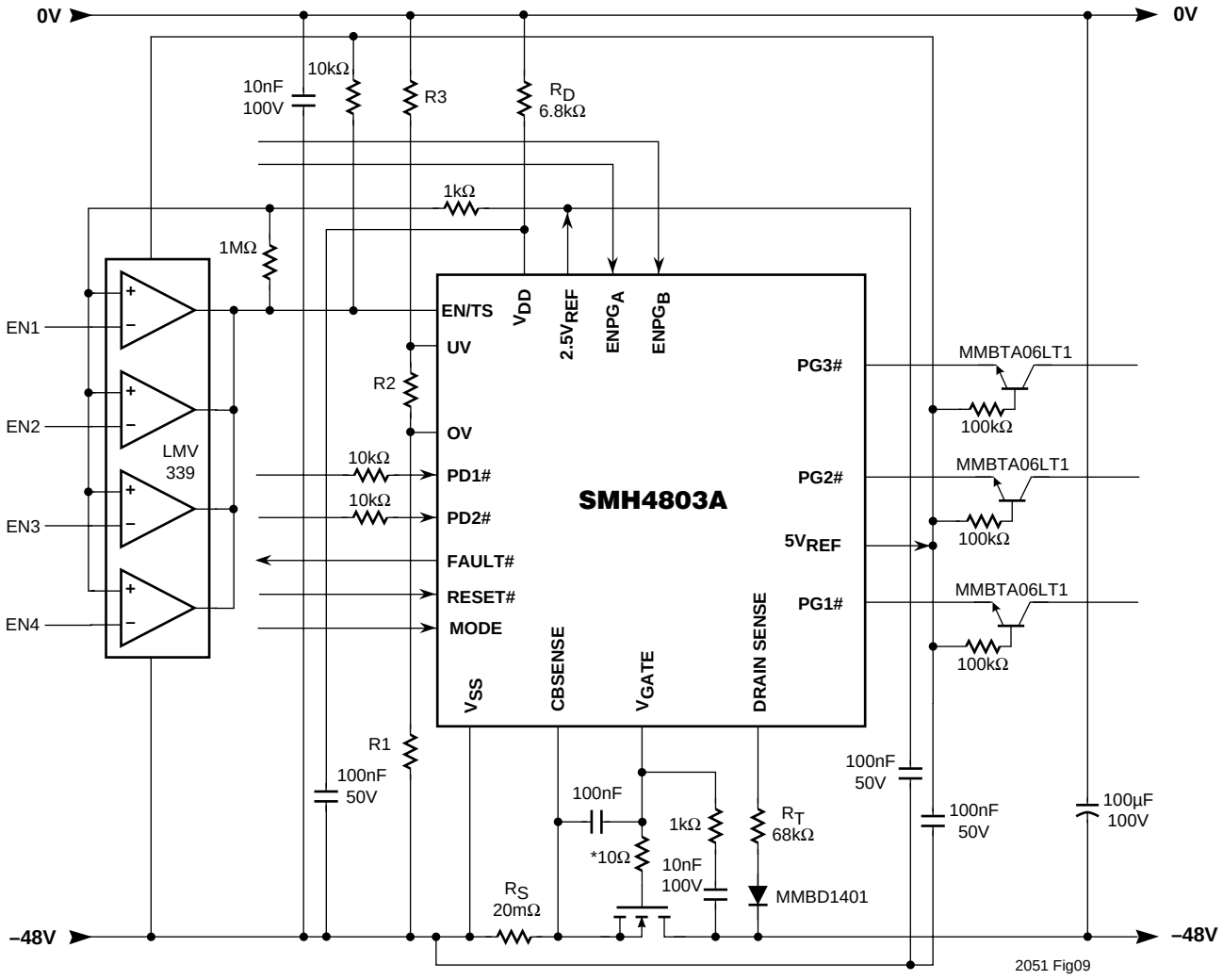

Figure 9. Expanding Input Monitoring Capability

Note: Figures 7 through 11 — the *10Ω resistor must be located as close as possible to the MOSFET

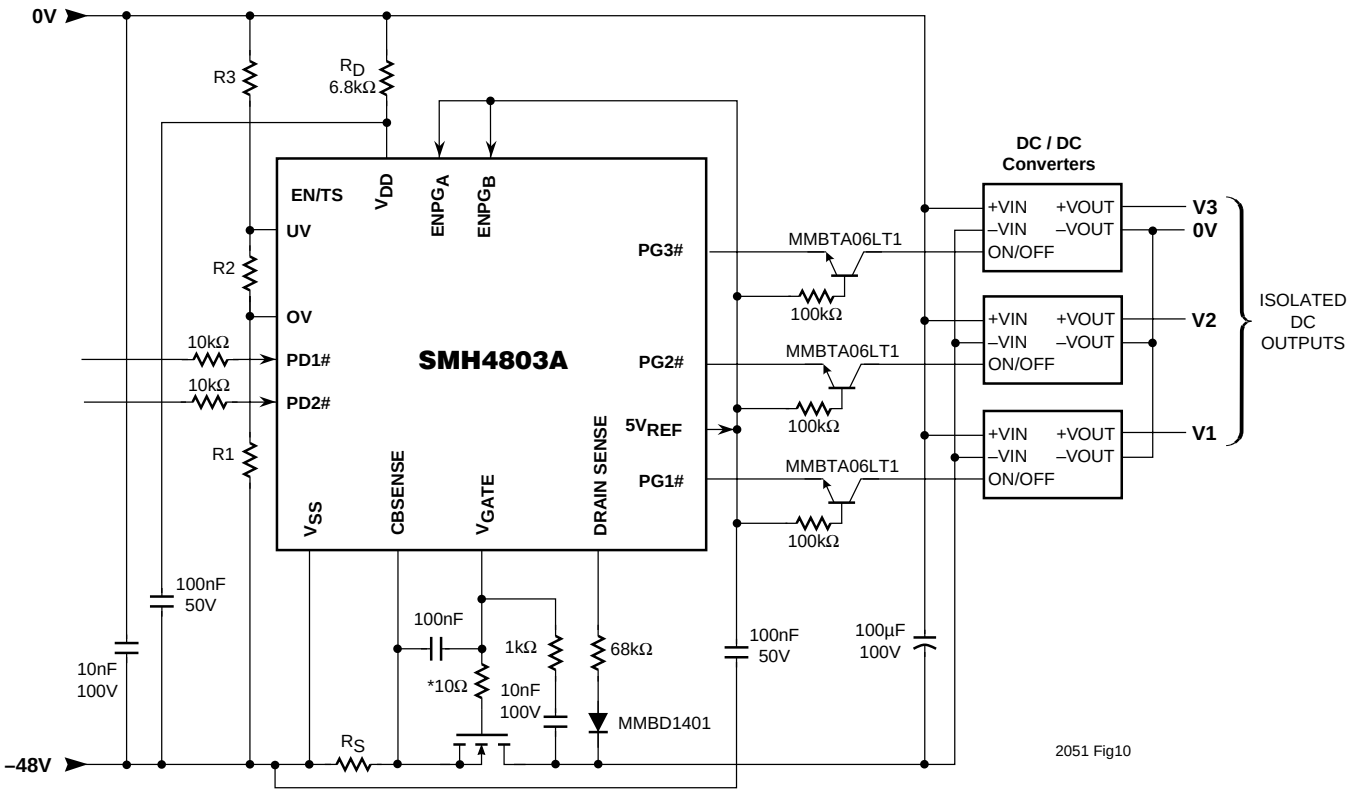

Figure 10. Typical Application Sequencing Three DC/DC Converters

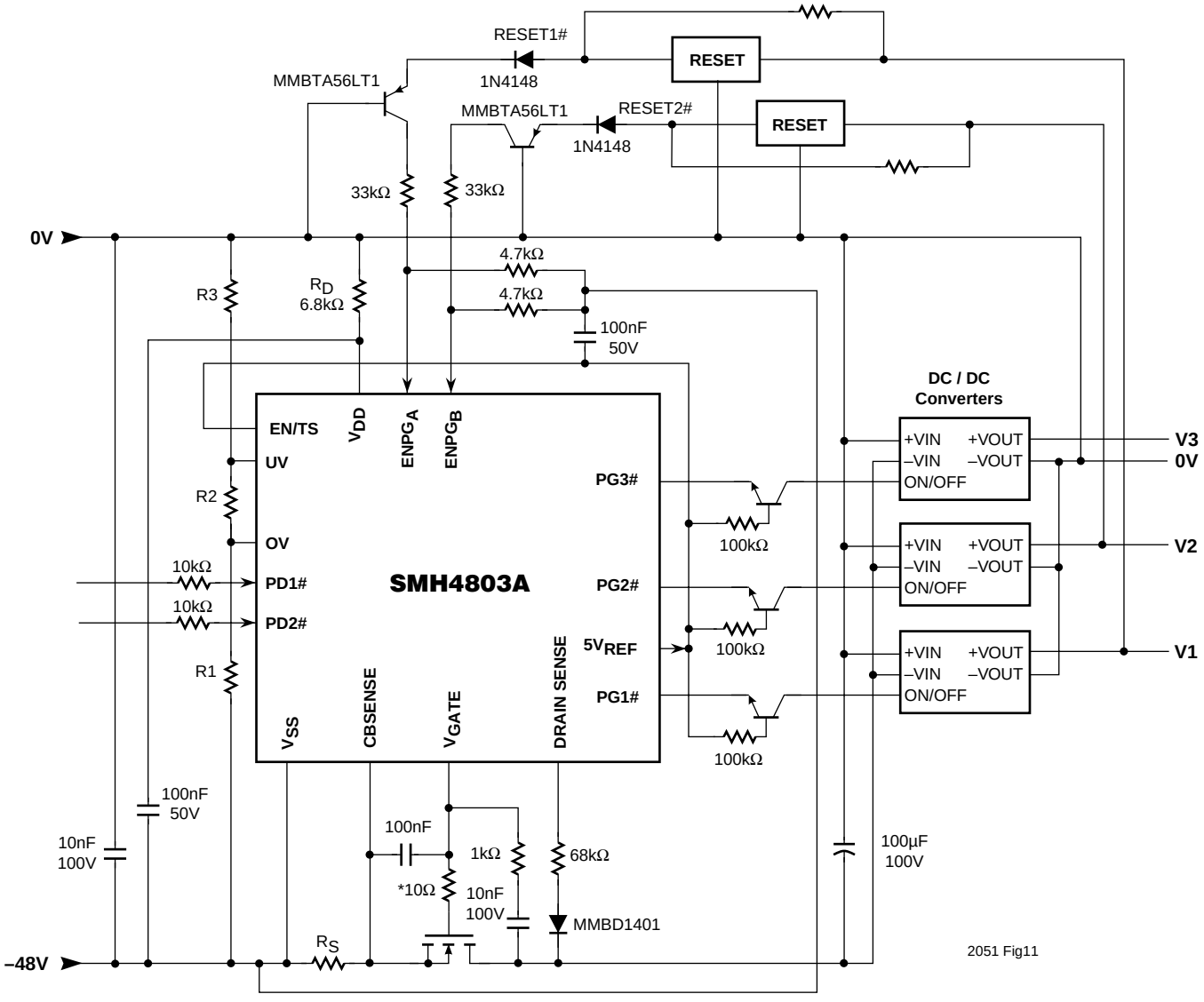

Figure 11. Sequencing Converters with Common I/O Ground and Voltage Feedback

Note: Figures 7 through 11 — the *10Ω resistor must be located as close as possible to the MOSFET

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20 PIN SOIC PACKAGE

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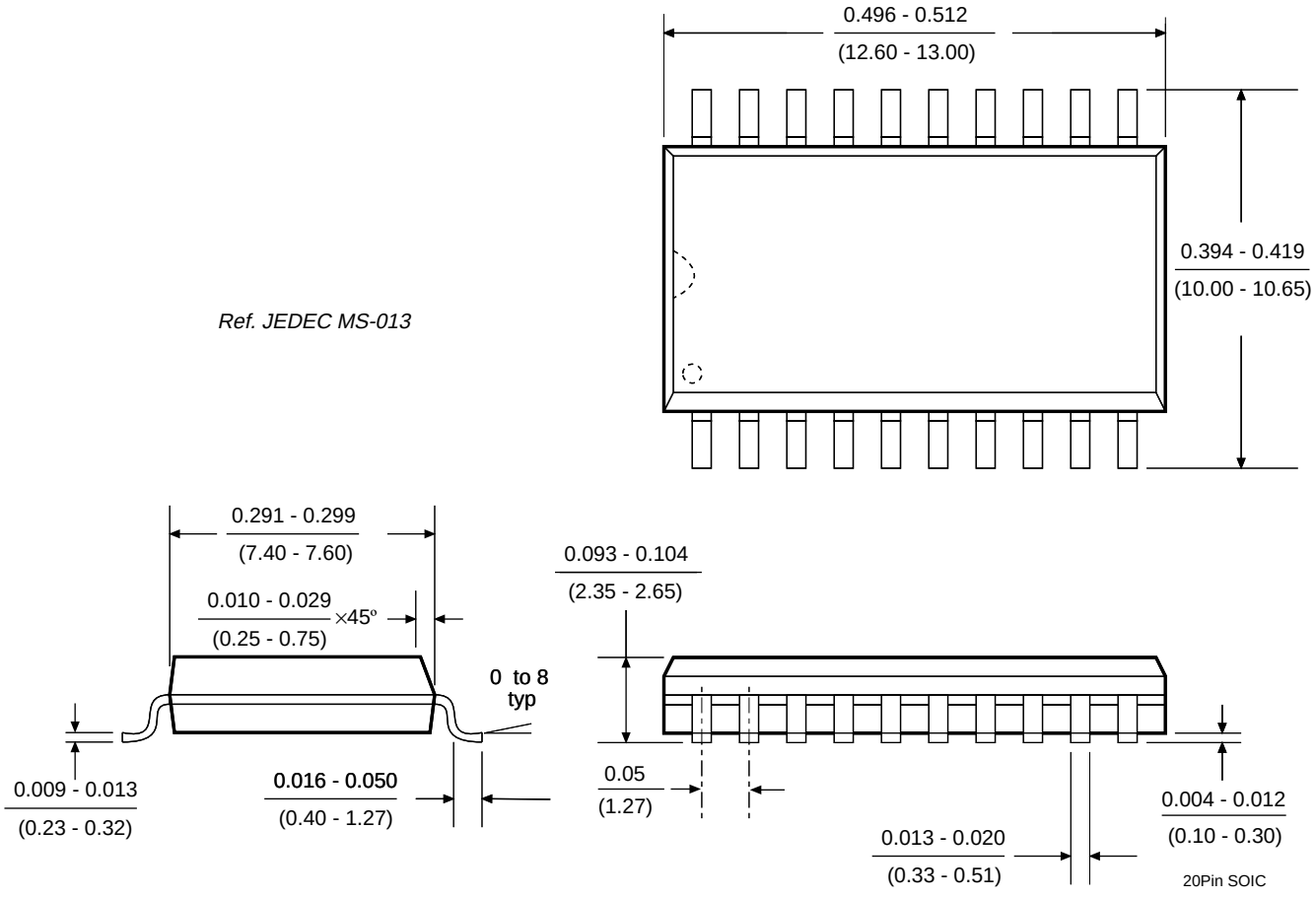
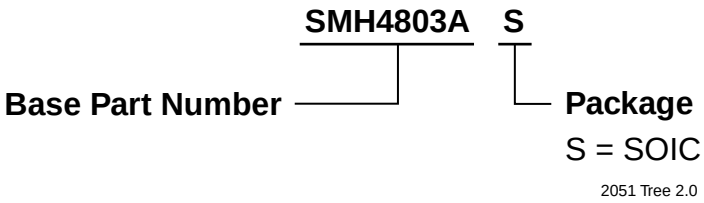


ORDERING INFORMATION



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