

REVISIONS

REV	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes in table I. Update boilerplate throughout.	92-02-19	<i>Am Palkis</i>

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A							
	SHEET	1	2	3	4	5	6	7	8	9	10	11								
PMIC N/A	PREPARED BY <i>Larry T. Sande</i>	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444																		
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin	MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY, TTL, OCTAL BUS TRANSCEIVERS AND REGISTERS, MONOLITHIC SILICON																		
	APPROVED BY Mike Frye																			
	DRAWING APPROVAL DATE 88-10-03	SIZE A	CAGE CODE 67268	5962-88753																
	REVISION LEVEL A	SHEET																	1	

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5962-E316

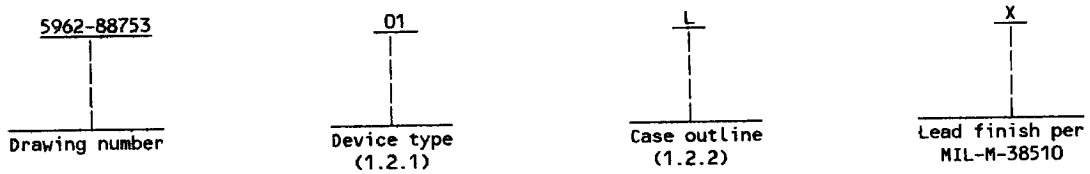
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

查询"5962-88753013A"供应商

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54AS651	Octal bus transceivers and registers (inverting), with three-state output

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range:	
Control inputs - - - - -	-1.2 V at -18 mA to +7.0 V
I/O ports - - - - -	-1.2 V at -18 mA to +5.5 V
Storage temperature range - - - - -	-65°C to +150°C
Maximum power dissipation (P_D) ^{1/} - - - - -	1072.5 mW
Lead temperature (soldering, 10 seconds) - - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC}) - - - - -	See MIL-M-38510, appendix C
Junction temperature (T_J)- - - - -	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) - - - - -	+4.5 V dc minimum to +5.5 V dc maximum.
Minimum high level input voltage (V_{IH}) - - - - -	2.0 V dc
Maximum low level input voltage (V_{IL}) - - - - -	0.8 V dc
Case operating temperature range (T_C) - - - - -	-55°C to +125°C
Pulse duration (t_W):	
CBA or CAB high - - - - -	6.0 ns minimum
CBA or CAB low - - - - -	7.0 ns minimum
Setup time before CAB rising or CBA rising (t_s) - - - - -	7.0 ns minimum
Hold time after CAB rising or CBA rising (t_h) - - - - -	0 ns minimum

^{1/} Maximum power dissipation is defined as $V_{CC} \times I_{CC}$, and must withstand the added P_D due to short circuit test; e.g., I_O .

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	1/ Group A subgroups	Limits		Unit	
				Min	Max		
High level output voltage	V _{OH}	V _{CC} = 4.5 V V _{IL} = 0.8 V V _{IH} = 2.0 V 2/	I _{OH} = -2.0 mA	1, 2, 3	2.5	V	
					2.4		
					2.0		
Low level output voltage	V _{OL}	V _{CC} = 4.5 V V _{IL} = 0.8 V V _{IH} = 2.0 V	I _{OL} = 32 mA 2/	1, 2, 3	0.5	V	
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA		1, 2, 3	-1.2	V	
Low level input current	I _{IL}	V _{CC} = 5.5 V V _{IN} = 0.4 V Unused inputs = 4.5 V	Control inputs	1, 2, 3		-0.5	mA
			A or B ports				
High level input current	I _{IH1}	V _{CC} = 5.5 V V _{IN} = 2.7 V Unused inputs = 0.0 V	Control inputs	1, 2, 3		20	μA
			A or B ports				
	I _{IH2}	V _{CC} = 5.5 V Unused inputs = 0.0 V	V _{IN} = 7.0 V Control inputs	1, 2, 3		0.1	mA
		V _{IN} = 5.5 V A or B ports	0.1				
Output current	I _O	V _{CC} = 5.5 V V _{OUT} = 2.25 V	3/	1, 2, 3	-30	-112	mA
Supply current	I _{CC}	V _{CC} = 5.5 V	Outputs high	1, 2, 3		185	mA
			Outputs low			195	
			Outputs disabled			195	
Functional tests		See 4.3.1c V _{CC} = 4.5 V, 5.5 V		7, 8			
Maximum clock frequency 4/	f _{MAX}	V _{CC} = 4.5 V and 5.5 V C _L = 50 pF R ₁ = 500Ω R ₂ = 500Ω See figure 3		9, 10, 11	75		MHz
Propagation delay time, from CBA or CAB to A or B	t _{PLH1}	5/		9, 10, 11	2	11	ns
	t _{PHL1}			9, 10, 11	2	10	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

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Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay time, from A or B to B or A	t _{PLH2}	V _{CC} = 4.5 V and 5.5 V C _L = 50 pF R ₁ = 500Ω R ₂ = 500Ω See figure 3	9, 10, 11	2	12	ns
	t _{PHL2}					
Propagation delay time, from SBA or SAB to A or B 6/	t _{PLH3}		9, 10, 11	2	15	ns
	t _{PHL3}					
Output enable time, from GBA to A	t _{PZH1}		9, 10, 11	2	11	ns
	t _{PZL1}					
Output disable time, from GBA to A	t _{PHZ1}		9, 10, 11	2	10	ns
	t _{PLZ1}					
Output enable time, from GAB to B	t _{PZH2}		9, 10, 11	3	12	ns
	t _{PZL2}					
Output disable time, from GAB to B	t _{PHZ2}		9, 10, 11	2	11	ns
	t _{PLZ2}					

- 1/ Unused inputs that do not directly control the pin under test must be ≥ 2.5 V or ≤ 0.4 V. Unused inputs shall not exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.
- 2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.
- 3/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}. Not more than one output shall be tested at one time and the duration of the test condition shall not exceed 1 second.
- 4/ This parameter shall be, as a minimum, tested initially and after any process or design changes which may affect the parameter, otherwise, it is guaranteed to the specified limits in table I for this device.
- 5/ Propagation delay limits are based on single output switching. Unused outputs = 3.5 V or ≤ 0.3 V.
- 6/ These parameters are measured with the internal output state of the storage registers opposite to that of the bus input.

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Case outlines	L and K	3
Terminal number	Terminal symbol	
1	CAB	NC
2	SAB	CAB
3	GAB	SAB
4	A1	GAB
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	A8	A6
12	GND	A7
13	B8	A8
14	B7	GND
15	B6	NC
16	B5	B8
17	B4	B7
18	B3	B6
19	B2	B5
20	B1	B4
21	GBA	B3
22	SBA	NC
23	CBA	B2
24	V _{CC}	B1
25	---	GBA
26	---	SBA
27	---	CBA
28	---	V _{CC}

NC = No connection

FIGURE 1. Terminal Connections.

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Inputs						Data I/O		Operation or function
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B data
L	H	↑	↑	X	X			
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, hold B
H	H	↑	↑	X**	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, store B
L	L	↑	↑	X	X**	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time \bar{B} data to A bus Stored \bar{B} data to A bus
L	L	X	H or L	X	H			
H	H	X	X	L	X	Input	Output	Real-time \bar{A} data to B bus Stored \bar{A} data to B bus
H	H	H or L	X	H	X			
H	L	H or L	H or L	H	H	Output	Output	Stored \bar{A} data to B bus and stored B data to A bus

H = High voltage level
 L = Low voltage level
 X = Irrelevant
 ↑ = Transition from low to high level
 * = The data output functions may be enabled or disabled by various signals at the GAB or $\bar{G}BA$ inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
 ** = Select control = L; clocks can occur simultaneously.
 Select control = H; clocks must be staggered in order to load both registers.

FIGURE 2. Truth table.

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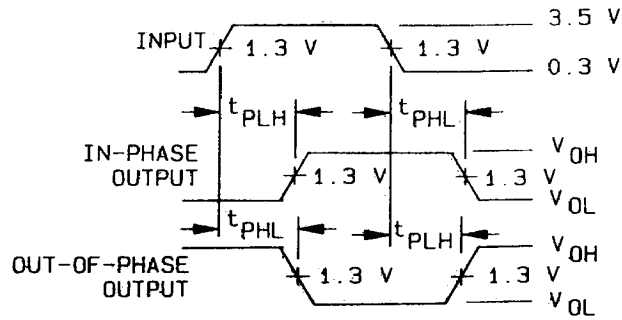
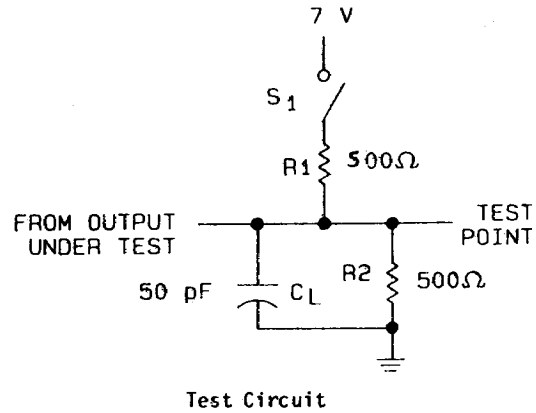
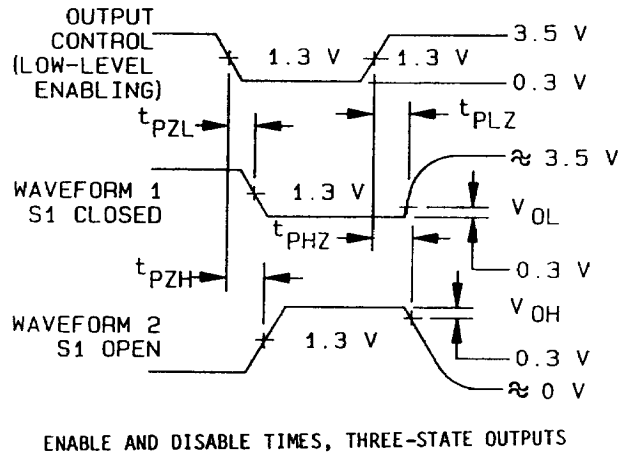


FIGURE 3. Test circuit and switching waveforms.

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ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics: $PRR \leq 10$ MHz, duty cycle = 50%, $t_r = t_f = 3 \pm 1$ ns.
3. The outputs are measured one at a time with one input transition per measurement.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. When measuring propagation delay items of 3-state outputs, switch S1 is open.

FIGURE 3. Test circuit and switching waveforms - Continued.

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3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

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3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = +125^\circ\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

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MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

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