



L6750

2 to 5 phase controller with LTB technology[®] for VR11.x and AMD6bit CPUs featuring I2C interface

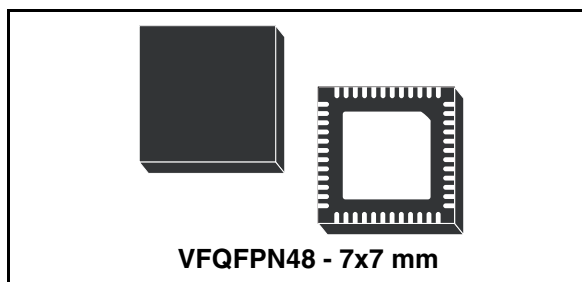
Data Brief

Features

- LTB technology[®] to enhance load transient
- I2C power manager
- 2 to 5 scalable phase operation
- Dual-edge asynchronous architecture
- Flexible driver support
- PSI# input and IMON output for VR11.1
- 7/8 bit programmable output - VR10/11.x DAC
- 6 bit programmable output - AMD AM2 DAC
- 0.5 % output voltage accuracy
- Full-differential current sense across inductor DCR
- Integrated remote sense buffer
- Adaptive Voltage Positioning (AVP)
- Feedback disconnection protection
- Adjustable oscillator from 100 kHz to 1 MHz
- LSLess startup to manage pre-biased output
- Programmable Soft-start
- Threshold sensitive enable pin for VTT Sensing
- VFQFPN48 7x7 mm package

Applications

- High-Current VRM / VRD for desktop / server / workstation CPUs
- Graphic cards
- Low-voltage, high-current power supplies
- High-density DC DC converters



Description

L6750 is a two-to-five phase controller designed to power Intel's most demanding PIV Processors and, most in general, low-voltage, high-current power supplies. The device features LTB technology[®] to provide the fastest response to load transients thus minimizing the output filter composition.

L6750 features Power Manager I2C to implement overspeeding and other power management options without using any external component.

The device embeds selectable DAC: Output Voltage is programmable up to 1.6000V (Intel VR10 and VR11.x DACs) or up to 1.550V (AMD 6bit DAC) managing DVID transitions with $\pm 0.5\%$ output voltage accuracy over line, load and temperature variations.

The device assures fast protection against load over current, under / over voltage and feedback disconnections. Low-Side-Less start-up allows soft-start over pre-biased output avoiding dangerous current return through the main inductors as well as negative spike at the load side. L6750 is available in VFQFPN48 7x7 mm package

Table 1. Device summary

Order code	Package	Packing
L6750	VFQFPN48	Tube
L6750TR	VFQFPN48	Tape and reel

1 Revision history

Table 1. Document revision history

Date	Revision	Changes
14-Feb-2008	1	Initial release.

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