FAIRCHILD SEMICONDUCTOR™

September 1983
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MM74HC423A
Dual Retriggerable Monostable Multivibrator

General Description

The 74HC423A high speed monostable multivibrators (one shots) utilize advanced silicon-gate CMOS technology. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken LOW resets the one shot. The MM74HC423A cannot be triggered from clear.

The MM74HC423A is retriggerable. That is, it may be triggered repeatedly while its outputs are generating a pulse and the pulse will be extended.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: PW = (R_{EXT}) (C_{EXT}); where PW

is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

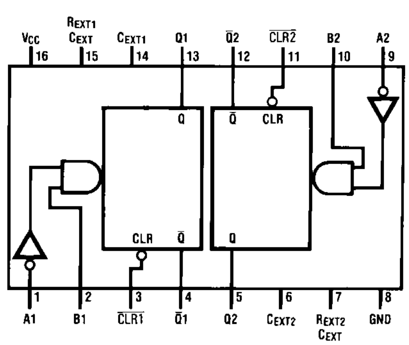
- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 µA maximum (74HC Series)
- Low input current: 1 µA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs allow rise and fall times to be as slow as one second

Ordering Code:

Order Number	Package Number	Package Description
MM74HC423AM (Note 1)	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC423ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC423AMTC (Note 1)	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC423AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

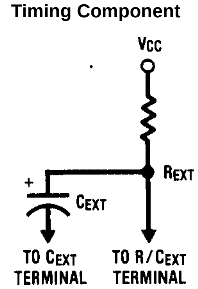
Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



Top View

Timing Component



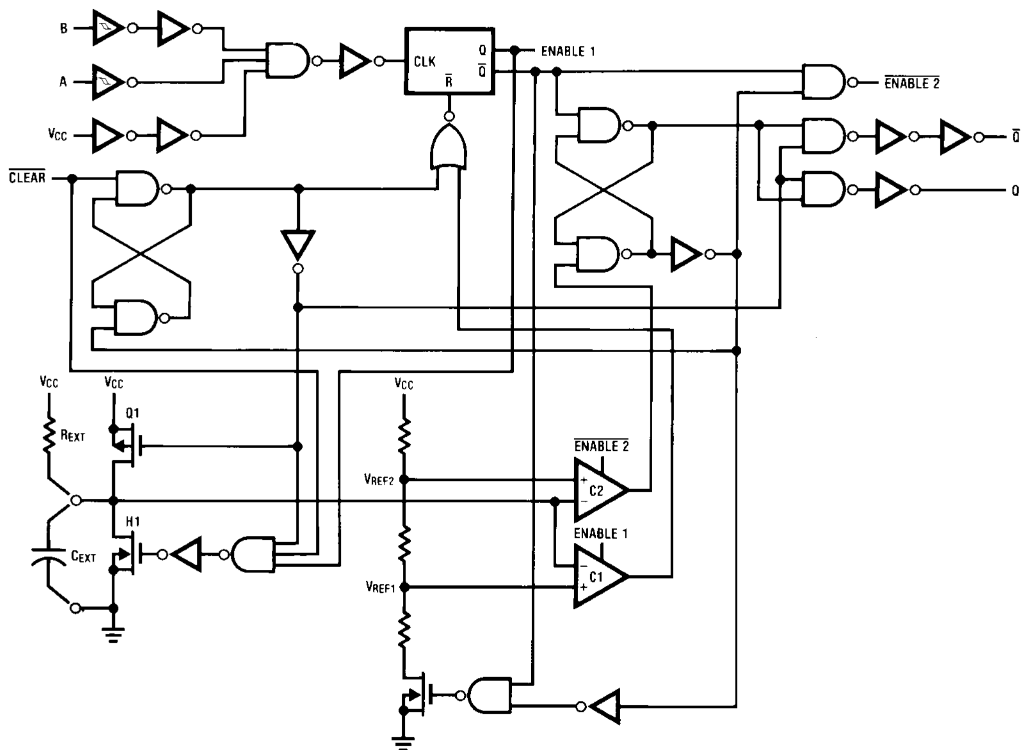
Note: Pin 6 and Pin 14 must be hard-wired to GND.

Truth Table

Inputs			Outputs	
$\overline{\text{Clear}}$	A	B	Q	$\overline{\text{Q}}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⊔ = One LOW Level Pulse
X = Irrelevant

Logic Diagram



Theory of Operation

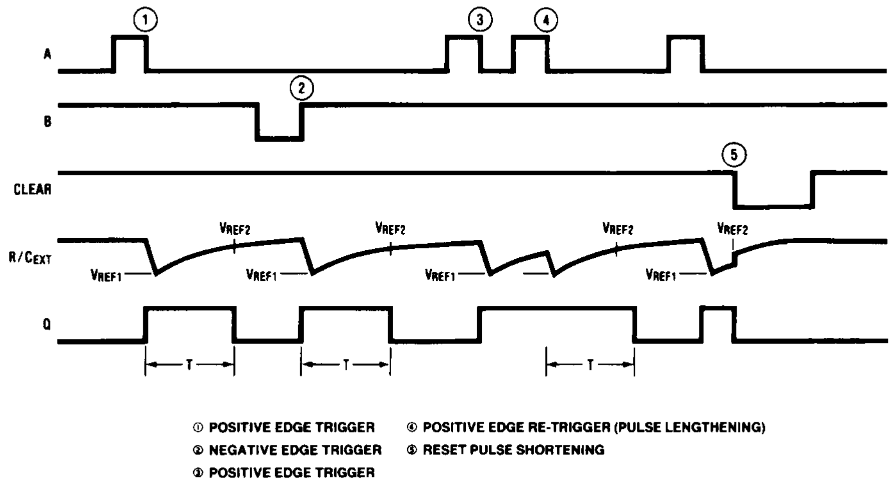


FIGURE 1.

TRIGGER OPERATION

As shown in Figure 1 and the Logic Diagram before an input trigger occurs, the one-shot is in the quiescent state with the Q output LOW, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N11. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns OFF. Comparator C1 then turns OFF while at the same time comparator C2 turns on. With transistor N1 OFF, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT}equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes LOW) while at the same time disabling comparator C2. This ends the timing cycle with the one-shot in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}2.)

It should be noted that in the quiescent state $C_{EXT}$is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "OFF" with the total device current due only to reverse junction leakages. An added feature of the MM74HC423A is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MM74HC423A is retriggered if a valid trigger occurs 3 followed by another trigger 4 before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin or has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated 4, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC}. The Q output will remain high until time T, after the last valid retrigger.

Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit, the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

$$t_{rr} = 20 + \frac{187}{V_{CC} - 0.7} + \frac{565 + (0.256\ V_{CC})\ C_X}{(V_{CC} - 0.7)^2}\ \text{ns}$$

Another removal/retrigger time occurs when a short clear pulse is used. Upon receipt of a clear, the one shot must charge the capacitor up to the upper trip point before the one shot is ready to receive the next trigger. This time is dependent on the capacitor used and is approximately:

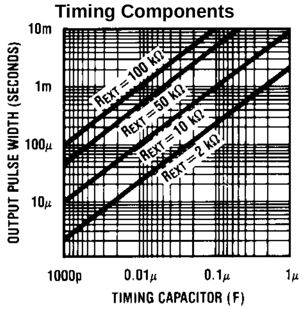
$$t_{rr} = 20 + \frac{187}{V_{CC} - 0.7} + \frac{565 + (0.256\ V_{CC})\ C_X}{(V_{CC} - 0.7)^2}\ \text{ns}$$

Theory of Operation (Continued)

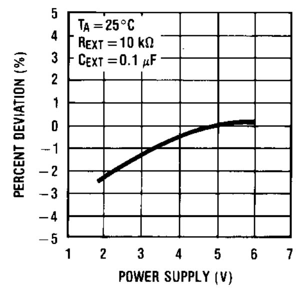
RESET OPERATION

These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 5. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held LOW, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

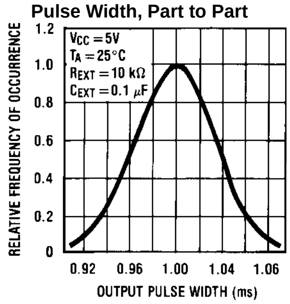
Typical Output Pulse Width vs. Timing Components



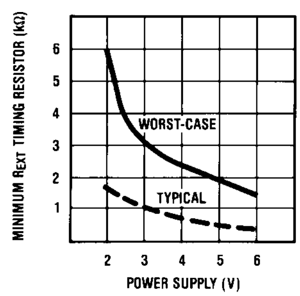
Typical 1ms Pulse Width Variation vs. Supply



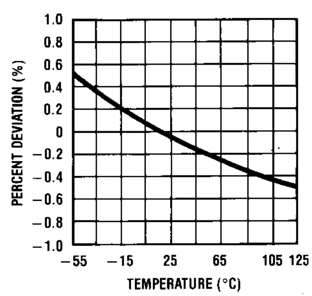
Typical Distribution of Output Pulse Width, Part to Part



Minimum R_{EXT} vs. Supply Voltage



Typical 1ms Pulse Width Variation vs. Temperature



Note: R and C are not subjected to temperature. The C is polypropylene.

Absolute Maximum Ratings (Note 2)

(Note 3)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Input Voltage (V_{IN})	–1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	–0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Power Dissipation (P_D)	
(Note 4)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	–40	+85	°C
Maximum Input Rise and Fall Time (Clear Input)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 2: Maximum Ratings are those values beyond which damage to the device may occur.

Note 3: Unless otherwise specified all voltages are referenced to ground.

Note 4: Power Dissipation Temperature Derating: Plastic "N" Package: –12mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		T_A = –40 to 85°C	T_A = –55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	
			6.0V		4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	
			6.0V		1.2	1.2	1.2	
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	
			6.0V	6.0	5.9	5.9	5.9	
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V		3.96	3.84	3.7	
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V		5.46	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	
			6.0V	0	0.1	0.1	0.1	
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4$ mA	4.5V		0.26	0.33	0.4	
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V		0.26	0.33	0.4	
I_{IN}	Maximum Input Current (Pins 7, 15)	$V_{IN} = V_{CC}$ or GND	5.0V		0.5	5.0	5.0	µA
I_{IN}	Maximum Input Current (all other pins)	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (standby)	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu A$	6.0V		8.0	80	160	µA
I_{CC}	Maximum Active Supply Current (per monostable)	$V_{IN} = V_{CC}$ or GND $R/C_{EXT} = 0.5V_{CC}$	2.0V	36	80	110	130	µA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 5: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guatanteed Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay, A, B to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT} = 28$ pF $R_{EXT} = 2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT} = 1000$ pF $R_{EXT} = 10$ kΩ	10		µs

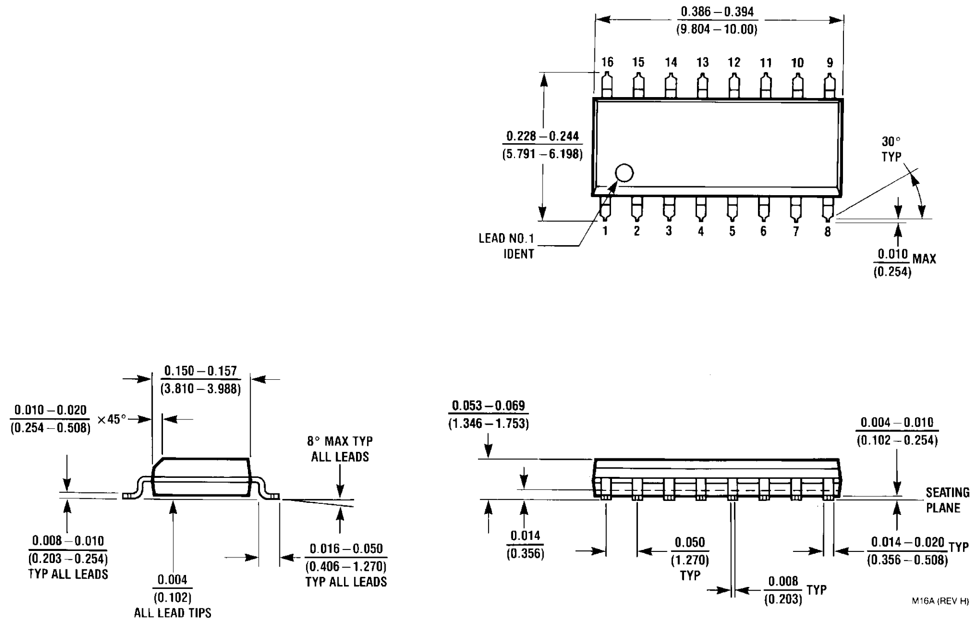
AC Electrical Characteristics

$C_L = 50$ pF $t_r = t_f = 6$ ns (Unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	$T_A = 25°C$		$T_A = -40$ to 85°C	$T_A = -55$ to 125°C	Units
					Typ	Guaranteed Limits			
t_{PLH}	Maximum Trigger Propagation Delay, A or B to Q			2.0V	77	169	194	210	ns
				4.5V	26	42	51	57	
				6.0V	21	32	39	44	
t_{PHL}	Maximum Trigger Propagation Delay, A or B to $\overline{Q}$			2.0V	88	197	229	250	ns
				4.5V	29	48	60	67	
				6.0V	24	38	46	51	
t_{PHL}	Maximum Propagation Delay, Clear to Q			2.0V	54	114	132	143	ns
				4.5V	23	34	41	45	
				6.0V	19	28	33	36	
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$			2.0V	56	116	135	147	ns
				4.5V	25	36	42	46	
				6.0V	20	29	34	37	
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123	144	157	ns
				4.5V	17	30	37	42	
				6.0V	12	21	27	30	
t_{REM}	Minimum Clear Removal Time			2.0V	0	0	0	0	ns
				4.5V	0	0	0	0	
				6.0V	0	0	0	0	
t_{WQ}	Output Pulse Width	$C_{EXT} = 0.1$ µF $R_{EXT} = 10$ kΩ	Min	5.0V	1	0.9	0.86	0.85	ms
			Max	5.0V	1	1.1	1.14	1.15	ms
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	
				6.0V	7	13	16	19	
C_{PD}	Power Dissipation Capacitance (Note 6)				83				pF
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (other inputs)				6	10	10	10	pF

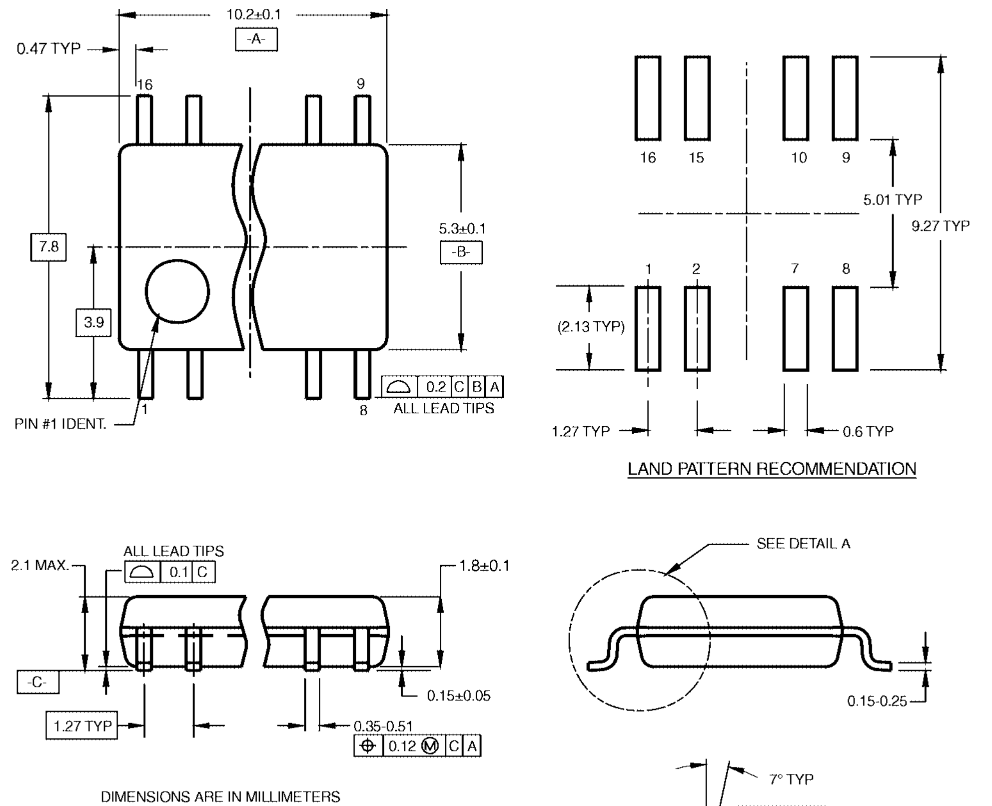
Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

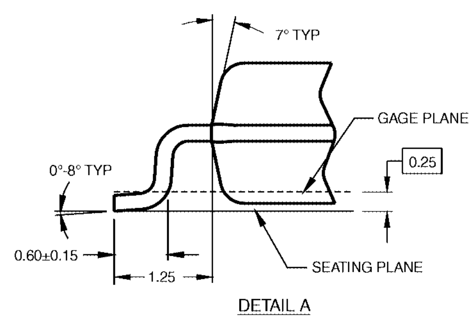
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

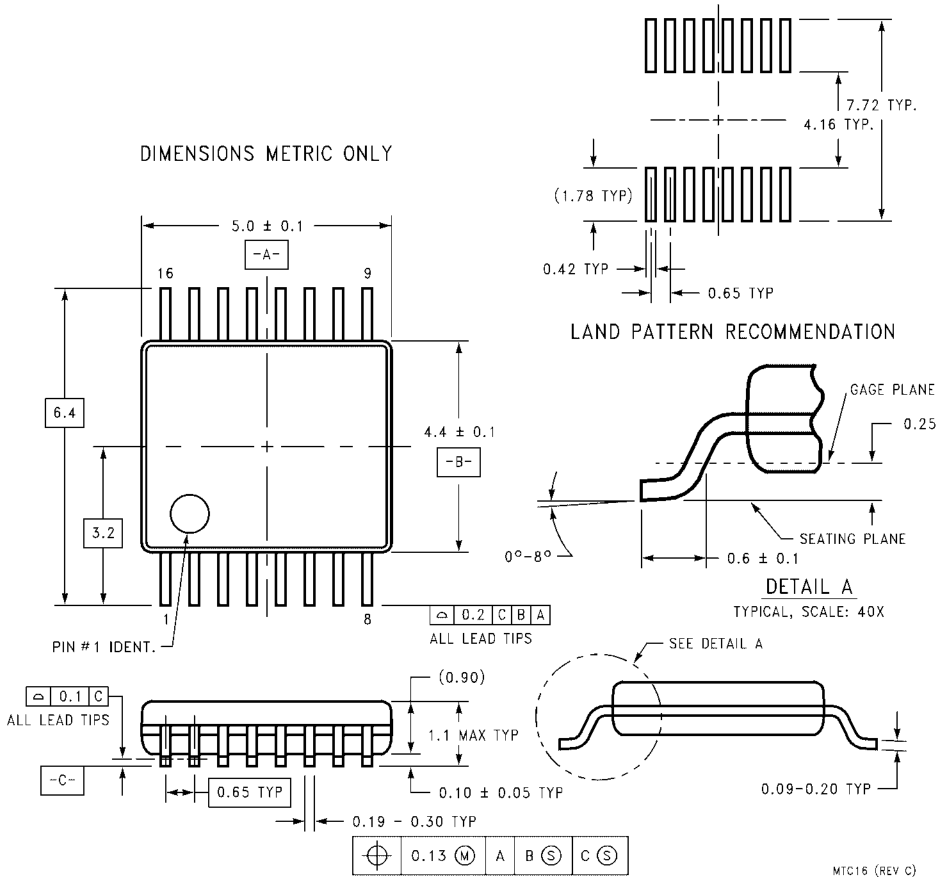
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

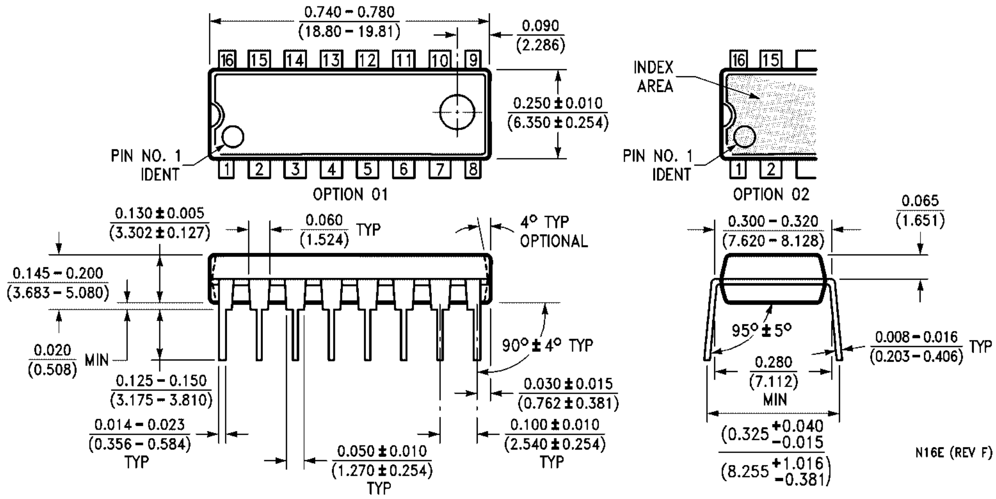
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E