Document Number: MRFE6S9160H
Rev. 1, 12/2008

√RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRFE6S9160HR3
MRFE6S9160HSR3

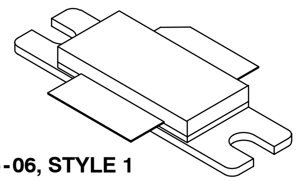
Designed for N-CDMA, GSM and GSM EDGE base station applications with frequencies from 865 to 960 MHz. Suitable for multicarrier amplifier applications.

- Typical Single-Carrier N-CDMA. Performance @ 880 MHz: V_{DD} = 28 Volts, I_{DQ} = 1200 mA, P_{out} = 35 Watts Avg., IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13) Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
  - Power Gain — 21 dB
  - Drain Efficiency — 31%
  - ACPR @ 750 kHz Offset — -46.8 dBc in 30 kHz Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 880 MHz, 3 dB Overdrive, Designed for Enhanced Ruggedness.

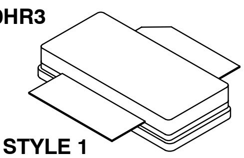
880 MHz, 35 W AVG., 28 V
SINGLE N-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465-06, STYLE 1
NI-780
MRFE6S9160HR3



CASE 465A-06, STYLE 1
NI-780S
MRFE6S9160HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +66	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 160 W CW Case Temperature 73°C, 35 W CW	$R_{\theta JC}$	 0.31 0.33	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

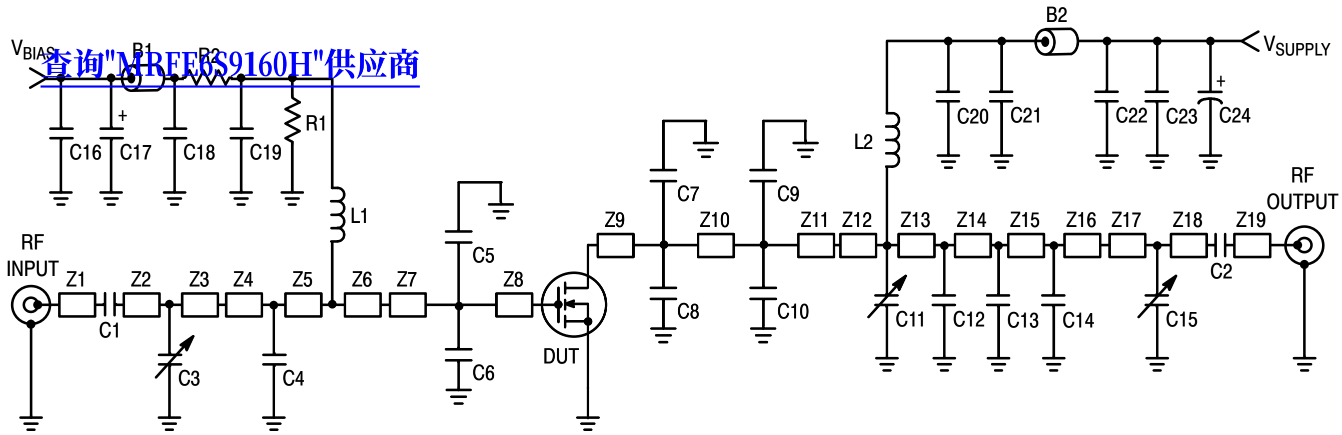
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 66 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	10	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 525 μAdc)	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 1200 mAdc)	$V_{GS(Q)}$	—	3	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_D = 1200 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	2.1	3.17	4.22	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.6 Adc)	$V_{DS(on)}$	0.1	0.175	0.3	Vdc
Dynamic Characteristics (2)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.2	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	80.2	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, P_{out} = 35 W Avg. N-CDMA, f = 880 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ ±750 kHz Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF.					
Power Gain	G_{ps}	20	21	23	dB
Drain Efficiency	η_D	29	31	—	%
Adjacent Channel Power Ratio	ACPR	—	-46.8	-45	dBc
Input Return Loss	IRL	—	-17	-9	dB

1. V_{GG} = 19/18 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part is internally matched on input.

(continued)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, 865-900 MHz Bandwidth					
Video Bandwidth @ 160 W PEP P_{out} where IM3 = -30 dBc (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency - IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	10	—	MHz
Gain Flatness in 35 MHz Bandwidth @ P_{out} = 35 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.016	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.008	—	dBm/°C



Z1	0.426″ x 0.080″ Microstrip	Z11	0.066″ x 0.630″ Microstrip
Z2	0.813″ x 0.080″ Microstrip	Z12	0.630″ x 0.425″ x 0.220″ Taper
Z3	0.471″ x 0.080″ Microstrip	Z13	0.120″ x 0.220″ Microstrip
Z4	0.319″ x 0.220″ Microstrip	Z14	0.292″ x 0.220″ Microstrip
Z5	0.171″ x 0.220″ Microstrip	Z15	0.023″ x 0.220″ Microstrip
Z6	0.200″ x 0.425″ x 0.630″ Taper	Z16	0.030″ x 0.220″ Microstrip
Z7	0.742″ x 0.630″ Microstrip	Z17	0.846″ x 0.080″ Microstrip
Z8	0.233″ x 0.630″ Microstrip	Z18	0.440″ x 0.080″ Microstrip
Z9	0.128″ x 0.630″ Microstrip	Z19	0.434″ x 0.080″ Microstrip
Z10	0.134″ x 0.630″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55

Figure 1. MRFE6S9160HR3(SR3) Test Circuit Schematic

Table 5. MRFE6S9160HR3(SR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1, B2	Ferrite Beads, Small	2743019447	Fair Rite
C1, C2, C19	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C3, C11	0.8-8.0 pF Variable Capacitors, Gigatrim	27291SL	Johanson
C4	2.7 pF Chip Capacitor	ATC100B2R7JT500XT	ATC
C5, C6	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
C7, C8	12 pF Chip Capacitors	ATC100B120JT500XT	ATC
C9, C10	4.3 pF Chip Capacitors	ATC100B4R3JT500XT	ATC
C12	8.2 pF Chip Capacitor	ATC100B8R2JT500XT	ATC
C13, C14	3.9 pF Chip Capacitors	ATC100B3R9JT500XT	ATC
C15	0.6-4.5 pF Variable Capacitor, Gigatrim	27271SL	Johanson
C16	22 pF Chip Capacitor	ATC100B220JT500XT	ATC
C17	1 μF, 50 V Tantalum Capacitor	T491C105K0J0AT	Kemet
C18	20K pF Chip Capacitor	CDR35BP203AKYS	Kemet
C20	180 pF Chip Capacitor	ATC100B181JT500XT	ATC
C21, C22, C23	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88B	Murata
C24	470 μF, 63 V Electrolytic Capacitor	ESME630ELL471MK25S	United Chemi-Con
L1, L2	10 nH Inductors	0603HC	Coilcraft
R1	180 Ω, 1/4 W Chip Resistor	CRCW12061800FKEA	Vishay
R2	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

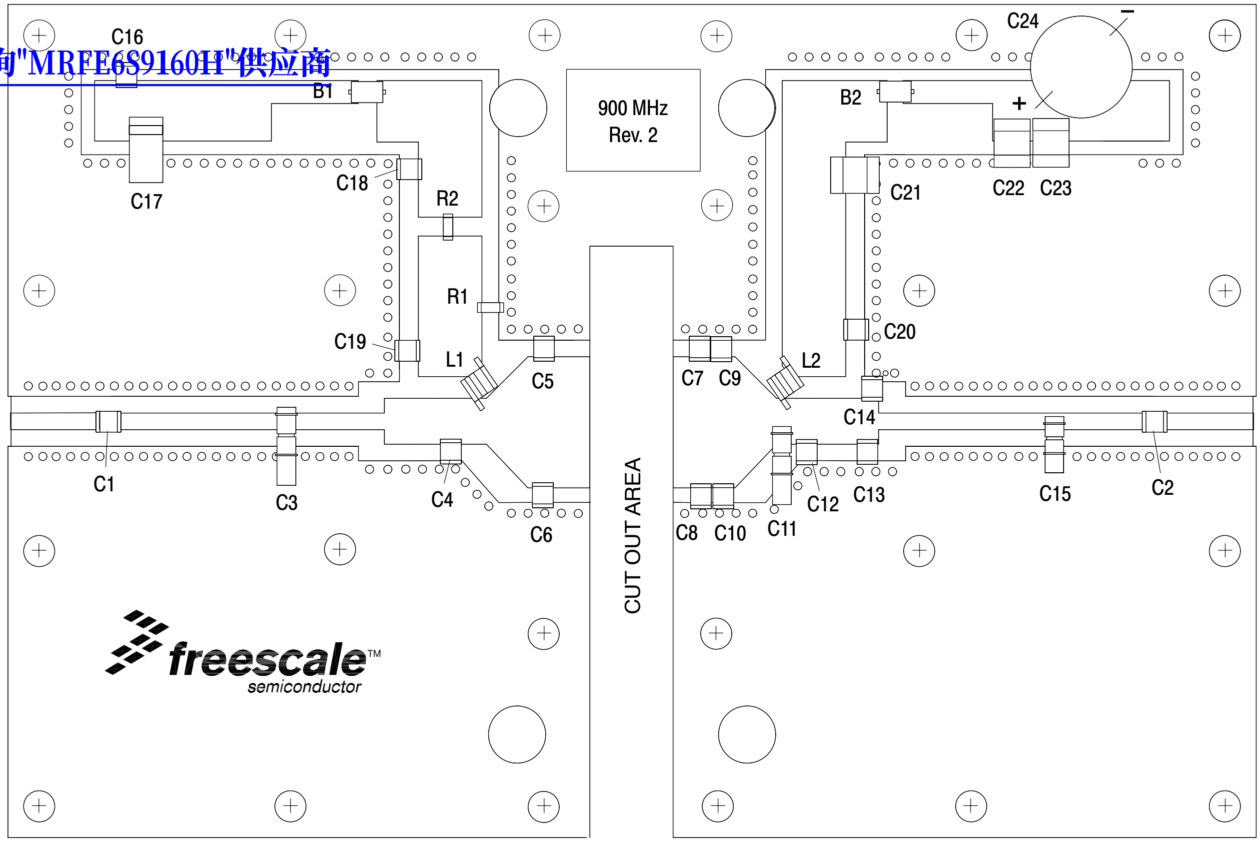


Figure 2. MRFE6S9160HR3(SR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

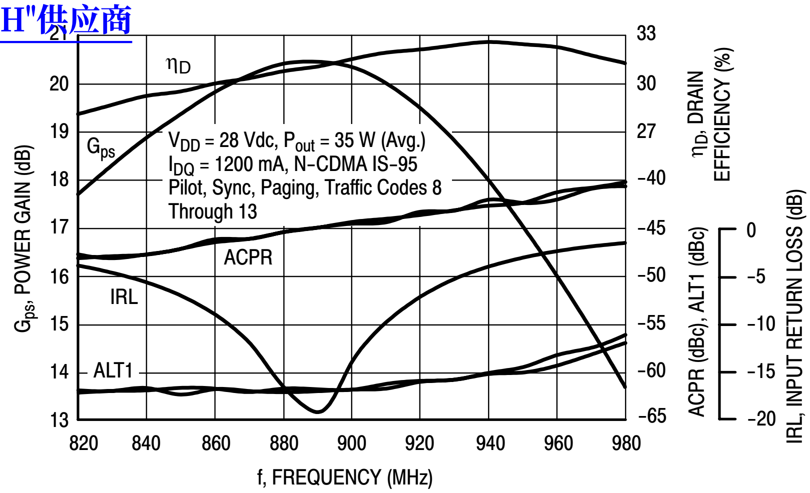


Figure 3. Single-Carrier N-CDMA Broadband Performance @ P_{out} = 35 Watts Avg.

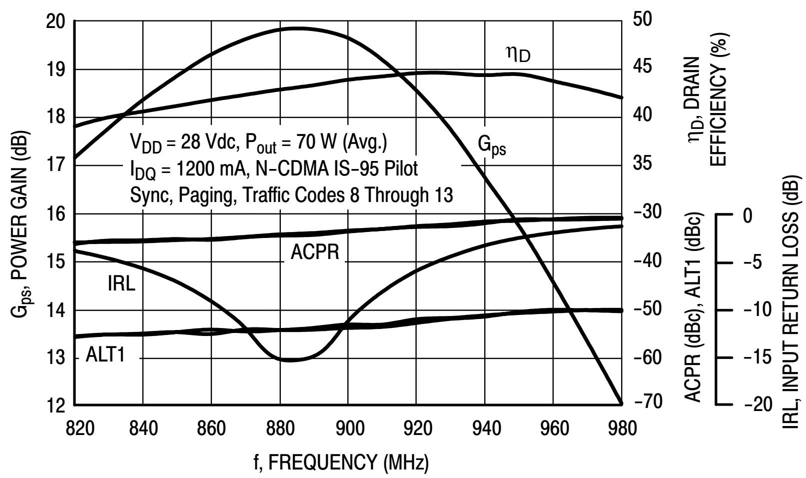


Figure 4. Single-Carrier N-CDMA Broadband Performance @ P_{out} = 70 Watts Avg.

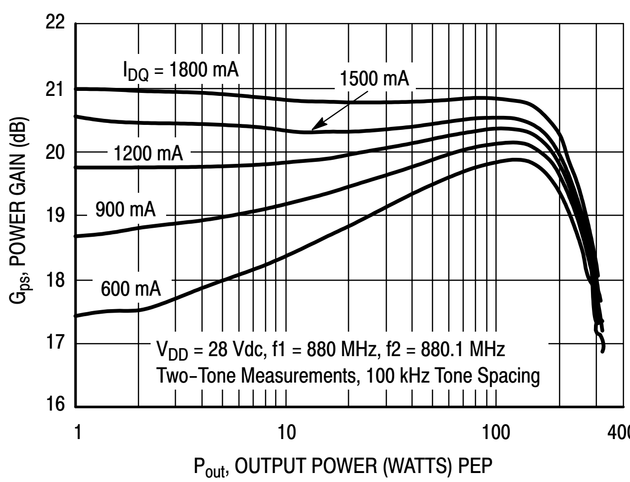


Figure 5. Two-Tone Power Gain versus Output Power

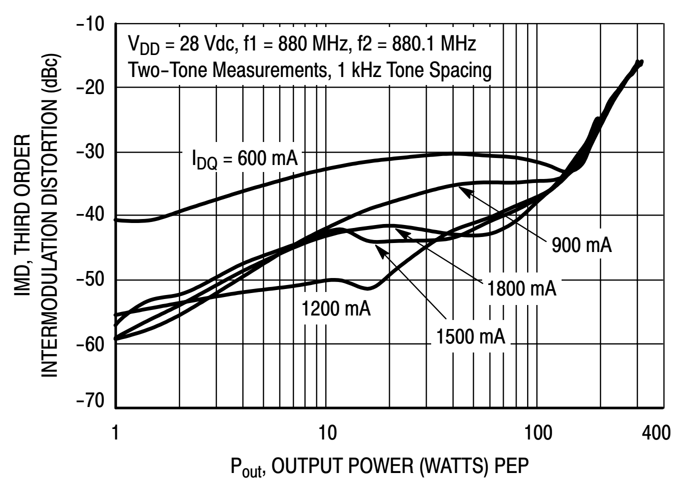


Figure 6. Third Order Intermodulation Distortion versus Output Power

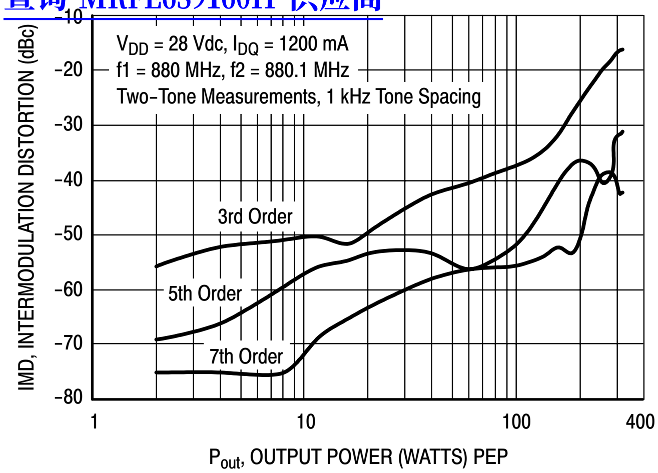


Figure 7. Intermodulation Distortion Products versus Output Power

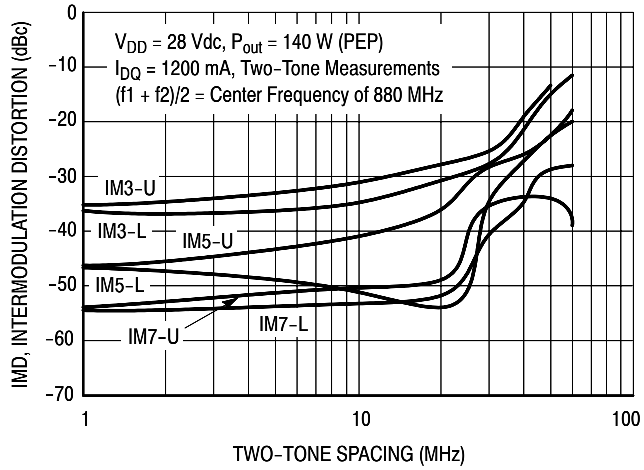


Figure 8. Intermodulation Distortion Products versus Tone Spacing

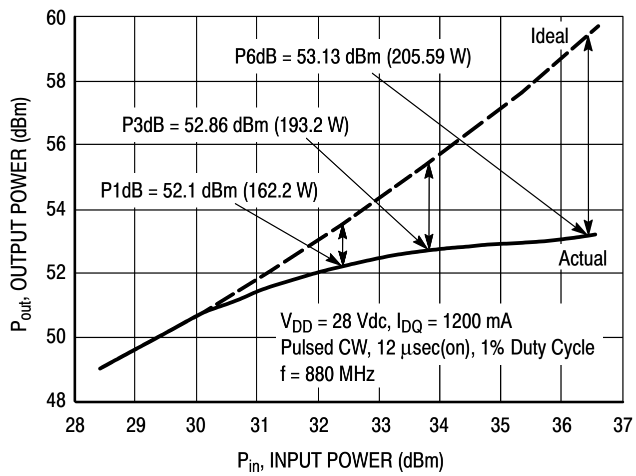


Figure 9. Pulsed CW Output Power versus Input Power

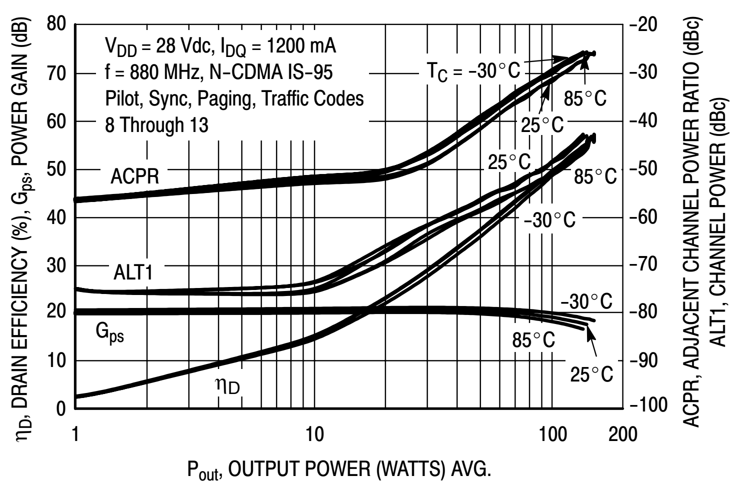


Figure 10. Single-Carrier N-CDMA ACPR, ALT1, Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS

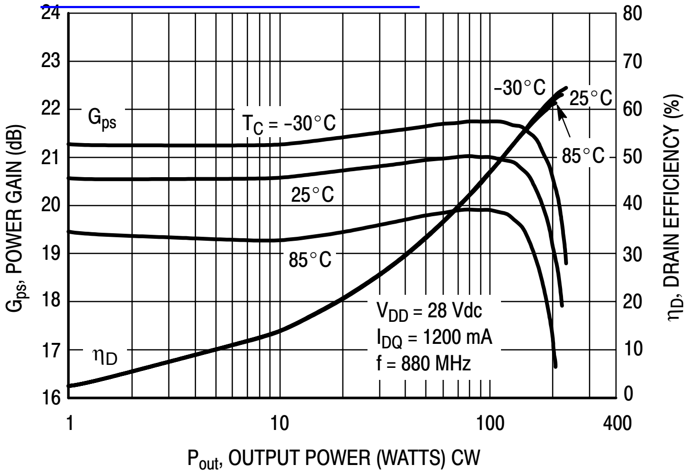


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

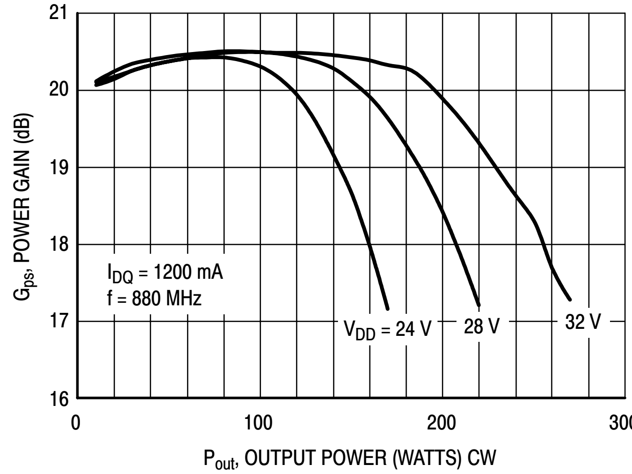
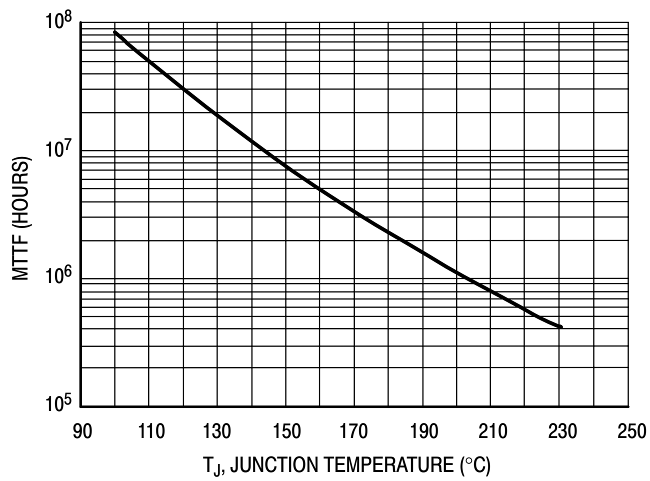


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 35 W Avg., and η_D = 31%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature

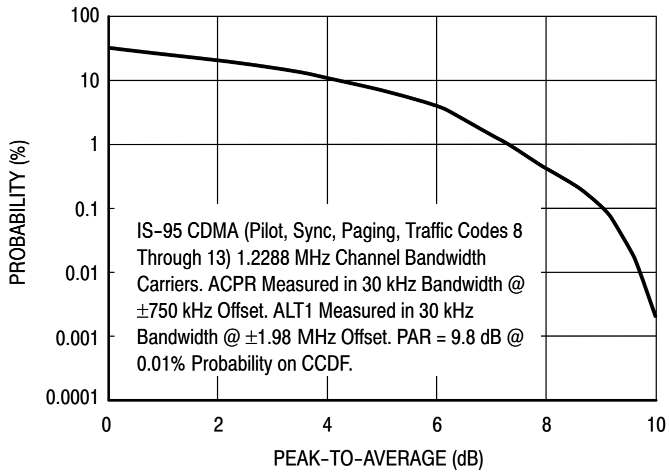


Figure 14. Single-Carrier CCDF N-CDMA

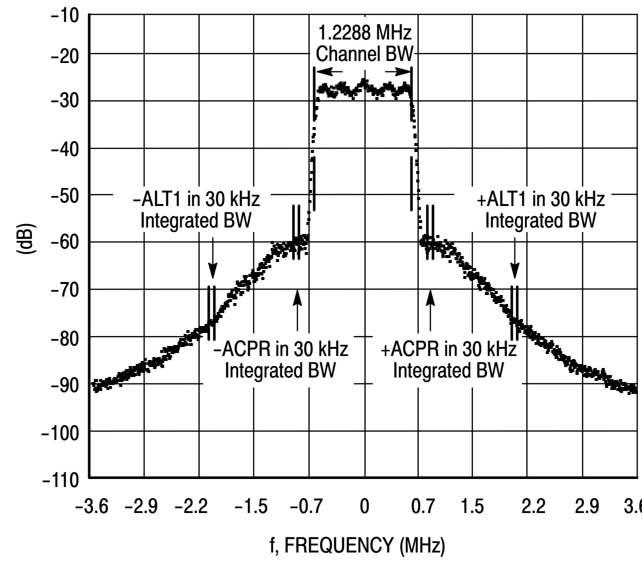
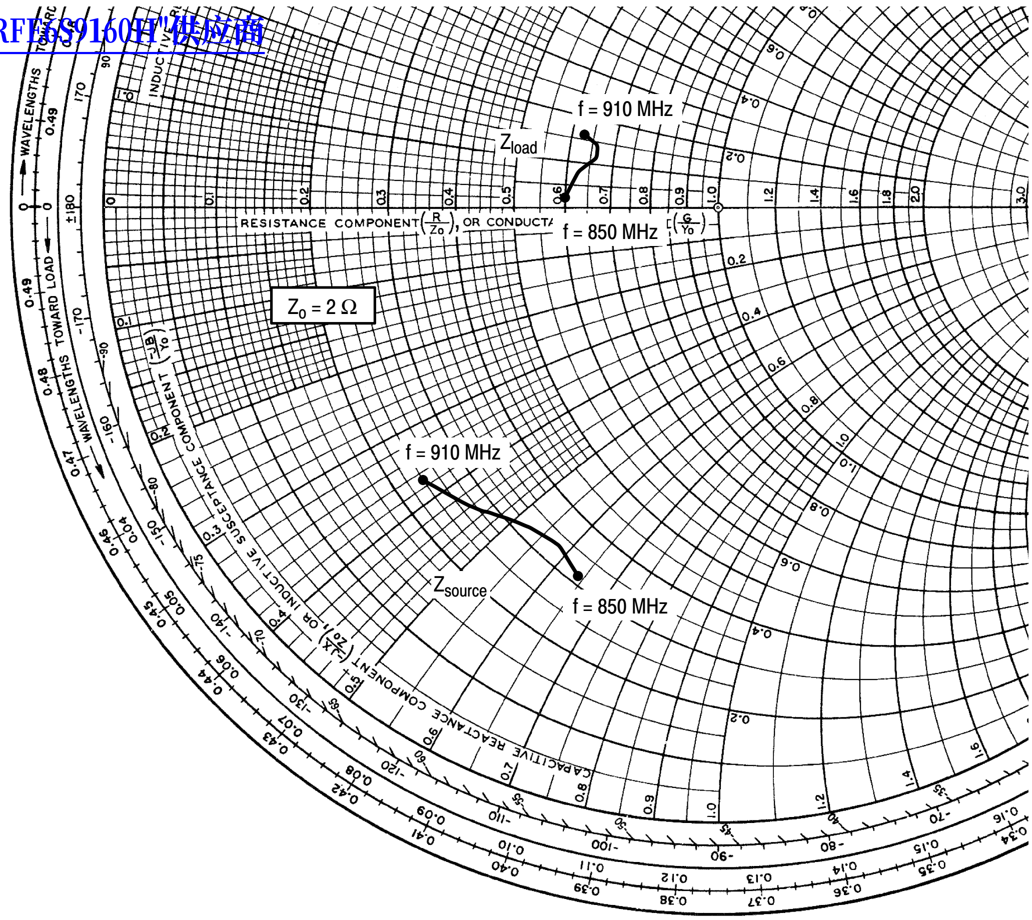


Figure 15. Single-Carrier N-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, P_{out} = 35 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
850	0.61 - j1.27	1.20 + j0.03
865	0.66 - j1.15	1.26 + j0.15
880	0.64 - j1.05	1.31 + j0.22
895	0.55 - j0.90	1.32 + j0.28
910	0.48 - j0.74	1.26 + j0.32

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

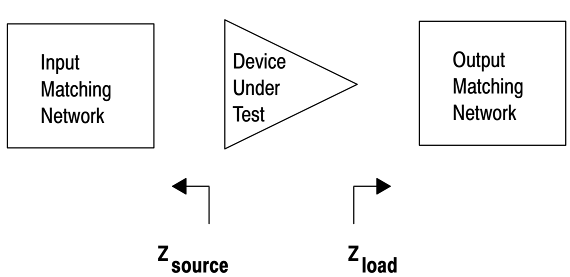
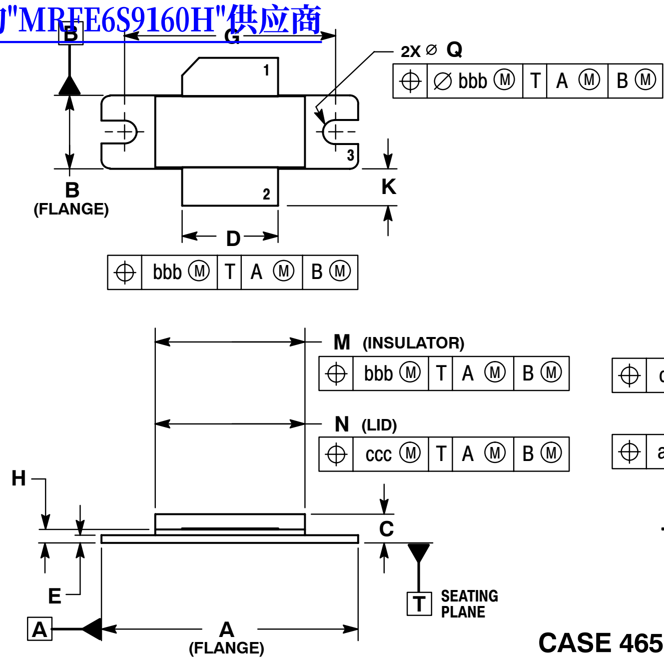
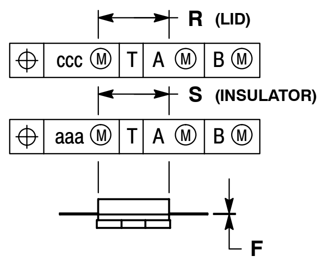


Figure 16. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



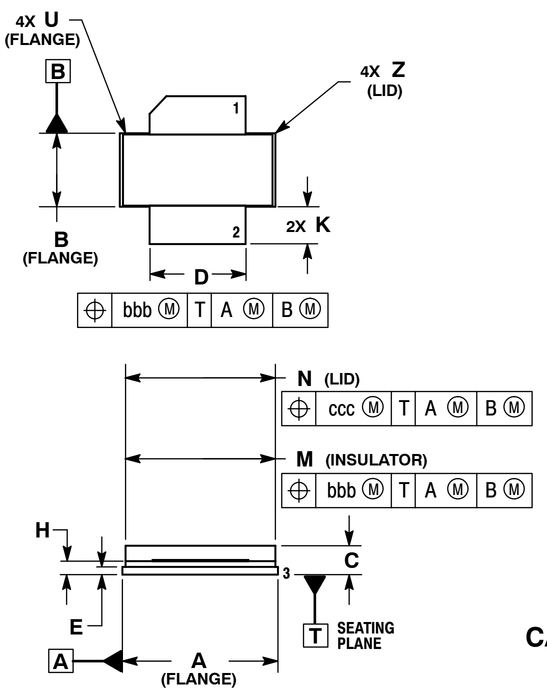


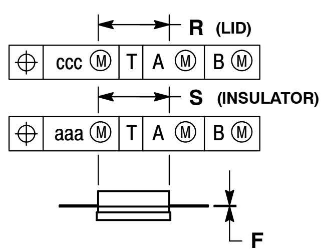
CASE 465-06
ISSUE G
NI-780
MRFE6S9160HR3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE





CASE 465A-06
ISSUE H
NI-780S
MRFE6S9160HSR3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2007	• Initial Release of Data Sheet
1	Dec. 2008	• Table 4, On Characteristics, tightened $V_{DS(on)}$ Min value from 0.05 to 0.1 to match production test values, p. 2 • Updated PCB information to show more specific material details, Fig. 1, Test Circuit Schematic, p. 4 • Updated Part Numbers in Table 5, Component Designations and Values, to latest RoHS compliant part numbers, p. 4 • Adjust scale for Fig. 8, Intermodulation Distortion Products versus Tone Spacing, to show wider dynamic range, p. 7

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