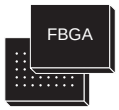
M36L0R7060U1 M36L0R7060L1 M36L0R7050U1 M36L0R7050L1

128 Mbit (Mux I/O, Multiple Bank, Multi-Level, Burst) Flash memory, 32 or 64 Mbit PSRAM, 1.8V supply Multi-Chip Package

Preliminary Data

Feature summary

- Multi-Chip Package
  - 1 die of 128 Mbit (8Mb x16, Mux I/O Multiple Bank, Multi-level, Burst) Flash Memory
  - 1 die of 32 or 64Mbit Mux I/O, Burst Pseudo SRAM
- Supply voltage
  - $V_{DDF} = V_{DDP} = V_{DDQF} = 1.7$ to 1.95V
  - $V_{PPF} = 9V$ for fast program
- Electronic signature
  - Manufacturer Code: 20h
  - Device Codes (Top Flash Configuration): M36L0R7060U1: 882Eh, M36L0R7050U1: 882Eh
  - Device Codes (Bottom Flash Configuration) M36L0R7060L1: 882Fh M36L0R7050L1: 882Fh
- ECOPACK® package



TFBGA88 (ZAM)
8 x 10mm

Flash memory

- Multiplexed address/data
- Synchronous / asynchronous read
  - Synchronous Burst Read mode: 66MHz
  - Random Access: 85ns
- Synchronous burst read suspend programming time
  - 10µs typical Word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple Bank Memory Array: 8 Mbit Banks
  - Parameter Blocks (Top or Bottom location)
- Security
  - 64 bit unique device number
  - 2112 bit user programmable OTP Cells
- 100,000 program/erase cycles per block
- Dual operations
  - program/erase in one Bank while read in others
  - No delay between Read and Write operations
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}_F$ for Block Lock-Down
  - Absolute Write Protection with $V_{PPF} = V_{SS}$
- Common Flash Interface (CFI)

PSRAM

- Access time: 70ns
- Synchronous modes:
  - Synchronous Write: continuous burst
  - Synchronous Read: continuous burst or fixed length: 4, 8 or 16 Words for 32 Mbit devices or 4, 8,16 or 32 Words for 64 Mbit devices
  - Maximum Clock Frequency: 83MHz
- Low power consumption
- Low power features
  - Partial Array Self-Refresh (PASR)
  - Deep Power-Down (DPD) Mode
  - Automatic Temperature-compensated Self-Refresh

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1 Summary description

The M36L0R7060U1, M36L0R7060L1, M36L0R7050U1 and M36L0R7050L1 combine two memory devices in a Multi-Chip Package:

- a 128-Mbit, Multiple Bank Flash memory, the M58LR128G(U/L)
- a 32 or 64 Mbit PseudoSRAM, the M69KM048AA or M69KM096AA, respectively.

The purpose of this document is to describe how the two memory components operate with respect to each other. It must be read in conjunction with the M58LRxxxGUL and M69KM048AA or M69KM096AA datasheets, where all specifications required to operate the Flash memory and PSRAM components are fully detailed. These datasheets are available from the STMicroelectronics website: *www.st.com*.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA88 (8 ×10mm, 8 × 10 ball array, 0.8mm pitch) package.

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic diagram

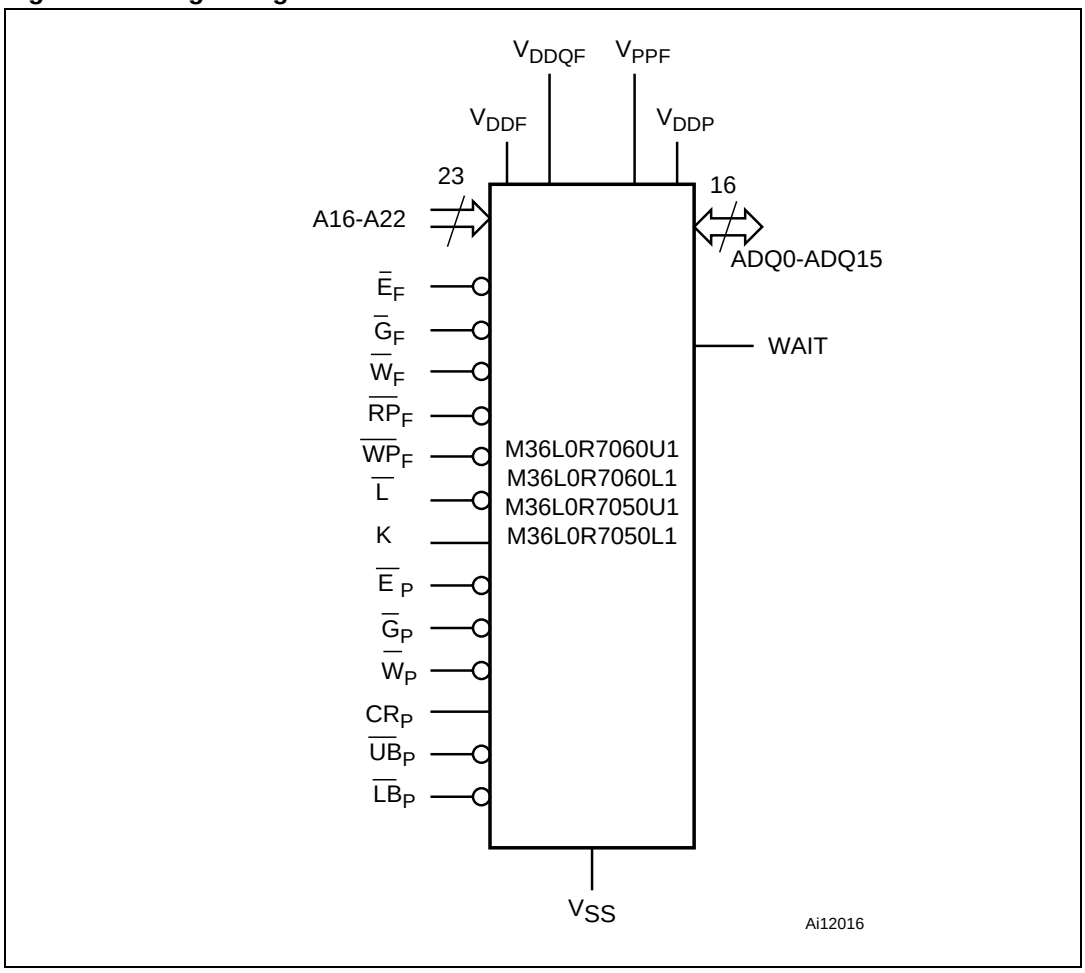
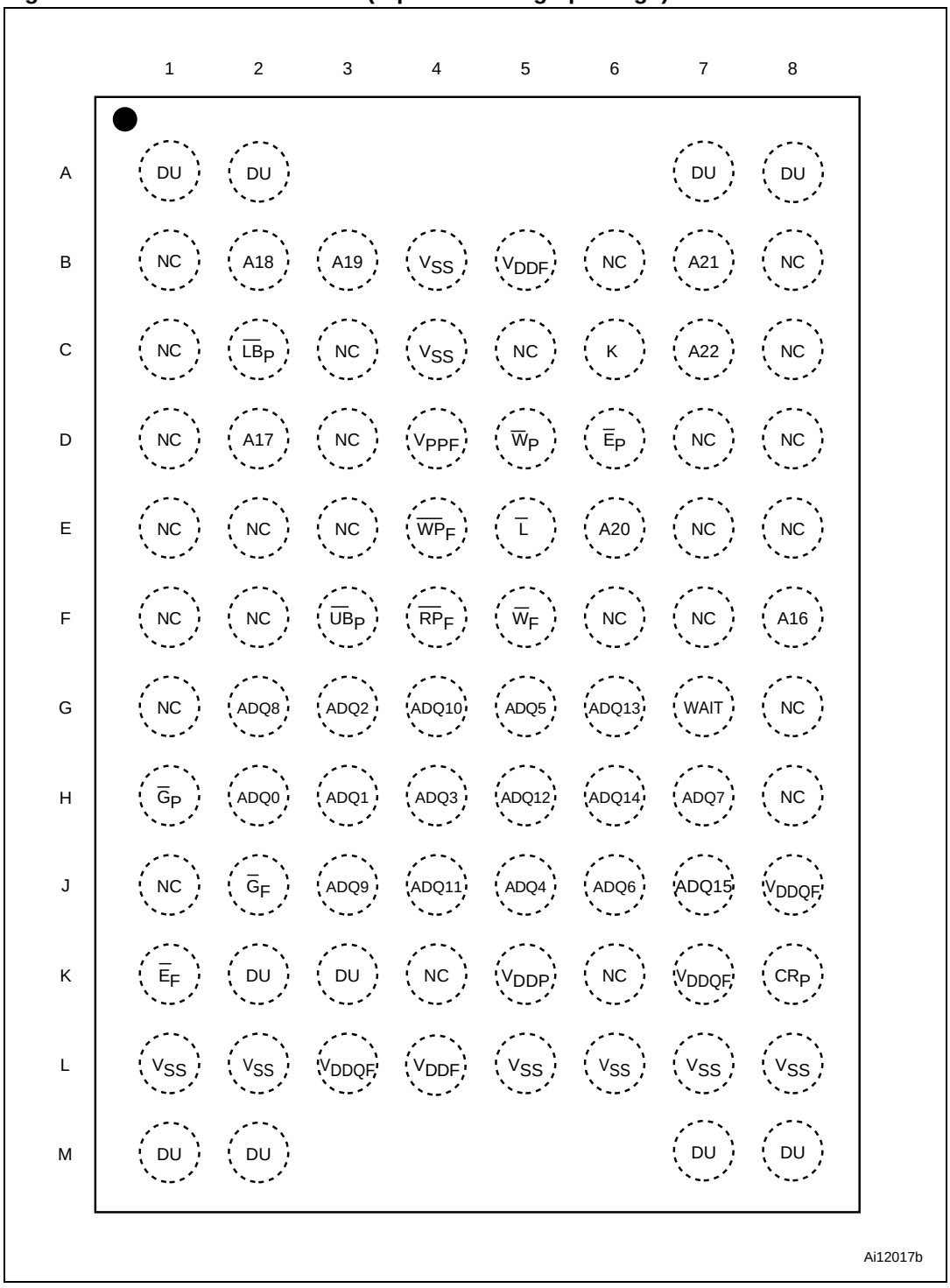


Table 1. Signal names

A16-A22(1), (2)	Address Inputs
ADQ0-ADQ15	Flash memory and PSRAM common Data Input/Outputs, Address Inputs or Command Inputs
V_{DDF}	Power Supply for Flash memory
V_{DDQF}	Flash memory Power Supply for I/O Buffers
V_{PPF}	Flash memory Optional Supply Voltage for Fast Program and Erase
V_{SS}	Ground
V_{DDP}	PSRAM Power Supply
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
WAIT	Flash memory and PSRAM Common Wait Data in Burst Mode
$\overline{L}$	Flash memory and PSRAM Latch Enable Input
K	Flash memory and PSRAM Burst Clock
Flash Memory	
$\overline{E}_F$	Chip Enable Input
$\overline{G}_F$	Output Enable Input
$\overline{W}_F$	Write Enable Input
$\overline{RP}_F$	Reset Input
$\overline{WP}_F$	Write Protect Input
PSRAM	
$\overline{E}_P$	Chip Enable Input
$\overline{G}_P$	Output Enable Input
$\overline{W}_P$	Write Enable Input
CR_P	Configuration Register Enable Input
$\overline{UB}_P$	Upper Byte Enable Input
$\overline{LB}_P$	Lower Byte Enable Input

1. A16-A20 (in the case of a 32Mb PSRAM) or A16-A21 (in the case of a 64Mb PSRAM) are common to the Flash memory and the PSRAM
2. A21-A22 (if the MCP contains a 32Mb PSRAM) or A22 (if the MCP contains a 64Mb PSRAM) are Address Input(s) for the Flash memory component only.

Figure 2. TFBGA connections (top view through package)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (ADQ0-ADQ15 and A16-A22)

ADQ0-ADQ15 and A16-A20 (for the M36L0R7050U1/L1) or A16-A21 (for the M36L0R7060U1/L1) are common to the Flash memory and PSRAM components.

In the Flash memory, the Address Inputs select the cells in the array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller.

In the PSRAM, the Address Inputs A16-A20 (/A21) are used in conjunction with ADQ0 to ADQ15, to select the cells in the memory array that are accessed during read and write operations.

2.2 Data Input/Output (ADQ0-ADQ15)

The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

2.3 Latch Enable ($\overline{L}$)

The Latch Enable input is common to the Flash memory and PSRAM components.

For details of how the Latch Enable signal behaves, please refer to the datasheets of the respective memory components: M69KM048AA or M69KM096AA for the PSRAM and M58LRxxxGUL for the Flash memory.

2.4 Clock (K)

The Clock input is common to the Flash memory and PSRAM components.

For details of how the Clock signal behaves, please refer to the datasheets of the respective memory components: M69KM048AA or M69KM096AA for the PSRAM and M58LRxxxGUL for the Flash memory.

2.5 Wait (WAIT)

The Wait output is common to the Flash memory and PSRAM components.

For details of how the WAIT signal behaves, please refer to the datasheets of the respective memory components: M69KM048AA or M69KM096AA for the PSRAM and M58LRxxxGUL for the Flash memory

2.6 Flash memory Chip Enable ($\overline{E}_F$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

It is not allowed to set both $\overline{E}_F$ and $\overline{E}_P$ to V_{IL} at the same time.

2.7 Flash memory Output Enable ($\overline{G}_F$)

The Output Enable input controls data outputs during the Bus Read operation of the Flash memory.

2.8 Flash memory Write Enable ($\overline{W}_F$)

The Write Enable input controls the Bus Write operation of the Flash memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.9 Flash memory Write Protect ($\overline{WP}_F$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at V_{IH}, the Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (refer to M58LRxxxGUL datasheet).

2.10 Flash memory Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to the M58LRxxxGUL datasheet for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to the M58LRxxxGUL datasheet).

2.11 PSRAM Chip Enable ($\overline{E}_P$)

Chip Enable, $\overline{E}_P$, activates the device when driven Low (asserted). When de-asserted (V_{IH}), the device is disabled and goes automatically in low-power Standby mode or Deep Power-Down mode, according to the RCR settings.

It is not allowed to set both $\overline{E}_F$ and $\overline{E}_P$ to V_{IL} at the same time.

2.12 PSRAM Output Enable ($\overline{G}_P$)

When held Low, V_{IL}, the Output Enable, $\overline{G}_P$, enables the Bus Read operations of the memory.

2.13 PSRAM Write Enable ($\overline{W}_P$)

Write Enable, $\overline{W}_P$, controls the Bus Write operation of the memory. When asserted (V_{IL}), the device is in write mode and write operations can be performed either to the configuration registers or to the memory array.

2.14 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte Enable, $\overline{UB}_P$, gates the data on the Upper Byte of the Address Inputs/ Data Inputs/Outputs (ADQ8-ADQ15) to or from the upper part of the selected address during a write or read operation.

2.15 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the Lower Byte of the Address Inputs/Data Input/Outputs (ADQ0-ADQ7) to or from the lower part of the selected address during a write or read operation.

If both $\overline{LB}_P$ and $\overline{UB}_P$ are disabled (High), the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{E}_P$ remains Low.

2.16 PSRAM Configuration Register Enable (CR_P)

When this signal is driven High, V_{IH}, bus read or write operations access either the value of the Refresh Configuration Register (RCR) or the Bus Configuration Register (BCR) according to the value of A19.

2.17 V_{DDF} Flash memory Supply Voltage

V_{DDF} provides the power supply to the internal core of the Flash memory. It is the main power supply for all Flash memory operations (Read, Program and Erase).

2.18 V_{CCP} PSRAM Supply Voltage

The V_{CCP} Supply Voltage is the core supply voltage.

2.19 V_{DDQF} Supply Voltage

V_{DDQF} provides the power supply to the I/O pins and enables all Outputs to be powered independently of V_{DDF}. V_{DDQF} can be tied to V_{DDF} or can use a separate supply.

2.20 V_{PPF} Flash memory Program Supply Voltage

V_{PPF} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQF}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives absolute protection against program or erase, while V_{PPF} in the V_{PP1} range enables these functions (see the M58LRxxxGUL datasheet for the relevant values). V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

2.21 V_{SS} Ground

V_{SS} ground is the common Flash memory and PSRAM ground. It is the reference for the core supplies. It must be connected to the system ground.

2.22 V_{SSQ} Ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQF}. V_{SSQ} must be connected to V_{SS}

Note: Each device in a system should have V_{DDF}, V_{DDQF} and V_{PP} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 5: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

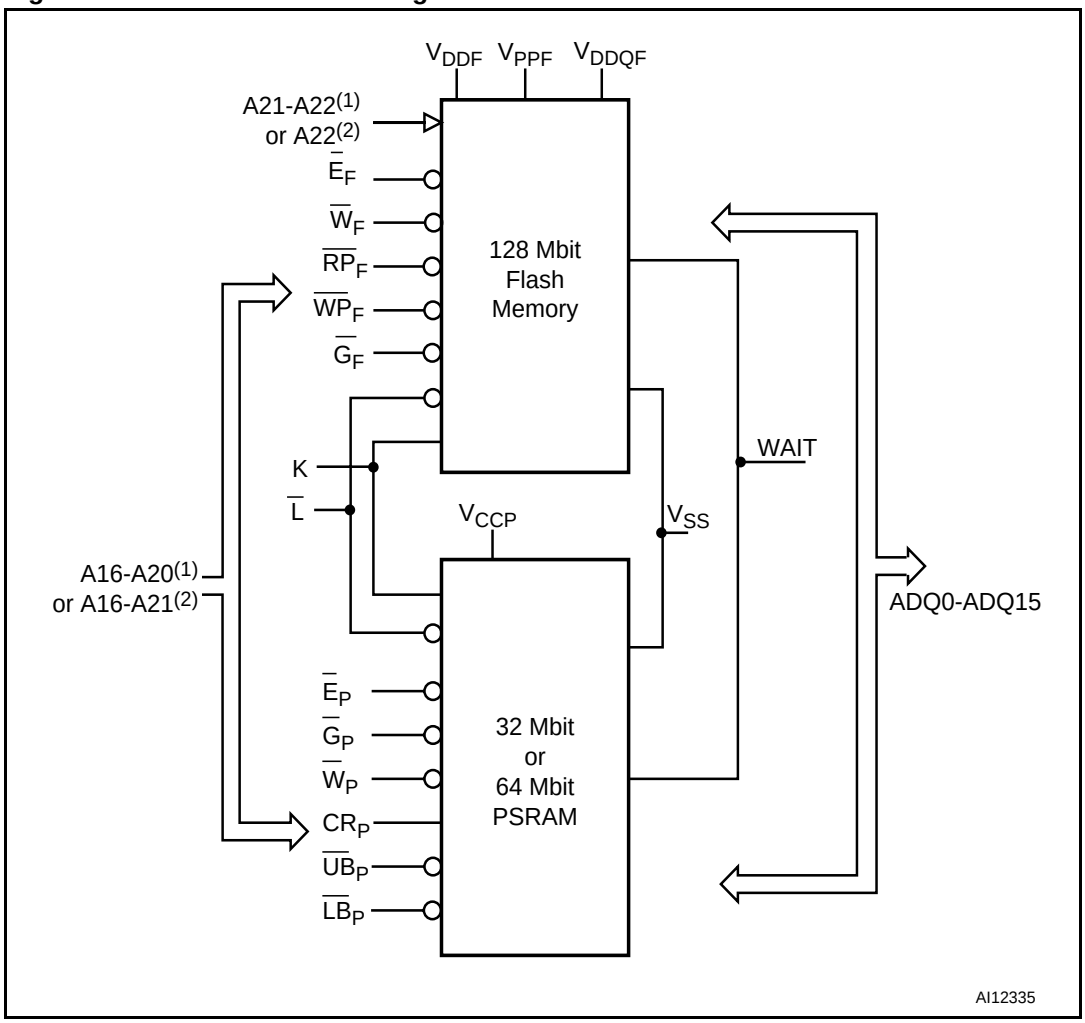
3 Functional description

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E}_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on one of the Flash memory and the PSRAM components which would result in a data bus contention.

Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 3. Functional block diagram



1. Address Inputs corresponding to the M36L0R7050U1 and M36L0R7050L1 devices.
2. Address Inputs corresponding to the M36L0R7060U1 and M36L0R7060L1 devices.

Table 2. Operating modes - Standard Asynchronous operation

Operation(1) (2)		$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{RP}_F$	WAIT (3)	$\overline{L}$	$\overline{E}_P$	$\overline{W}_P$	$\overline{G}_P$	$\overline{UB}_P$	$\overline{LB}_P$	CR_P	A19	A18	Other Address Inputs	ADQ0-ADQ7	ADQ8-ADQ15
Flash memory	Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}		V_{IH}	The PSRAM must be disabled.									Data Output	
	Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}		V_{IH}										Data Input	
	Address Latch	V_{IL}	V_{IH}	X	V_{IH}		V_{IL}										Address Input	
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}		V_{IH}	Any PSRAM mode is allowed.									Hi-Z	
	Standby	V_{IH}	X	X	V_{IH}	Hi-Z	X										Hi-Z	
	Reset	X	X	X	V_{IL}	Hi-Z	X										Hi-Z	
PSRAM	Word Read	The Flash memory must be disabled.					¯_/¯	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	Address In Valid			Address In/ Data Out Valid	
	Word Write								V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Address In Valid			Address In/ Data In Valid	
	Read Configuration Register (CR controlled method)(4)								V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	00(RCR) 10(BCR) X1(DIDR)	X		Address In/ BCR, RCR or DIDR Content Valid	
	Program Configuration Register (CR Controlled)(5)						V_{IL}		V_{IL}	V_{IH}	X	X		0 or 00 (RCR) 1 or 10 (BCR)(6)	BCR/ RCR Data		Address In Valid	
	Output Disable/No Operation	Any Flash memory mode is allowed.					X		V_{IH}	X	X	X	V_{IL}	X	X	X	High-Z	
	Deep Power-Down(7)							V_{IH}	X	X	X	X	X	X	X	X	High-Z	
	Standby							V_{IH}	X	X	X	X	X	V_{IL}	X	X	High-Z	

1. The Clock signal, K, must remain Low when the PSRAM is operating in asynchronous mode.
2. X = Don't Care
3. In the Flash memory the WAIT signal polarity is configured using the Set Configuration Register command.
4. Operating mode available in the M36L0R7060U1 and M36L0R7060L1 only (see M69KM096AA datasheet).
5. BCR and RCR only.
6. In the PSRAM of the M36L0R7050U1 and M36L0R7050L1, A19 is used to select between the BCR and the RCR whereas in the PSRAM of the M36L0R7060U1 and M36L0R7060L1 both A18 and A19 are used to select the BCR, the RCR or the DIDR.
7. The device enters Deep Power-Down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to '0'. The device remains in Deep Power-Down mode until $\overline{E}$ goes Low again and is held Low for $t_{ELEH(DP)}$.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–25	85	°C
T_{BIAS}	Temperature Under Bias	–25	85	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{IO}	Input or Output Voltage	–0.2	2.45	V
V_{DDF}, V_{DDQF} V_{CCP}	Core and Input/Output Supply Voltages	–0.2	2.45	V
V_{PPF}	Flash Program Voltage	–0.2	10	V
I_O	Output Short Circuit Current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} Supply Voltage	1.7	1.95	–	–	V
V_{CCP} Supply Voltage	–	–	1.7	1.95	V
V_{DDQF} Supply Voltage	1.7	1.95	–	–	V
V_{PPF} Supply Voltage (Factory environment)	8.5	9.5	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQF} +0.4	–	–	V
Ambient Operating Temperature	–25	85	–25	85	°C
Load Capacitance (C_L)	30		30		pF
Output Circuit Resistors (R_1, R_2)	16.7		16.7		kΩ
Input Rise and Fall Times		5		2	ns
Input Pulse Voltages	0 to V_{DDQF}		0 to $V_{CCP}/2$		V
Input and Output Timing Ref. Voltages	$V_{DDQF}/2$		$V_{CCP}/2$		V

Figure 4. AC measurement I/O waveform

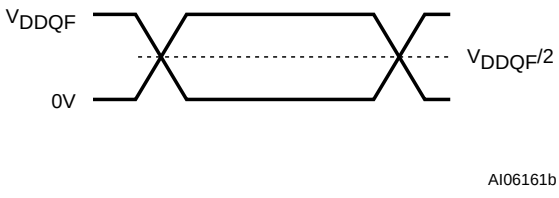


Figure 5. AC measurement load circuit

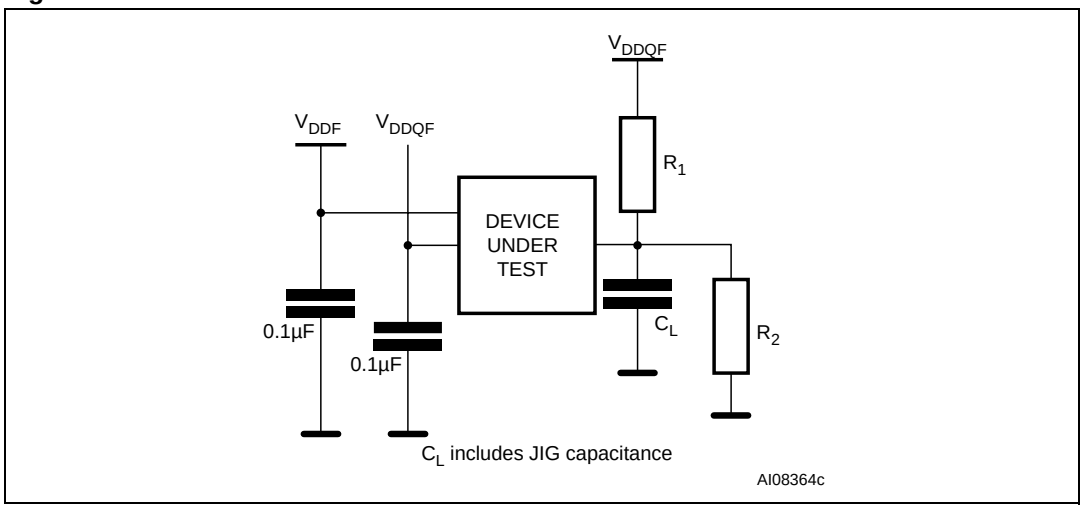


Table 5. Device capacitance

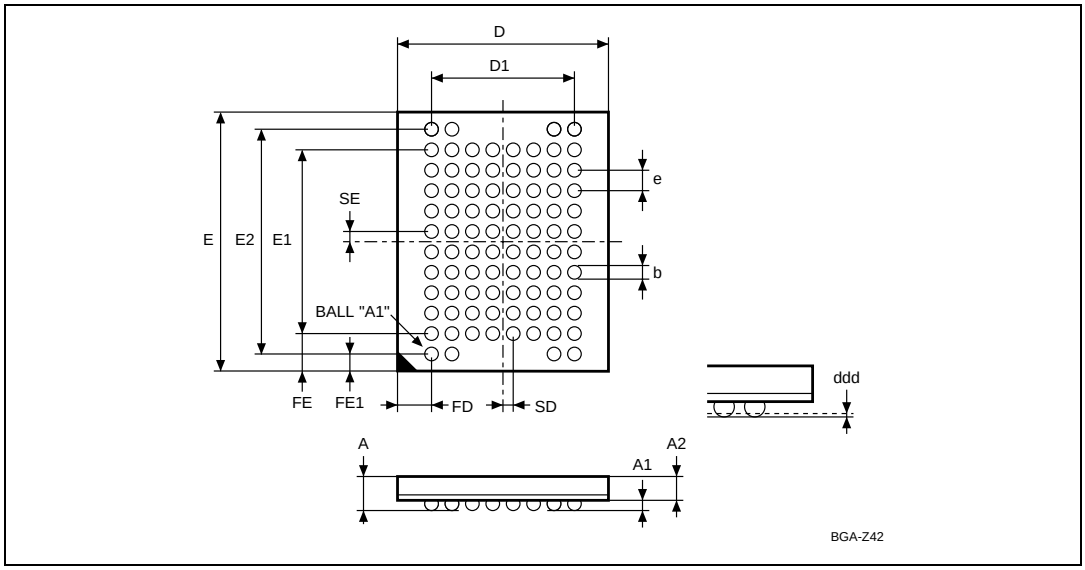
Symbol	Parameter	Test Condition	Min	Max(1)	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		18	pF

1. Sampled only, not 100% tested.

Please refer to the M58LRxxxGUL and M69KM048AA or M69KM096AA datasheets for further DC and AC characteristics values and illustrations.

6 Package mechanical

Figure 6. TFBGA88 8 × 10mm, 8 × 10 ball array - 0.8mm pitch, bottom view package outline



1. Drawing is not to scale.

Table 6. Stacked TFBGA88 8 × 10mm - 8 × 10 active ball array, 0.8mm pitch, package data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

7 Part numbering

Table 7. Part numbering scheme

Example: M36 L 0 R 7 0 5 0 L 1 ZAM F

Device Type

M36 = Multi-Chip Package (Flash + RAM)

Flash 1 Architecture

L = Multi-Level, Multiple Bank, Burst Mode

Flash 2 Architecture

0 = No Die

Operating Voltage

R = V_{DDF} = V_{DDP} = V_{DDQF} = 1.7V to 1.95V

Flash 1 Density

7 = 128 Mbit

Flash 2 Density

0 = No Die

RAM 1 Density

5 = 32 Mbit

6 = 64 Mbit

RAM 2 Density

0 = No Die

Parameter Block Location

U = Top Boot Block Flash

L = Bottom Boot Block Flash

Product Version

1 = 0.13µm Flash technology and multilevel design, 85ns speeds;
RAM, 70ns speed Mux I/O

Package

ZAM = Stacked TFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch

Packing Option

E = ECOPACK® Package, Standard Packing

F = ECOPACK® Package, Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest ST Sales Office.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
08-Jun-2006	1	Initial release.

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