

Gigabit 8 x 8 CROSSPOINT SWITCH

Check for Samples: [SN65LVCP408](#)

FEATURES

- Up to 4.25 Gbps Operation
- Non-Blocking Architecture Allows Each Output to be Connected to Any Input
- 30 ps of Deterministic Jitter
- Selectable Transmit Pre-Emphasis Per Lane
- Selectable Receive Equalization
- Available Packaging 64 Pin QFP
- Propagation Delay Times: 500 ps Typical
- Inputs Electrically Compatible With CML Signal Levels
- Operates From a Single 3.3-V Supply
- Ability to 3-STATE Outputs
- Integrated Termination Resistors
- I²C™ Control Interface

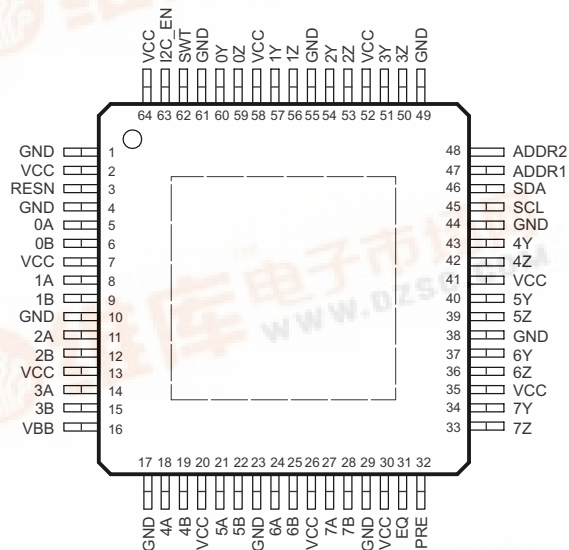
APPLICATIONS

- Clock Buffering/Clock MUXing
- Wireless Base Stations
- High-Speed Network Routing
- Telecom/Datacom
- XAUI 802.3ae Protocol Backplane Redundancy

DESCRIPTION

The SN65LVCP408 is a 8 × 8 non-blocking crosspoint switch in a flow-through pin-out allowing for ease in PCB layout. VML signaling is used to achieve a high-speed data throughput while using low power. Each of the output drivers includes a 8:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVCP408 incorporates 100-Ω termination resistors for those applications where board space is a premium. Built-in transmit pre-emphasis and receive equalization for superior signal integrity performance.

The SN65LVCP408 is characterized for operation from –40°C to 85°C. (See operating free air condition requirements)



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I²C is a trademark of Philips Electronics.

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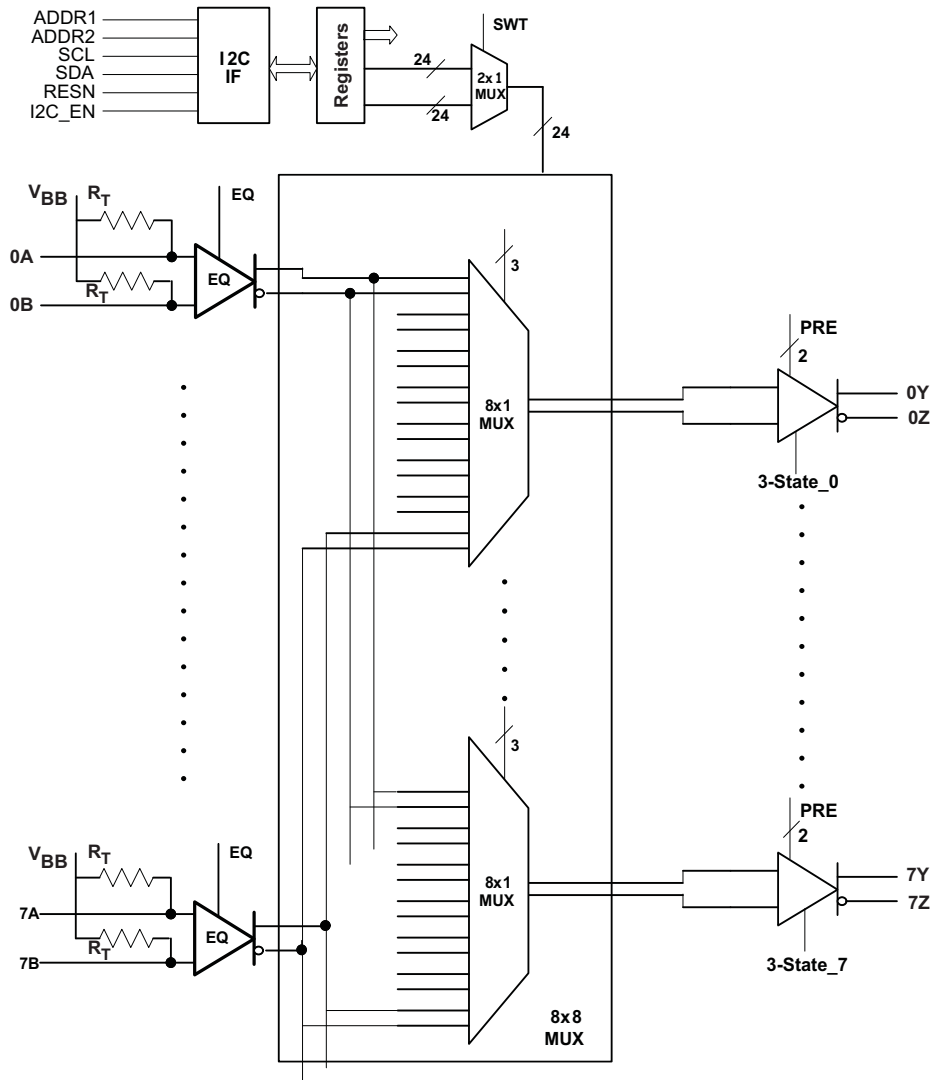




This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

LOGIC DIAGRAM



- A. V_{BB} : Receiver input internal biasing voltage (allows ac coupling)
- B. R_T : Internal 50- Ω receiver termination (100- Ω differential)

PIN FUNCTIONS

| Pin | | TYPE | DESCRIPTION |
|------------------------|--|---|---|
| NAME | NO. | | |
| High Speed I/O | | | |
| xA | 5, 8, 11, 14, 18, 21, 24, 27 | Differential Inputs (with 50-Ω termination to V _{bb}) xA=P; xB=N | Line Side Differential Inputs CML compatible |
| xB | 6, 9, 12, 15, 19, 22, 25, 28 | | |
| xY | 34, 37, 40, 43, 51, 54, 57, 60 | Differential Output xY=P; xZ=N | Switch Side Differential Outputs. VML |
| xZ | 33, 36, 39, 42, 50, 53, 56, 59 | | |
| Control Signals | | | |
| SCL | 45 | Inputs | I ² C Control Interface (SCL: Clock, SDA: Data, ADDR: Address) |
| SDA | 46 | | |
| ADDR1 | 47 | | |
| ADDR2 | 48 | | |
| EQ | 31 | Input | Equalization setting when I ² C is not enabled. EQ=0 for 13dB and setting EQ=1 for 9dB. |
| PRE | 32 | Input | Pre-Emphasis setting when I ² C is not enabled. PRE=0 for 0 dB and PRE=1 for 6 dB |
| I2C_EN | 63 | Input | Enables I ² C control interface I ² C_EN=1 for enable; When EN=0 then the PRE and EQ pins are used to set the Pre-Emphasis and Equalization settings rather than the I2C register map. When EN=0 the I ² C register map is still open for read and write operations. |
| SWT | 62 | Input | Enable switch event when toggled |
| RESN | 3 | Input (Active Low) | Configuration Reset. Resets I ² C register space (Active Low). Note upon device startup the RESN pin must be driven low to reset the device registers. |
| Power Supply | | | |
| VCC | 2, 7, 13, 20, 26, 30, 35, 41, 52, 58, 64 | Power | Power Supply 3.3v±5% |
| GND | 1,4, 10, 17, 23, 29, 38, 44, 49, 55, 61 | Ground | |
| V _{BB} | 16 | Input | Receiver input biasing voltage |
| PowerPAD™ | | Ground | The ground center pad of the package must be connected to GND plane. |

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

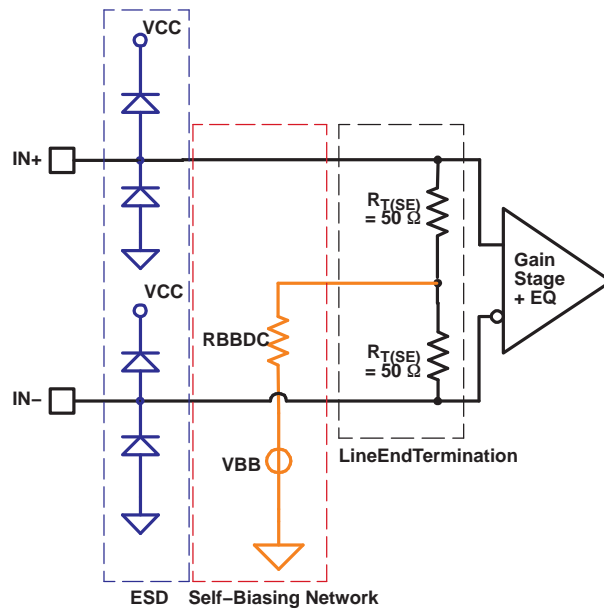


Figure 1. Equivalent Input Circuit Design

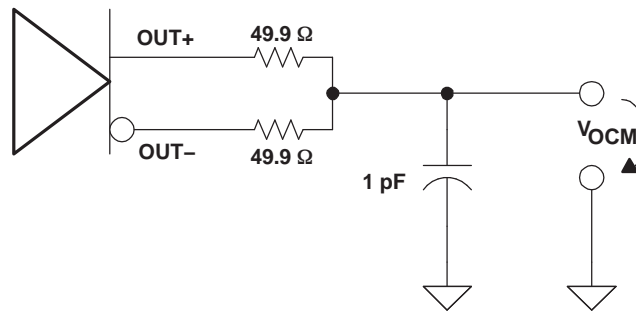


Figure 2. Common-Mode Output Voltage Test Circuit

AVAILABLE OPTIONS⁽¹⁾

| T _A | DESCRIPTION | PACKAGED DEVICE ⁽²⁾ |
|----------------|--------------------|--------------------------------|
| | | PAP (64 pin) |
| -40°C to 85°C | Serial multiplexer | SN65LVCP408 |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) The package is available taped and reeled. Add an R suffix to device types (e.g., SN65LVCP408PAP). Temperature range assumes 1 m/s airflow.

PACKAGE THERMAL CHARACTERISTICS

| PACKAGE THERMAL CHARACTERISTICS ⁽¹⁾ | | NOM | UNIT |
|--|---|------|------|
| θ _{JA} (junction-to-ambient) | 100LFM airflow is required otherwise a 4x4 thermal via array must be implemented with 6 layer or greater PCB. | 21.2 | °C/W |

- (1) See application note SPRA953 for a detailed explanation of thermal parameters (<http://www-s.ti.com/sc/psheets/spra953/spra953.pdf>).

ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | UNIT | |
|---|-------------------------------------|---|-------------------------------------|
| V _{CC} | Supply voltage range ⁽²⁾ | –0.5 V to 6 V | |
| Voltage range | | Control inputs, all outputs | –0.5 V to (V _{CC} + 0.5 V) |
| | | Receiver inputs | –0.5 V to 4 V |
| ESD | Human Body Model ⁽³⁾ | All pins | 6 kV |
| | Charged-Device Model ⁽⁴⁾ | All pins | 500 V |
| T _J | Maximum junction temperature | See Package Thermal Characteristics Table | |
| Moisture sensitivity level | | 2 | |
| Reflow temperature package soldering, 4 seconds | | 260°C | |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT | | |
|-----------------------------|---|--|-----|-----------------------|------|--|---|
| dR | Operating data rate | | | 4.25 | Gbps | | |
| V _{CC} | Supply voltage | 3.135 | 3.3 | 3.465 | V | | |
| V _{CC(N)} | Supply voltage noise amplitude | 10 Hz to 2.125 GHz | | 20 | mV | | |
| T _J | Junction temperature | | | 125 | °C | | |
| T _A | Operating free-air temperature ⁽¹⁾ | Assumes 4x4 thermal via array is implemented with 6 layer or greater PCB otherwise 100LFM airflow is required. | | –40 | 85 | °C | |
| DIFFERENTIAL INPUTS | | | | | | | |
| V _{ID} | Receiver peak-to-peak differential input voltage ⁽²⁾ | dR _(in) ≤ 4.25 Gbps | | 100 | 1750 | mV _{PP} | |
| | | 1.25 Gbps < dR _(in) ≤ 4.25 Gbps | | 100 | 1560 | mV _{PP} | |
| | | dR _(in) > 4.25 Gbps | | 100 | 1000 | mV _{PP} | |
| V _{ICM} | Receiver common-mode input voltage | Note: for best jitter performance ac coupling is recommended. | | 1.5 | 1.6 | V _{CC} – $\frac{ V_{ID} }{2}$ | V |
| CONTROL INPUTS | | | | | | | |
| V _{IH} | High-level input voltage | 2 | | V _{CC} + 0.3 | V | | |
| V _{IL} | Low-level input voltage | –0.3 | | 0.8 | V | | |
| DIFFERENTIAL OUTPUTS | | | | | | | |
| R _L | Differential load resistance | 80 | 100 | 120 | Ω | | |

- (1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.
- (2) Differential input voltage V_{ID} is defined as |IN+ – IN–|.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|-----------------------------|---|---|---|------|------------------|------|
| DIFFERENTIAL INPUTS | | | | | | |
| V _{IT+} | Positive going differential input high threshold | | | 50 | mV | |
| V _{IT-} | Negative going differential input low threshold | -50 | | | mV | |
| A _(EQ) | Equalizer gain | at 1.875 GHz (EQ=1) | | 9 | dB | |
| R _{T(D)} | Termination resistance, differential | 80 | 100 | 120 | Ω | |
| V _{BB} | Open-circuit Input voltage (input self-bias voltage) | AC-coupled inputs | | 1.6 | V | |
| R _(BBDC) | Biasing network dc impedance | | | 30 | kΩ | |
| R _(BBAC) | Biasing network ac impedance | 375 MHz | | 42 | Ω | |
| | | 2.125 GHz | | 8.4 | | |
| DIFFERENTIAL OUTPUTS | | | | | | |
| V _{ODH} | High-level output voltage | R _L = 100 Ω ±1%, Pre-Emph=0 dB | | 650 | mV _{PP} | |
| V _{ODL} | Low-level output voltage | | | -650 | mV _{PP} | |
| V _{ODB} | Output differential voltage without preemphasis ⁽²⁾ | | | 1000 | 1300 | 1500 |
| V _{OCM} | Output common mode voltage | | | 1.8 | V | |
| ΔV _{OC(SS)} | Change in steady-state common-mode output voltage between logic states | See Figure 2 | | 1 | mV | |
| V _(PE) | Output preemphasis voltage ratio, $\frac{V_{ODB(PP)}}{V_{ODPE(PP)}}$ | R _L = 100 Ω ±1%; x = L or S; See Figure 3 | | 0 | dB | |
| | | | | 3 | | |
| | | | | 6 | | |
| | | | | 10 | | |
| t _(PRE) | Preemphasis duration measurement | Output preemphasis is set to 10 dB during test Measured with a 100-MHz clock signal; R _L = 100 Ω ±1%, See Figure 4 | | 175 | ps | |
| r _o | Output resistance | Differential on-chip termination between OUT+ and OUT- | | 100 | Ω | |
| CONTROL INPUTS | | | | | | |
| I _{IH} | High-level Input current | VIN = VCC | | 5 | μA | |
| I _{IL} | Low-level Input current | VIN = GND | | -125 | -90 | μA |
| R _(PU) | Pullup resistance | | | 35 | kΩ | |
| POWER CONSUMPTION | | | | | | |
| P _D | Device power dissipation | All outputs terminated 100 Ω | PRBS 2 ⁷⁻¹ pattern at 4.25 Gbps | 1.52 | W | |
| P _Z | Device power dissipation in 3-State | All outputs in 3-state | | 864 | mW | |
| I _{CC} | Device current consumption | All outputs terminated 100 Ω | | 440 | mA | |

(1) All typical values are at T_A = 25°C and V_{CC} = 3.3 V supply unless otherwise noted. They are for reference purposes and are not production tested.

(2) Differential output voltage V_(ODB) is defined as | OUT+ – OUT- |.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------------------------|---|---|-------------------------------|---|-----|--------------------|-----|--------|
| MULTIPLEXER | | | | | | | | |
| $t_{(SM)}$ | Multiplexer switch time | Multiplexer to valid output | | | | | 15 | ns |
| DIFFERENTIAL OUTPUTS | | | | | | | | |
| t_{PLH} | Low-to-high propagation delay | Propagation delay input to output, See Figure 6 | | | | 0.5 | 0.7 | ns |
| t_{PHL} | High-to-low propagation delay | | | | | 0.5 | 0.7 | ns |
| t_r | Rise time | 20% to 80% of $V_{O(DB)}$; Test Pattern: 100-MHz clock signal; See Figure 5 and Figure 8 | | | | 90 | | ps |
| t_f | Fall time | | | | | 90 | | ps |
| $t_{sk(p)}$ | Pulse skew, $ t_{PHL} - t_{PLH} ^{(2)}$ | | | | | | 20 | ps |
| $t_{sk(o)}$ | Output skew ⁽³⁾ | All outputs terminated with 100 Ω | | | | 25 | 75 | ps |
| $t_{sk(pp)}$ | Part-to-part skew ⁽⁴⁾ | | | | | | 150 | ps |
| t_{zd} | 3-State switch time to Disable | Assumes 50 Ω to V_{cm} and 150 pF load on each output; Tested using I2C | | | | | 30 | ns |
| t_{ze} | 3-State switch time to Enable | Assumes 50 Ω to V_{cm} and 150 pF load on each output; Tested using I2C | | | | | 20 | ns |
| RJ | Device random jitter, rms | See Figure 8 for test circuit. BERT setting 10^{-15} Alternating 10-pattern. | | | | 0.8 | 2 | ps-rms |
| DJ | Intrinsic deterministic device jitter ⁽⁵⁾ , peak-to-peak | 0 dB preemphasis See Figure 8 for the test circuit. | PRBS 2 ⁷⁻¹ pattern | 4.25 Gbps | | | 30 | ps |
| | Absolute deterministic output jitter ⁽⁶⁾ , peak-to-peak | 0 dB preemphasis See Figure 8 for the test circuit. | PRBS 2 ⁷⁻¹ pattern | 1.25Gbps; EQ=13dB Over 25-inch FR4 trace 4.25 Gbps; EQ=13dB Over FR4 trace 2-inch to 43 inches long | | 15 | 40 | ps |

(1) All typical values are at 25°C and with 3.3 V supply unless otherwise noted.

(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.

(3) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any two outputs of a single device.

(4) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(5) The SN65LVCP408 built-in passive input equalizer compensates for ISI. For a 25-inch FR4 transmission line with 8-mil trace width, the LVCP408 typically reduces jitter by 29 ps from the device input to the device output.

(6) Absolute deterministic output jitter reflects the deterministic jitter measured at the SN65LVCP408 output. The value is a real measured value with a Bit error tester as described in [Figure 8](#). The absolute DJ reflects the sum of all deterministic jitter components accumulated over the link: $DJ_{(absolute)} = DJ_{(Signal\ generator)} + DJ_{(transmission\ line)} + DJ_{(intrinsic(LVCP408))}$.

PARAMETER MEASUREMENT INFORMATION

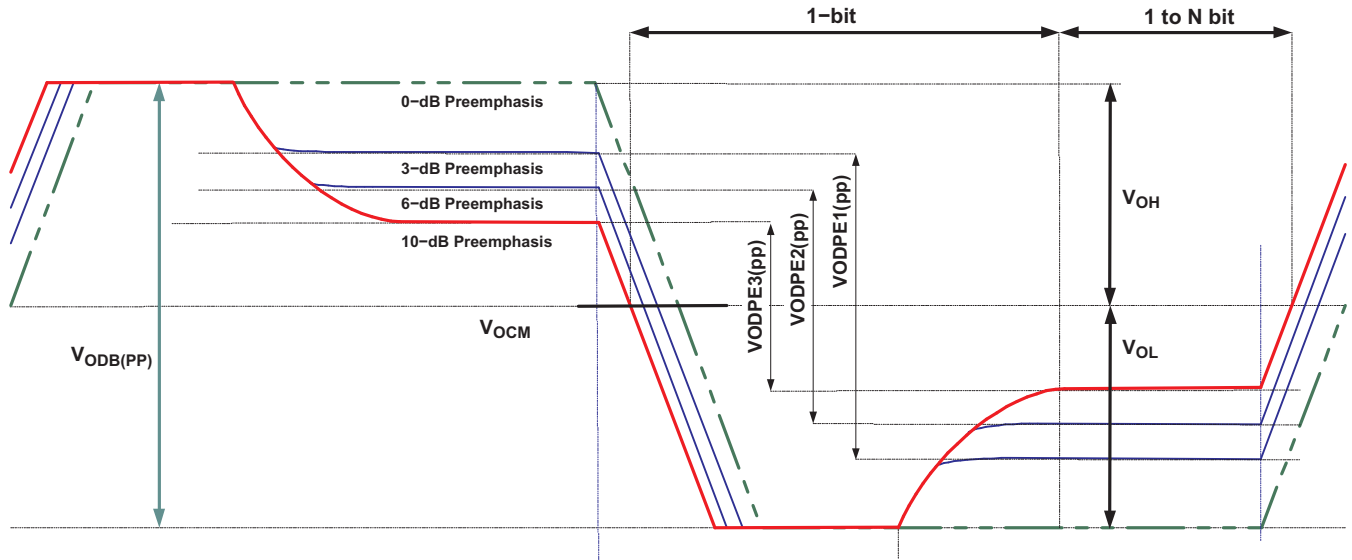


Figure 3. Preemphasis and Output Voltage Waveforms and Definitions

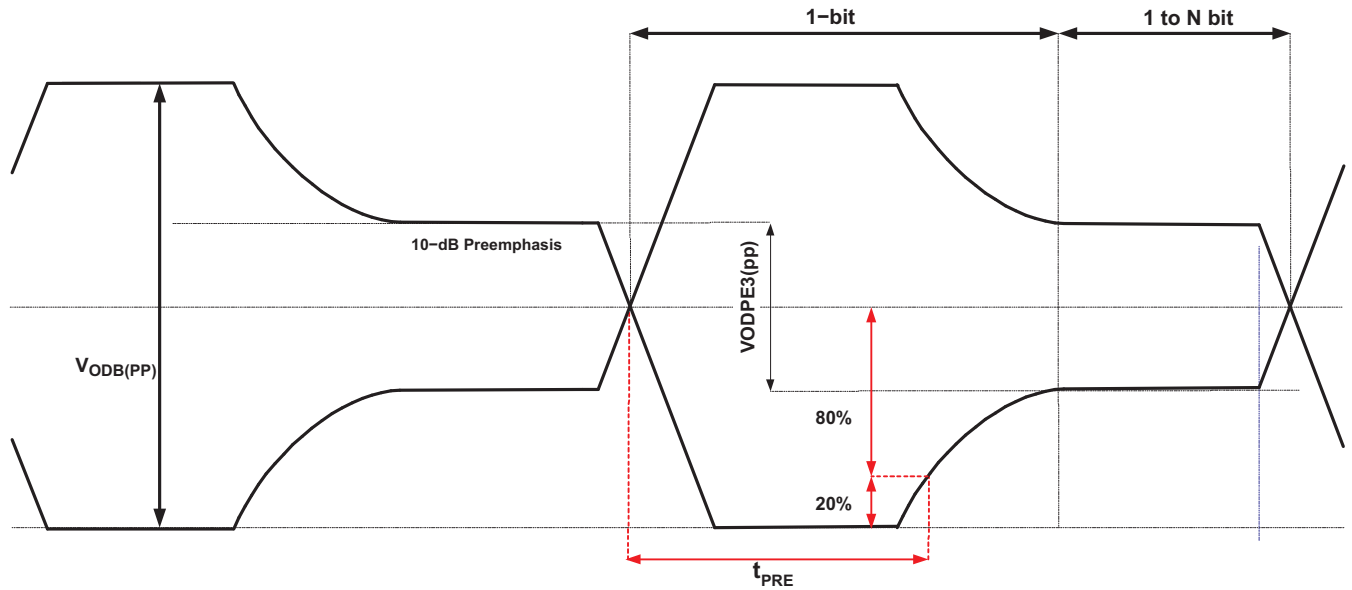


Figure 4. t_{PRE} Preemphasis Duration Measurement

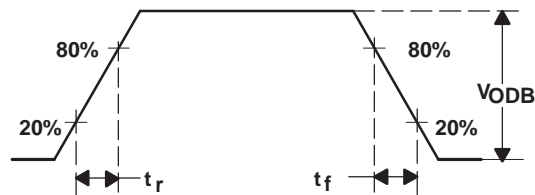


Figure 5. Driver Output Transition Time

PARAMETER MEASUREMENT INFORMATION (continued)

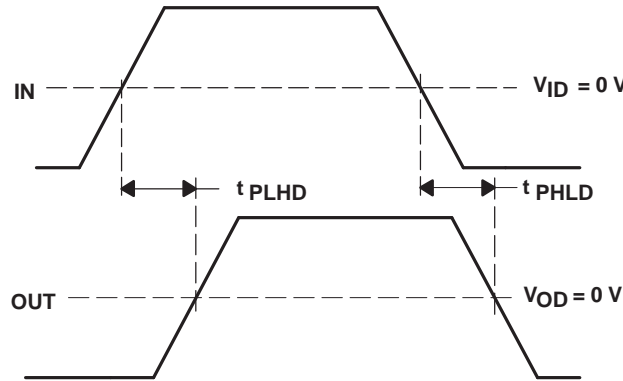
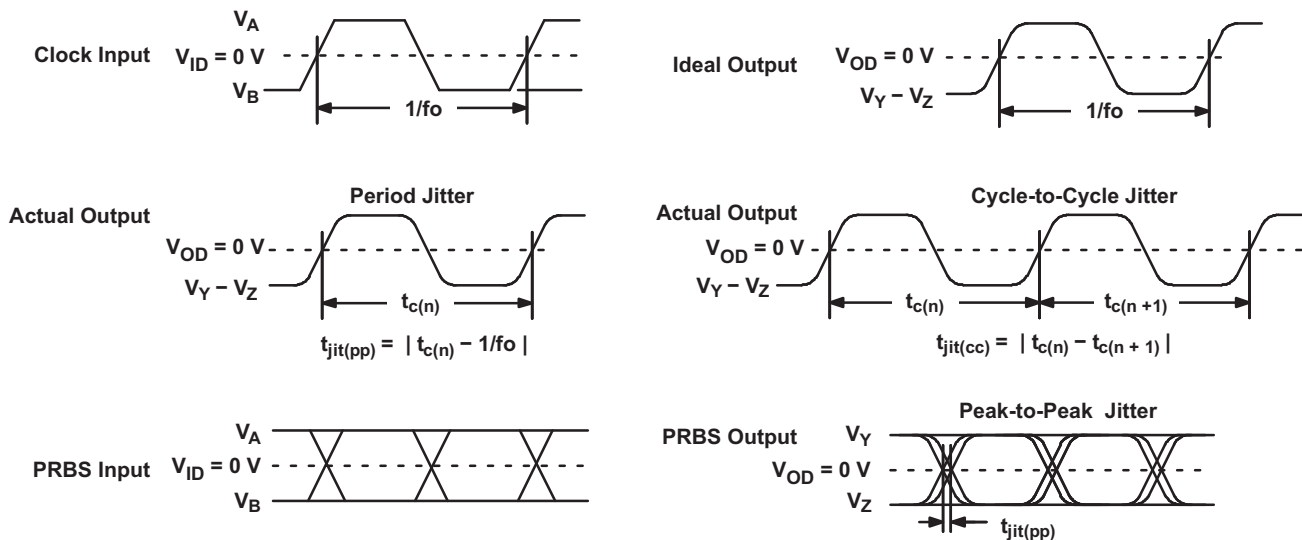
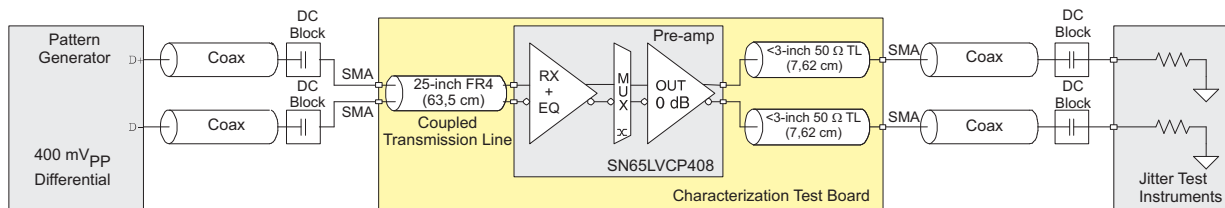


Figure 6. Propagation Delay Input to Output



- A. All input pulses are supplied by an Agilent 81250 Stimulus System.
- B. The measurement is made with the AgilentParBert measurement software.

Figure 7. Driver Jitter Measurement Waveforms



For the rise/fall time measurements, the 25-inch FR4 transmission line is removed.

Figure 8. AC Test Circuit — Jitter and Output Rise Time Test Circuit

The SN65LVCP408 input equalizer provides frequency gain to compensate for frequency loss of a shorter backplane transmission line. For characterization purposes, a 25-inch (63,5 cm) FR-4 coupled transmission line is used in place of the backplane trace. The 25-inch trace provides roughly 5 dB of attenuation between 375 MHz and 2.125 GHz, representing closely the characteristics of a short backplane trace. The loss tangent of the FR4 in the test board is 0.018 with an effective $\epsilon(r)$ of 4.1.

TYPICAL DEVICE BEHAVIOR

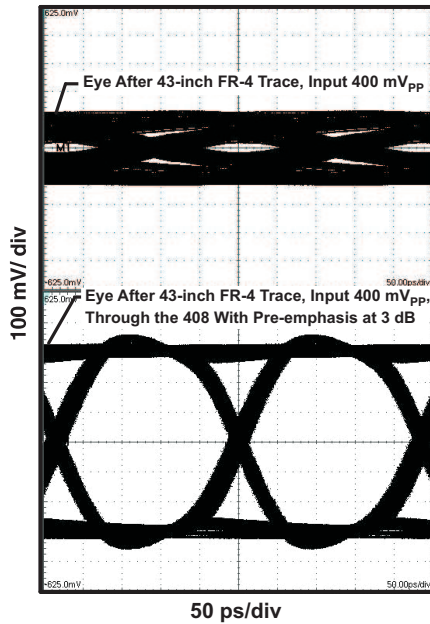


Figure 9. Data Input and Output Pattern

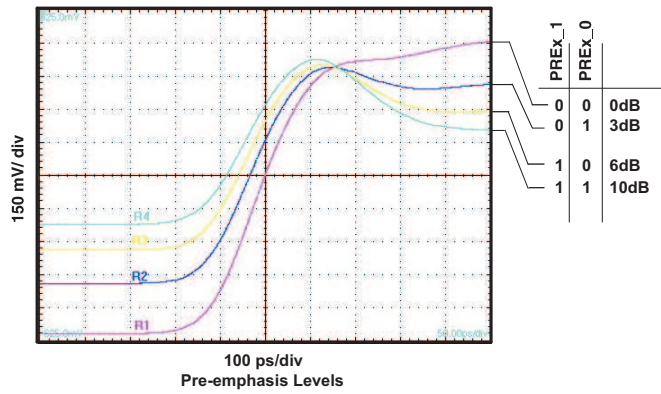


Figure 10. Preemphasis Signal Shape

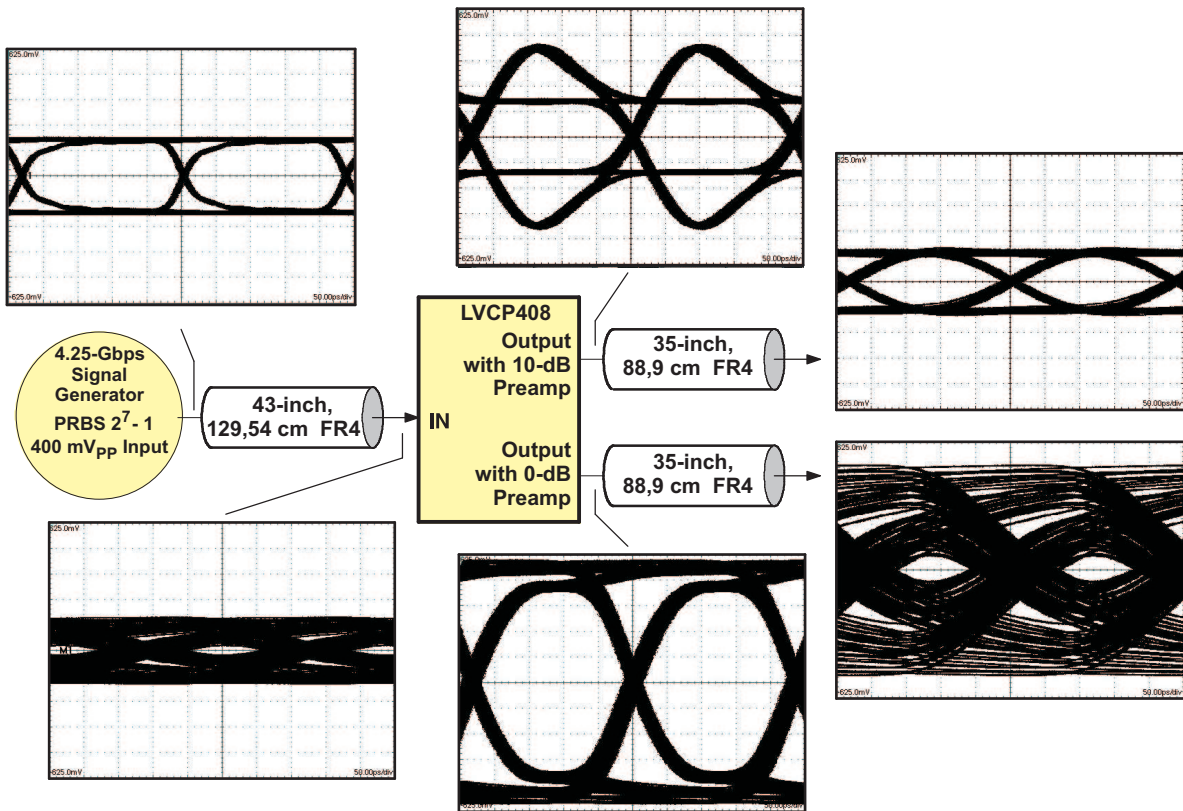


Figure 11. Data Output Pattern

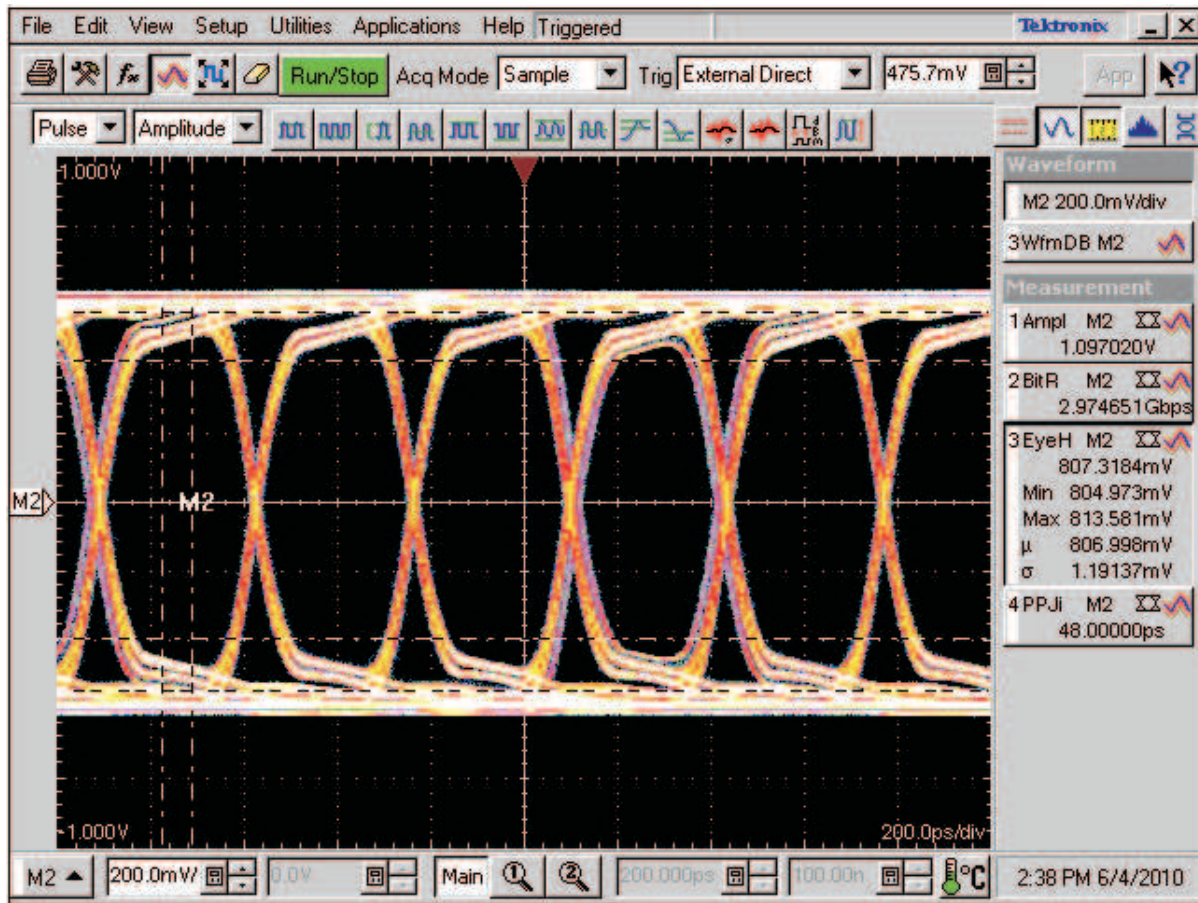


Figure 12. SN65LVCP408 Passing 3G (2.97Gbps) SDI Pathological Data Pattern DC Coupled Environment

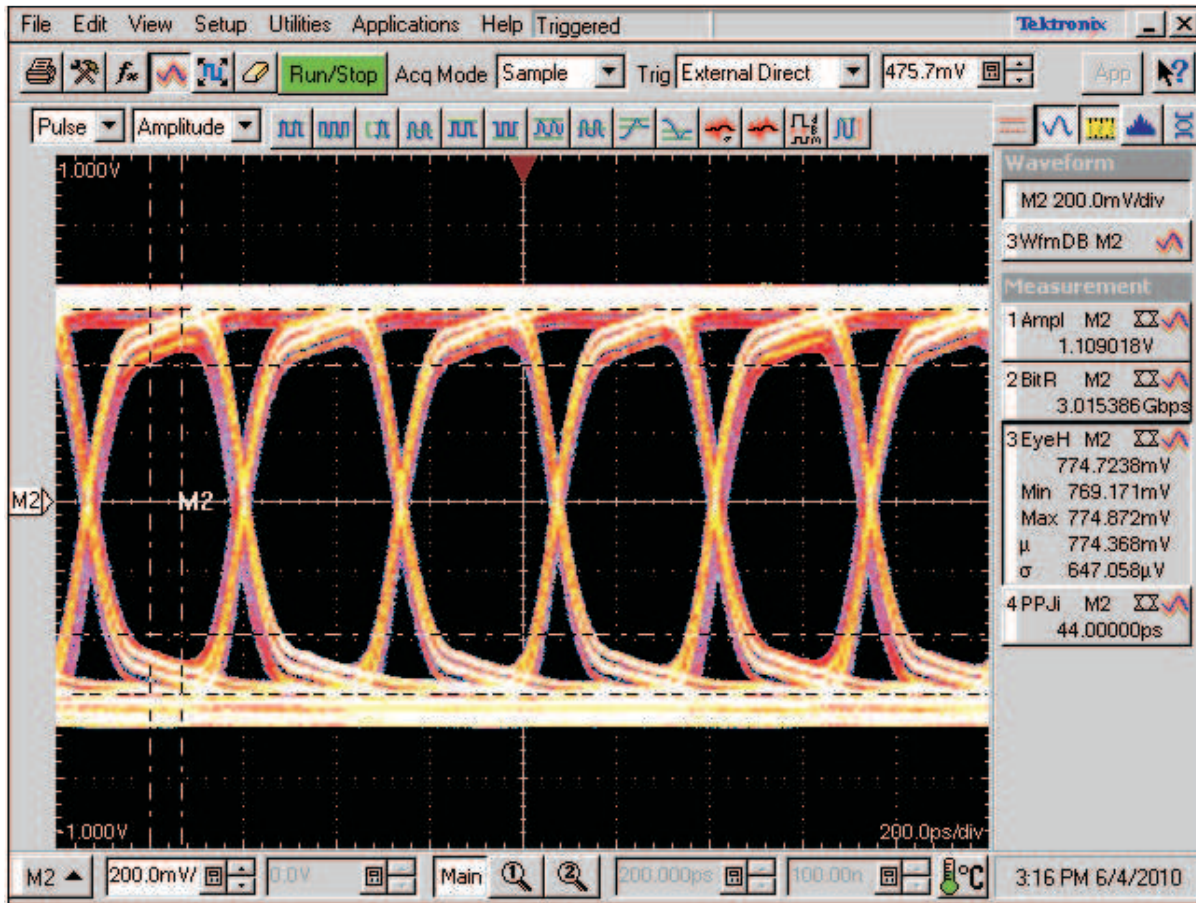


Figure 13. SN65LVCP408 Passing 3G (2.97Gbps) SDI Pathological Data Pattern AC Coupled Environment

TYPICAL CHARACTERISTICS

DETERMINISTIC OUTPUT JITTER vs DATA RATE

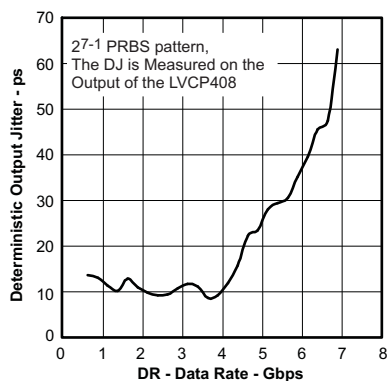


Figure 14.

DETERMINISTIC OUTPUT JITTER vs DIFFERENTIAL INPUT AMPLITUDE

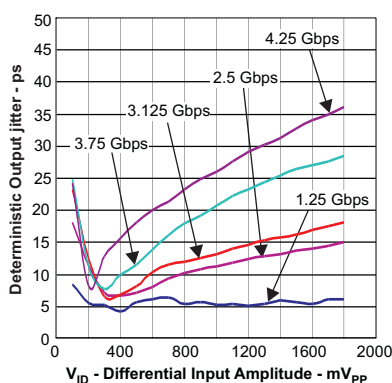


Figure 15.

DIFFERENTIAL OUTPUT VOLTAGE vs DATA RATE

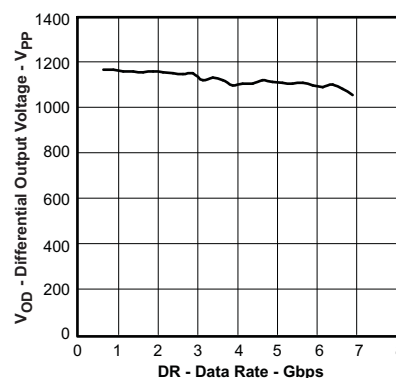


Figure 16.

SUPPLY NOISE vs DETERMINISTIC JITTER vs DATA RATE

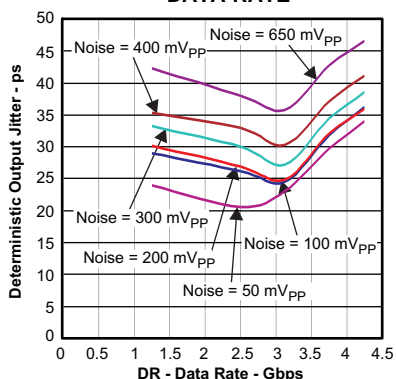


Figure 17.

DETERMINISTIC OUTPUT JITTER vs COMMON-MODE INPUT VOLTAGE

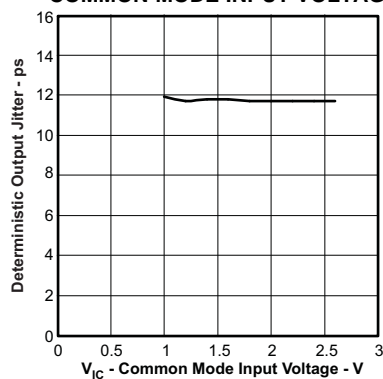


Figure 18.

I²C CONTROL INTERFACE

I²C Interface Notes

The I²C interface is used to access the internal registers of the SN65LVCP408. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device. The SN65LVCP408 works as a slave and supports the standard mode transfer (100 kbps).

The basic I²C start and stop access cycles are shown in Figure 19. The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

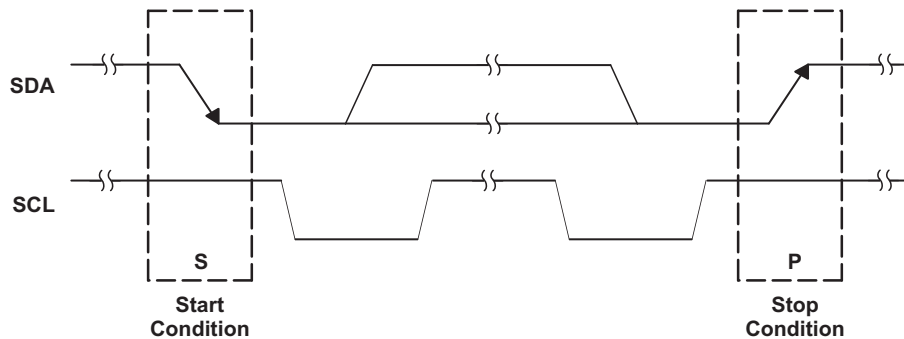


Figure 19. I²C Start and Stop Conditions

General I²C Protocol

- The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 19. All I²C-compatible devices should recognize a start condition.
- The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 20). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 21) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 22).
- To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 19). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.
- All bytes are transmitted most significant bit first.

Table 1. I²C Timing

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|------------------------|-----|-----|-----|------|
| f _{SCL} | SCL clock frequency for internal register | Local I ² C | | | 100 | kHz |
| t _{W(L)} | Clock LOW period for I ² C register | Local I ² C | 4.7 | | | μs |
| t _{W(H)} | Clock HIGH period for internal register | Local I ² C | 4 | | | μs |
| t _{SU1} | Internal register setup time, SDA to SCL | Local I ² C | 250 | | | μs |
| t _{h(1)} | Internal register hold time, SCL to SDA | Local I ² C | 0 | | | μs |
| t _(buf) | Internal register bus free time between STOP and START | Local I ² C | 4.7 | | | μs |
| t _{SU(2)} | Internal register setup time, SCL to START | Local I ² C | 4.7 | | | μs |
| t _{h(2)} | Internal register hold time, START to SCL | Local I ² C | 4 | | | μs |
| t _{SU(3)} | Internal register hold time, SCL to STOP | Local I ² C | 4 | | | μs |

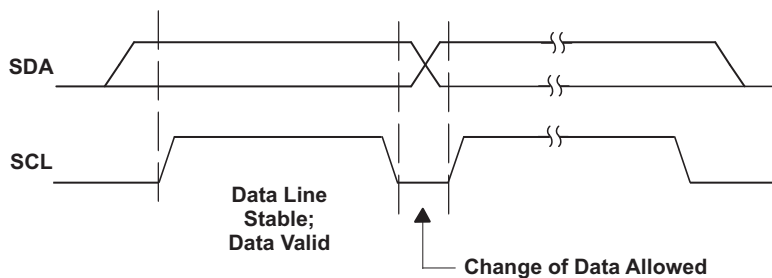


Figure 20. I²C Bit Transfer

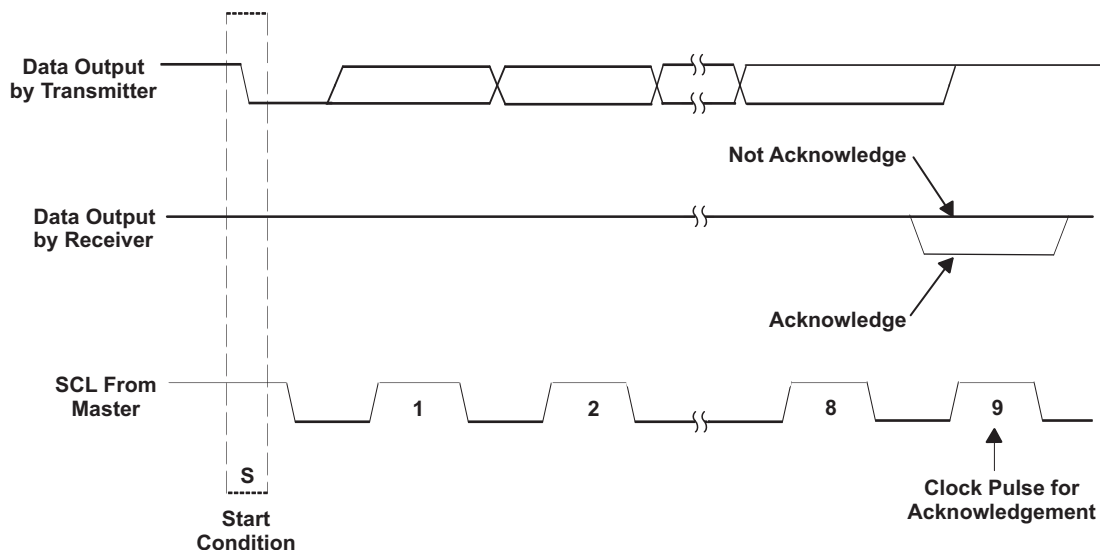


Figure 21. I²C Acknowledge

Note: Following power up, this device must be reset.

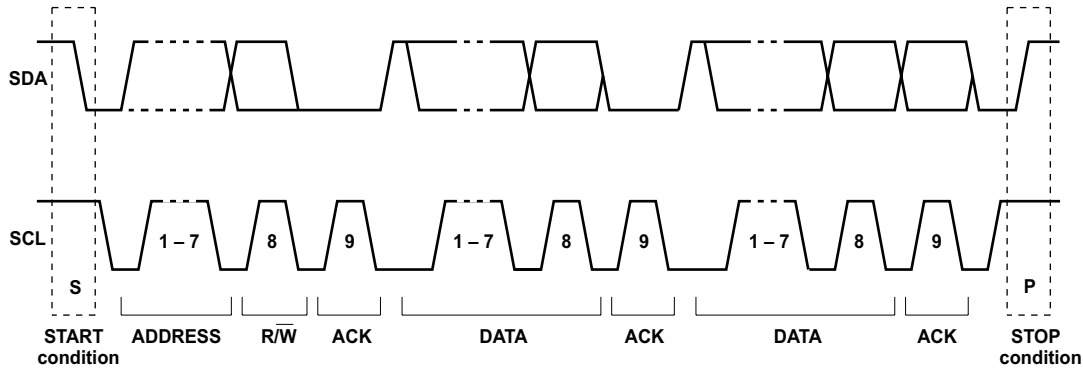


Figure 22. I²C Address and Data Cycles

During a write cycle, the slave sends an acknowledge (A) after every byte that follows the device address. The first byte following the device address is the register address, which maps to the register addresses specific to the device. The second byte following the device address is the data byte to be written at the register address (see Figure 23). If only the register address is to be written for a subsequent read sequence, the data byte is omitted and the sequence ends with a Stop (see Figure 24) or a repeated Start after the register address byte (see Figure 26). If multiple data bytes are to be written at subsequent register addresses, the master may continue to send data bytes after each slave acknowledge, and the slave device automatically increments the register address. Note that the master must not drive the SDA signal line during the slave acknowledge since the slave is in control of the SDA bus and may be holding it low.

During a read cycle, the slave acknowledges the initial address byte if it decodes the device address as its own device address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. The first byte received by the master is the data stored at the register address, while subsequent bytes are data stored at incrementing register addresses. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the Stop (P) condition. This sequence terminates a read cycle as shown in Figure 25. A combined format is when the read cycle is preceded by a write cycle for setting the register address, and is shown in Figure 26.

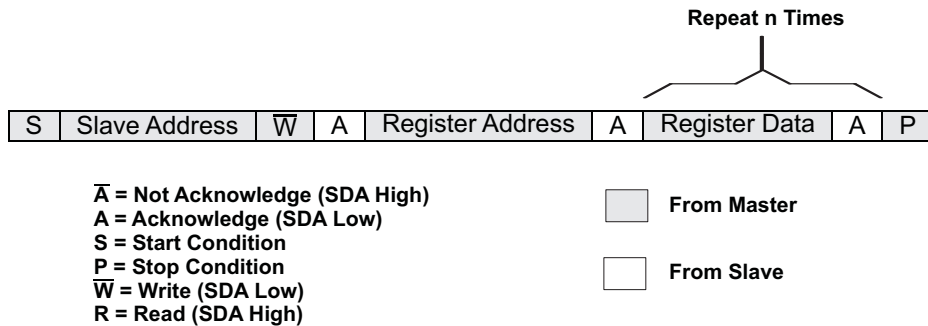


Figure 23. I²C Write Cycle with Register Address and Data

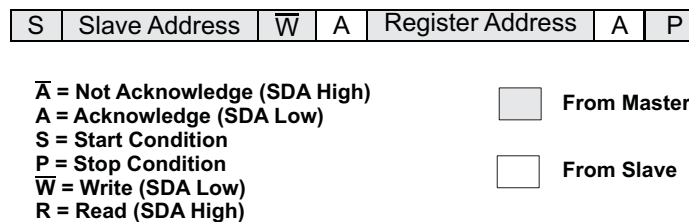


Figure 24. I²C Write Cycle with Register Address Only

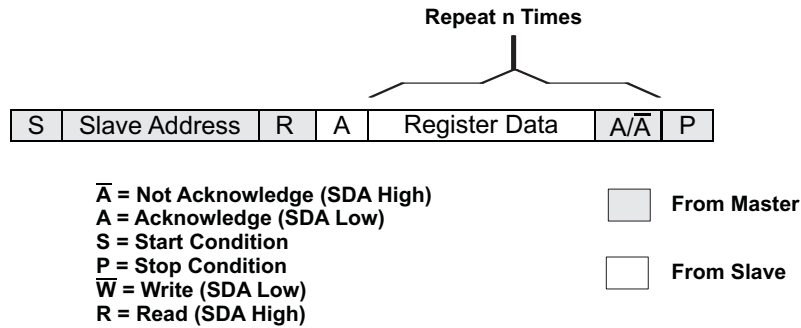


Figure 25. I²C Read Cycle

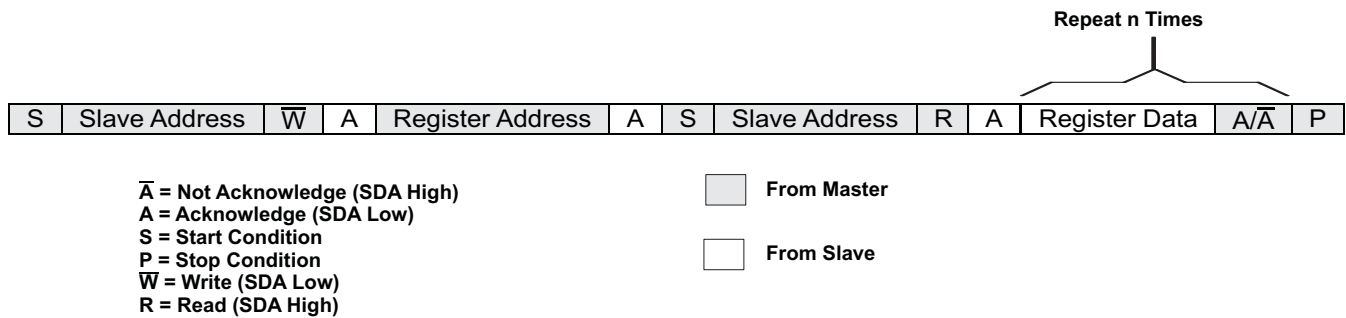


Figure 26. I²C Combined Format Write/Read Cycle

Slave Address

Both SDA and SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The slave address is the first 7 bits received following the START condition from the master device. The first 5 Bits (MSBs) of the address are factory preset to 01011. The next two bits of the SN65LVCP408 address are controlled by the logic levels appearing on the ADDR2 and ADDR1 pins. The ADDR2 and ADDR1 address inputs can be connected to VCC for logic 1, GND for logic 0, or can be actively driven by TTL/CMOS logic levels. The device addresses are set by the state of these pins and are not latched. Thus a dynamic address control system could be utilized to incorporate several devices on the same system. Up to four SN65LVCP408 devices can be connected to the same I²C-Bus without requiring additional glue logic. Table 2 lists the possible addresses for the SN65LVCP408.

Table 2. Slave Addresses

| Fixed Address | | | | | Selectable with Address Pins | |
|---------------|-------|-------|-------|-------|------------------------------|---------------|
| Bit 6 (MSB) | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1(addr2) | Bit 0 (addr1) |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |

Note: Following power up, this device must be reset.

Table 3. Port Register Addresses

| Register Name | Register Address |
|---------------------|------------------------|
| Output Port 0 | 0000 0000 |
| Output Port 1 | 0000 0001 |
| Output Port 2 | 0000 0010 |
| Output Port 3 | 0000 0011 |
| Output Port 4 | 0000 0100 |
| Output Port 5 | 0000 0101 |
| Output Port 6 | 0000 0110 |
| Output Port 7 | 0000 0111 |
| Input Port 0 | 0000 1000 |
| Input Port 1 | 0000 1001 |
| Input Port 2 | 0000 1010 |
| Input Port 3 | 0000 1011 |
| Input Port 4 | 0000 1100 |
| Input Port 5 | 0000 1101 |
| Input Port 6 | 0000 1110 |
| Input Port 7 | 0000 1111 |
| Switch Control | 0001 0000 |
| Reserved for TI use | 0001 0001 to 0001 1010 |

Table 4. Output Port Control Registers

| Bit | Function | Default | Note | Access |
|-----|------------------------|---------|--|--------|
| 7 | Input Port Select No.1 | 0 | Selects the desired input port to be used by the output port. Defaults to same port number as the output port. Valid values are : 000 for port 1, 001 for port 1...etc | R/W |
| 6 | | 0 | | |
| 5 | | 0 | | |
| 4 | Pre-Emphasis | 00 | Pre-Emphasis setting. Valid Values are: 00 = 0 dB; 01 = 3 dB; 10 = 6dB, and 11 = 10dB; Note When EN=0 then the PRE pin is used to set the Pre-Emphasis setting rather than the I2C register map. | |
| 3 | | | | |
| 2 | Port 3-State | 0 | 3-State Off = 0; 3-State On=1 | R |
| 1 | RSVD | 0 | Reserved | |
| 0 | RSVD | 0 | Reserved | |

Table 5. Input Port Control Registers

| Bit | Function | Default | Note | Access |
|-----|------------------------|---------|---|--------|
| 7 | Rx Equalization Select | 0 | Rx Equalization Setting; 0 = 13dB ; 1 = 9dB; Note When EN=0 then the EQ pin is used to set the Equalization setting rather than the I2C register map. | R/W |
| 6 | Input Port Select No.2 | 0 | Selects the desired input port to be used by the output port when the switch event is triggered. Defaults to same port number as the output port. Valid values are : 000 for port 0, 001 for port 1...etc | |
| 5 | | 0 | | |
| 4 | | 0 | | R |
| 3 | RSVD | 0 | Reserved | |
| 2 | RSVD | 0 | Reserved | |
| 1 | RSVD | 0 | Reserved | |
| 0 | RSVD | 0 | Reserved | |

Note: Following power up, this device must be reset.

Table 6. Switch Control

| Bit | Function | Default | Note | Access |
|-----|-----------------------------|---------|--|--------|
| 7 | Enable Switch Via Pin | 0 | 0= Switch Via I ² C bit is used to enable the switch event; 1 = Switch via SWT pin; When SWT is logic 0, Port Select No. 1 settings will be used. When SWT is logic 1, the Port Select No. 2 settings will be used. The Switch Via i2C setting will be ignored. | R/W |
| 6 | Switch Via I ² C | 0 | Selects between Port Select No. 1 and No. 2 when enable Switch Via Pin is 0. 0= Port Select No. 1, 1=Port Select No. 2 | |
| 5 | RSVD | 0 | Reserved | R |
| 4 | RSVD | 0 | Reserved | |
| 3 | RSVD | 0 | Reserved | |
| 2 | RSVD | 0 | Reserved | |
| 1 | RSVD | 0 | Reserved | |
| 0 | RSVD | 0 | Reserved | |

Table 7. Reserved for TI Use

| Bit | Function | Default | Note | Access |
|-----|----------|---------|------------------------------------|--------|
| 7:0 | RSVD | - | Read only value is indeterministic | R |

Switching Options

For each output port, users can select two possible input port selection profiles (i.e. sources that indicate which input port to use for the output). Input port select No. 1 I²C™ register bits are used to select the configuration of each output port that is used for default operation. (Note: on power up and after resetting the I2C register space with the RESN pin, each output port is mapped to its matching input port. For example, output port 0 is mapped to input port 0, and output port 1 is mapped to input port 1, etc.). Input Port Select No. 2 registers are used to select the secondary output port configuration that is used when the switch event is triggered.

Triggering Switch Event

Switching between the active output port configuration and the secondary output port configuration (configuration selected with Input Port Select No 2 registers) is accomplished in two ways:

1. The switch event can be triggered using the I²C register bit Switch Via I²C and setting it to 1 (high).
2. If the switch event needs to occur faster than the I²C access allows, then users have the option to use the SWT pin (pin #62) to trigger the switch from port configuration No. 1 to port configuration No. 2. For this option, users should set the Enable Switch Via I²C register bit to 1 upon initial start up. The SWT pin should be logic high state to initiate the switch. Changing the logic states of the SWT pin causes the port configurations to move between the two port configuration options.

APPLICATION INFORMATION

BANDWIDTH REQUIREMENTS

Error free transmission of data over a transmission line has specific bandwidth demands. It is helpful to analyze the frequency spectrum of the transmit data first. For an 8B10B coded data stream at 3.75 Gbps of random data, the highest bit transition density occurs with a 1010 pattern (1.875 GHz). The least transition density in 8B10B allows for five consecutive ones or zeros. Hence, the lowest frequency of interest is 1.875 GHz/5 = 375 MHz. Real data signals consist of higher frequency components than sine waves due to the fast rise time. The faster the rise time, the more bandwidth becomes required. For 80-ps rise time, the highest important frequency component is at least $0.6/(\pi \times 80 \text{ ps}) = 2.4 \text{ GHz}$. [Figure 27](#) shows the Fourier transformation of the 375-MHz and 1.875-GHz trapezoidal signal.

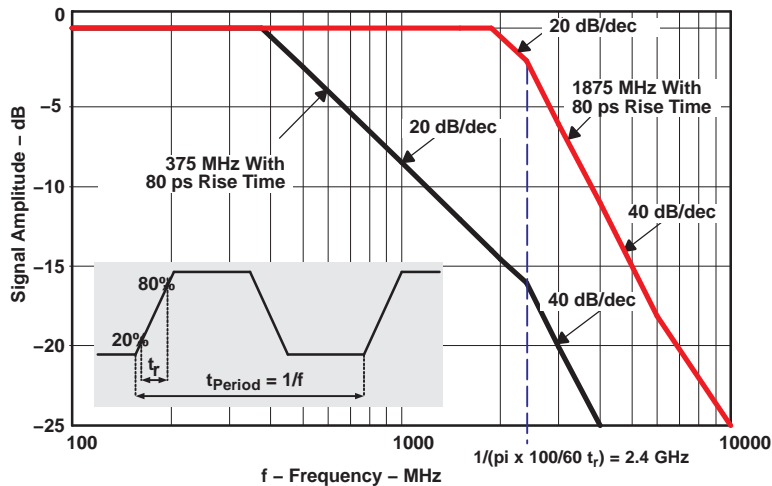


Figure 27. Approximate Frequency Spectrum of the Transmit Output Signal With 80 ps Rise Time

The spectrum analysis of the data signal suggests building a backplane with little frequency attenuation up to 2 GHz. This is achievable only with expensive, specialized PCB material. To support material like FR4, a compensation technique is necessary to compensate for backplane imperfections.

EXPLANATION OF EQUALIZATION

Backplane designs differ widely in size, layer stack-up, and connector placement. In addition, the performance is impacted by trace architecture (trace width, coupling method) and isolation from adjacent signals. Common to most commercial backplanes is the use of FR4 as board material and its related high-frequency signal attenuation. Within a backplane, the shortest to longest trace lengths differ substantially – often ranging from 8 inches up to 40 inches. Increased loss is associated with longer signal traces. In addition, the backplane connector often contributes a good amount of signal attenuation. As a result, the frequency signal attenuation for a 300-MHz signal might range from 1 dB to 4 dB while the corresponding attenuation for a 2-GHz signal might span 6 dB to 24 dB. This frequency dependent loss causes distortion jitter on the transmitted signal. Each LVCP408 receiver input incorporates an equalizer and compensates for such frequency loss. The SN65LVCP408 equalizer provides 5 dB of frequency gain between 375 MHz and 1.875 GHz, compensating roughly for 20 inches of FR4 material with 8-mil trace width. Distortion jitter improvement is substantial, often providing more than 30-ps jitter reduction. The 5-dB compensation is sufficient for most short backplane traces. For longer trace lengths, it is recommended to enable transmit preemphasis in addition.

SETTING THE PREEMPHASIS LEVEL

The receive equalization compensates for ISI. This reduces jitter and opens the data eye. In order to find the best preemphasis setting for each link, calibration of every link is recommended. Assuming each link consists of a transmitter (with adjustable pre-emphasis such as LVCP408) and the LVCP408 receiver, the following steps are necessary:

1. Set the transmitter and receiver to 0-dB preemphasis; record the data eye on the LVCP408 receiver output.
2. Increase the transmitter preemphasis until the data eye on the LVCP408 receiver output looks the cleanest.

REVISION HISTORY

| Changes from Original (June 2009) to Revision A | Page |
|--|------|
| • Added Figures 12 (Figure 11a) and Figure 13 (Figure 11b) | 11 |



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PACKAG

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|---------------|
| SN65LVCP408PAPR | ACTIVE | HTQFP | PAP | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C |
| SN65LVCP408PAPT | ACTIVE | HTQFP | PAP | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com> for more information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all RoHS materials, with the exception of lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for high temperature soldering processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based eutectic solder used between the leadframe leads and the die.

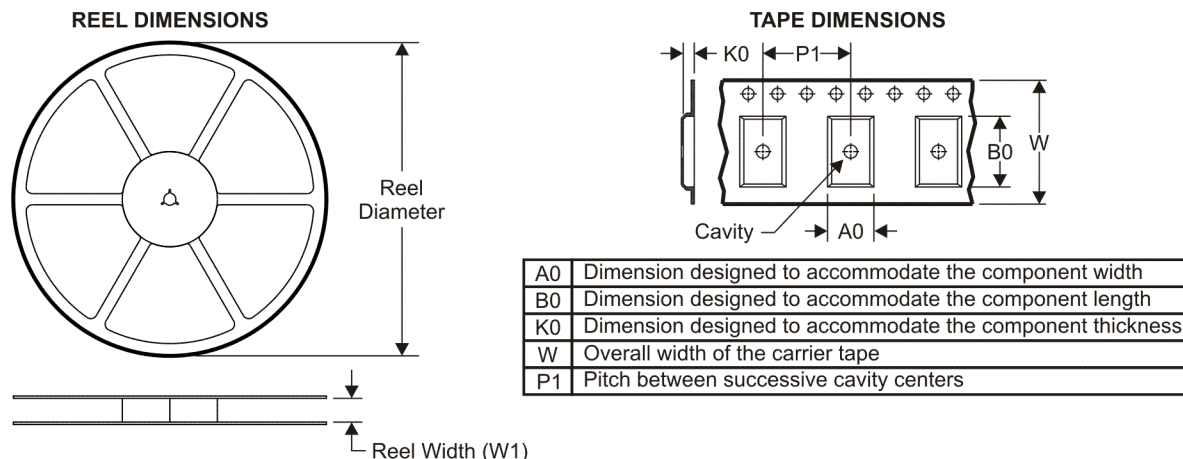
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (unless otherwise designated in homogeneous material).

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

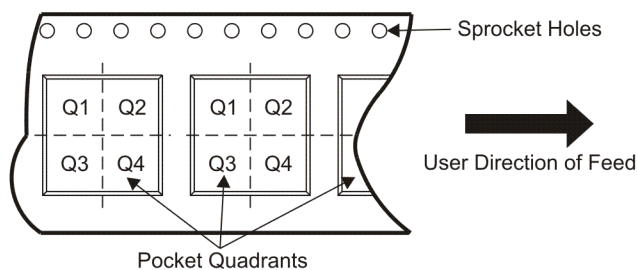
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LVCP408PAPR | HTQFP | PAP | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |
| SN65LVCP408PAPT | HTQFP | PAP | 64 | 250 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

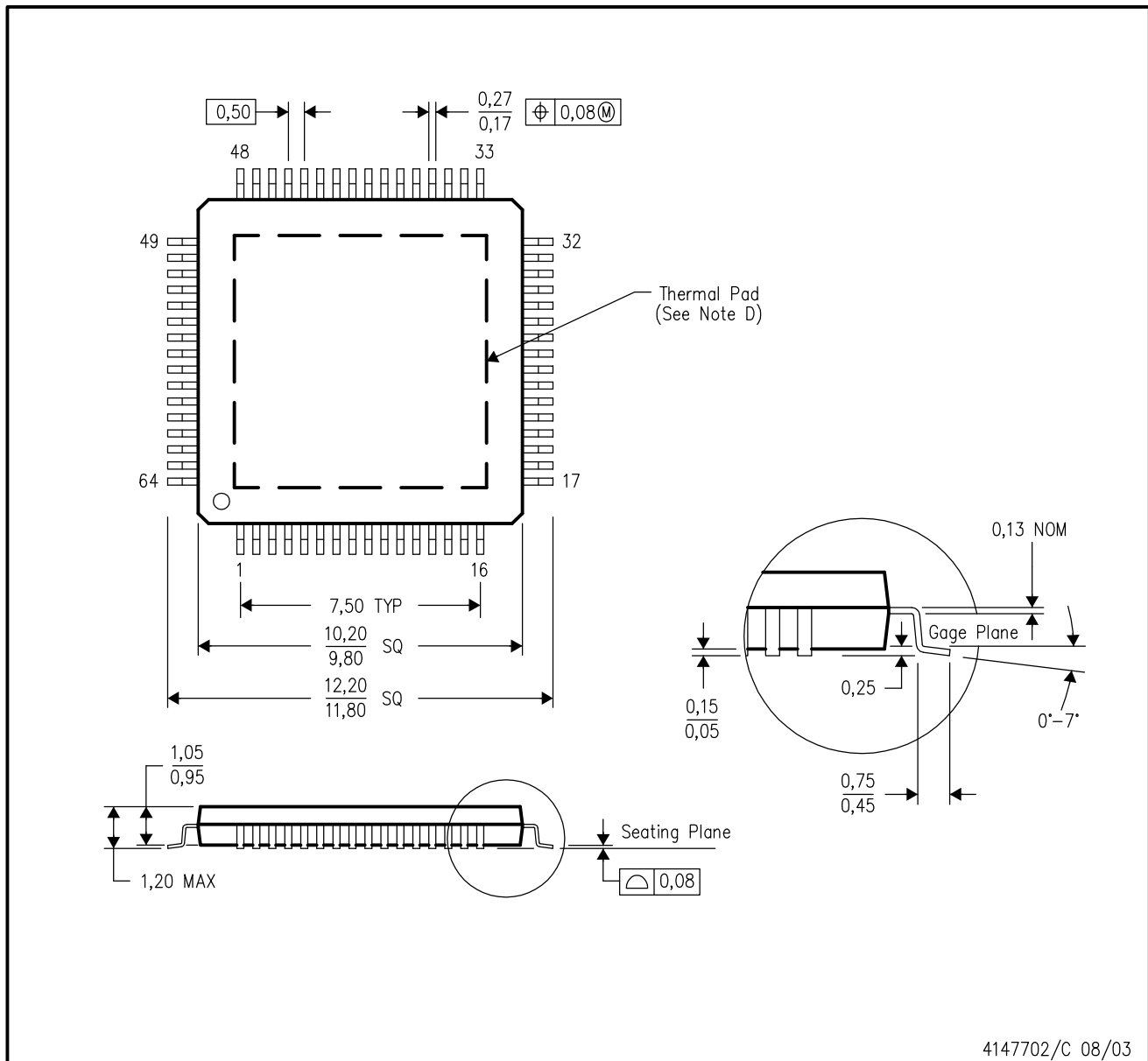


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LVCP408PAPR | HTQFP | PAP | 64 | 1000 | 346.0 | 346.0 | 41.0 |
| SN65LVCP408PAPT | HTQFP | PAP | 64 | 250 | 346.0 | 346.0 | 41.0 |

PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

PAP (S-PQFP-G64)

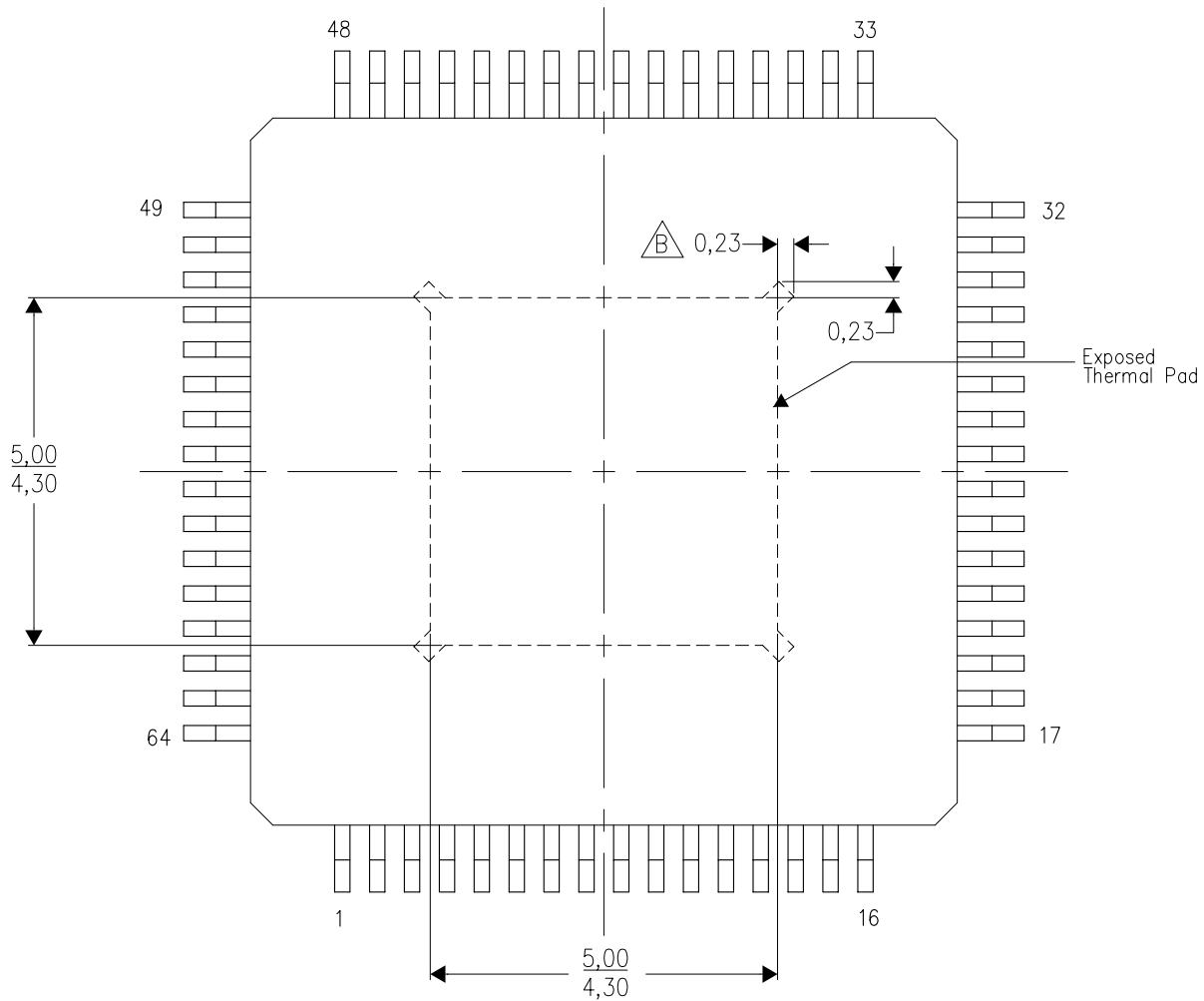
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.


The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View
Exposed Thermal Pad Dimensions

4206326-3/M 09/10

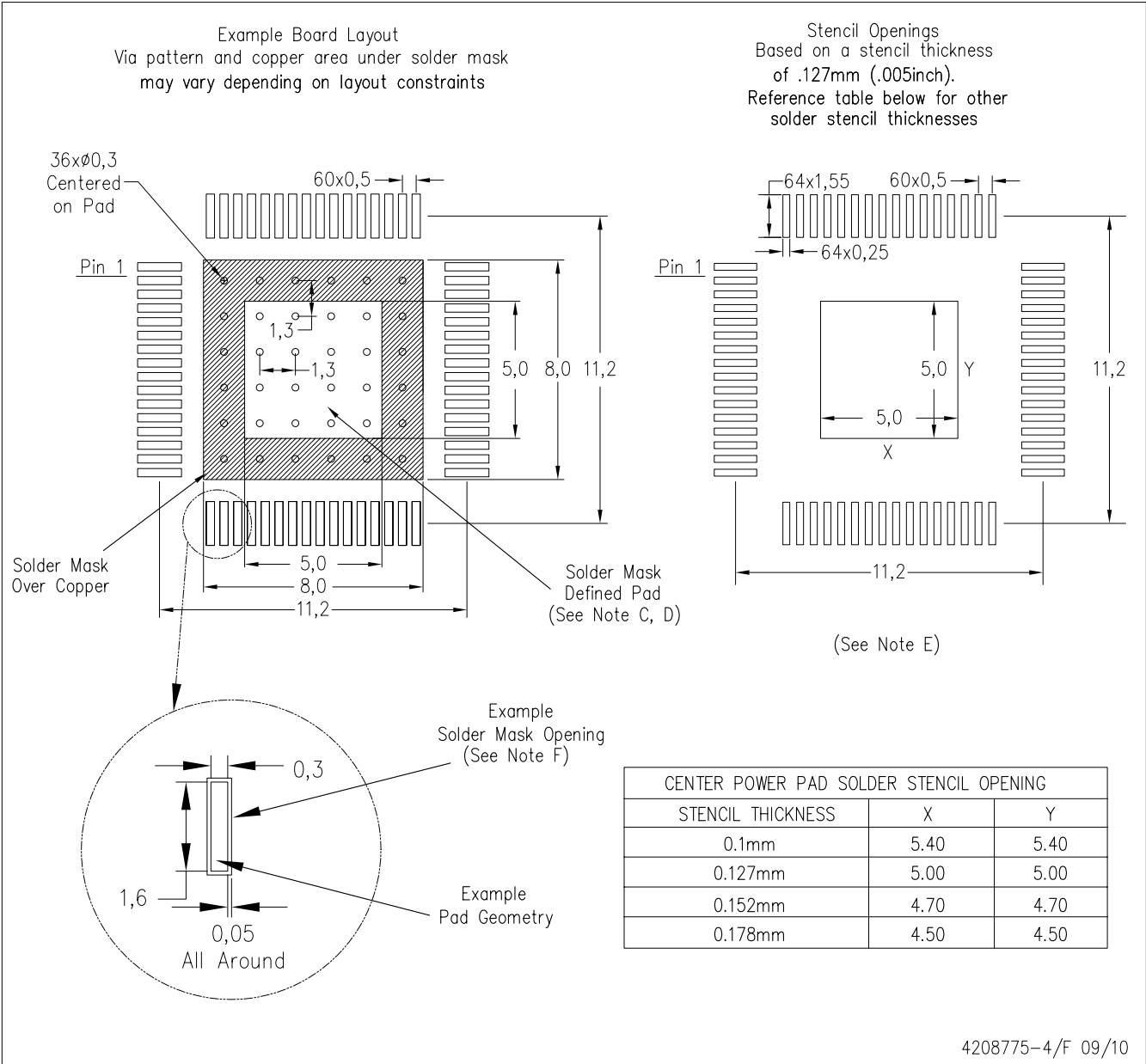
NOTES: A. All linear dimensions are in millimeters

 Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
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