



N-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

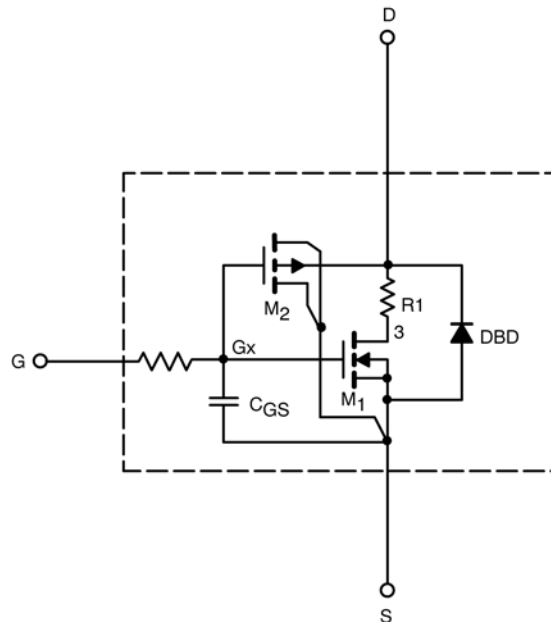
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



SPICE Device Model SiE808DF



查询"SiE808DF"供应商
Vishay Siliconix

SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.3		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	2562		A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 25 A	0.0013	0.0013	Ω
		V _{GS} = 4.5 V, I _D = 25 A	0.0022	0.0021	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 25 A	234	95	S
Forward Voltage ^a	V _{SD}	I _S = 10 A	0.84	0.80	V
Dynamic^b					
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	6664	8800	pF
Output Capacitance	C _{oss}		1585	1600	
Reverse Transfer Capacitance	C _{rss}		472	600	
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 20 A	121	102	nC
Gate-Source Charge	Q _{gs}	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 20 A	58	46	
Gate-Drain Charge	Q _{gd}		26	26	
			28	28	

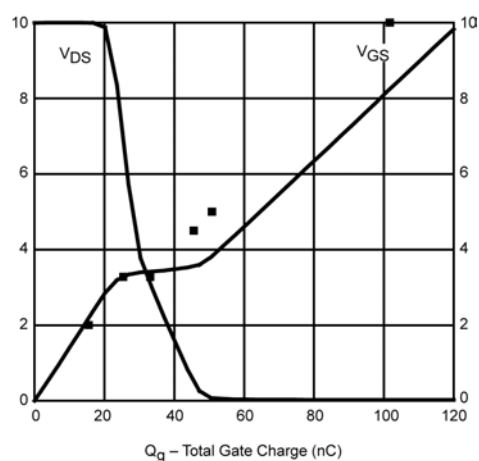
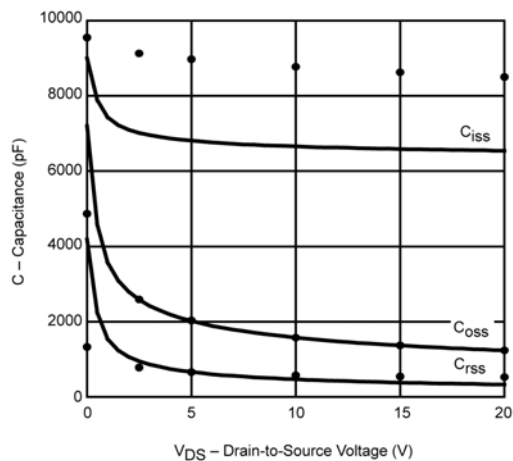
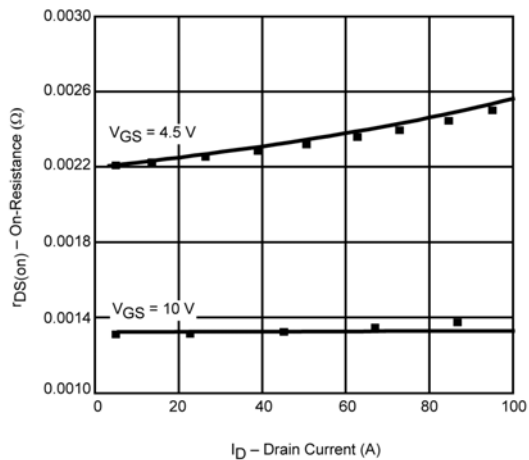
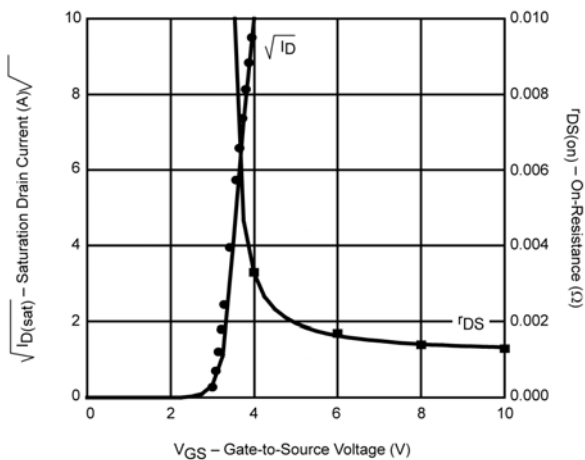
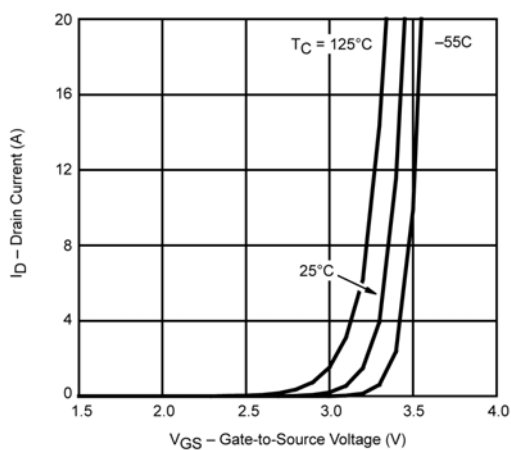
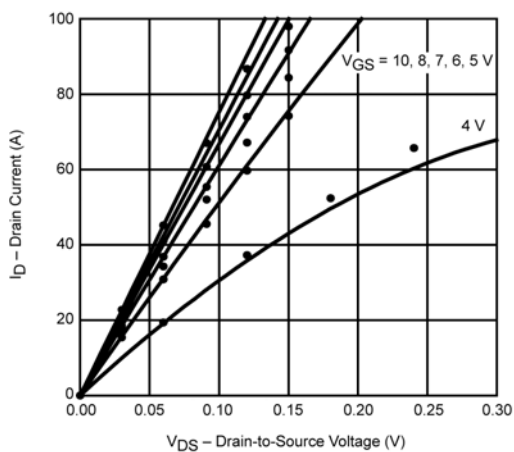
Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.