16 Megabit FlashBank Memory

LE28BW168T

FEATURES:

- **Single 3.0-Volt Read and Write Operations**
- **Separate Memory Banks by Address Space**
  - Simultaneous Read and Write Capability
- **Superior Reliability**
  - Endurance: 10,000 Cycles
  - Data Retention: 10 years
- **Low Power Consumption**
  - Active Current, Read: 10 mA (typical)
  - Active Current, Read & Write: 30 mA (typical)
  - Standby Current: 5µA (typical)
  - Auto Low Power Mode Current: 5µA (typical)
- **Fast Write Operation**
  - Bank Erase + Program: 8 sec (typical)
  - Block Erase + Program: 500 ms (typical)
  - Sector Erase + Program: 30 ms (typical)
- **Fixed Erase, Program, Write Times**
  - Does not change after cycling
- **Read Access Time**
  - 80/90 nsec
- **Latched Address and Data**
- **End of Write Detection**
  - Toggle Bit
  - Data # Polling
- **Flash Bank:** Two Small Erase Element Sizes
  - 1K Words per Sector or 32K Words per Block
  - Erase either element before Word Program
- **CMOS I/O Compatibility**
- **Packages Available**
  - 48-Pin TSOP
- **Continuous Hardware and Software Data Protection (SDP)**

Product Description

The LE28BW168T consists of two memory banks, 2 each 512K x 16 bits sector mode flash EEPROM manufactured with SANYO's proprietary, high performance FlashTechnology. The LE28BW168T writes with a 3.0-volt-only power supply.

The LE28BW168T is divided into two separate memory banks, 2 each 512K x 16 Flash banks. Each Flash bank is typically used for program code storage and contains 512 sectors, each of 1K words or 16 blocks, each of 32K words. The Flash banks may also be used to store data.

Any bank may be used for executing code while writing data to a different bank. Each memory bank is controlled by separate Bank selection address (A19) lines.

The LE28BW168T inherently uses less energy during Erase, and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the Flash technology uses less current to program and has a shorter Erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The Auto Low Power mode automatically reduces the active read current to approximately the same as standby; thus, providing an average read current of approximately 1 mA/MHz of Read cycle time.

The Flash technology provides fixed Erase and Program times, independent of the number of erase/program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated erase/program cycles.

Device Operation

The LE28BW168T operates as two independent 8 Megabit Word Pogram, Sector Erase flash EEPROMs.

All memory banks share common address lines, I/O lines, WE#, and OE#. Memory bank selection is by bank select address. WE# is used with SDP to control the Erase and Program operation in each memory bank.

The LE28BW168T provides the added functionality of being able to simultaneously read from one memory bank while erasing, or programming to one other memory bank. Once the internally controlled Erase or Program cycle in a memory bank has commenced, a different memory bank can be accessed for read. Also, once WE# and CE# are high during the SDP load sequence, a different bank may be accessed to read. LE28BW168T which selectes a bank by a address. It can be used as a normal conventinal flash memory when operats erase or program operation to only a bank at non-concurrent operation.

The device ID cannot be accessed while any bank is writing, erasing, or programming.

The Auto Low Power Mode automatically puts the LE28BW168T in a near standby mode after data has been accessed with a valid Read operation. This reduces the I_{DD} active read current from typically 10mA to typically 5µA.

The Auto Low Power mode reduces the typical I_{DD} active read current to the range of 1mA/MHz of Read cycle time. If a concurrent Read while Write is being performed, the I_{DD} is reduced to typically 40mA. The device exits the Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty.

Read

The Read operation of the LE28BW168T Flash banks is controlled by CE# and OE#, a chip enable and output enable both have to be low for the system to obtain data from the outputs. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the timing waveforms for further details (Figure 3).

When the read operation is executed without address change after power switch on, CE# should be changed the level high to low. If the read operation is executed after programing , CE# should be changed the level high to low.

Write

All Write operations are initiated by first issuing the Software Data Protect (SDP) entry sequence for Bank, Block, or Sector Erase. Word Program in the selected Flash bank. Word Program and all Erase commands have a fixed duration, that will not vary over the life of the device, i.e., are independent of the number of Erase/Program cycles endured.

Either Flash bank may be read to another Flash Bank during the internally controlled write cycle.

The device is always in the Software Data Protected mode for all Write operations Write operations are controlled by toggling WE# or CE#. The falling edge of WE# or CE#, whichever occurs last, latches the address. The rising edge of WE# or CE#, whichever occurs first, latches the data and initiates the Erase or Program cycle.

For the purposes of simplification, the following descriptions will assume WE# is toggled to initiate an Erase or Program. Toggling the applicable CE# will accomplish the same function. (Note, there are separate timing diagrams to illustrate both WE# and CE# controlled Program or Write commands.)

Word Program

The Word Program operation consists of issuing the SDP Word Program command, initiated by forcing CE# and WE# low, and OE# high. The words to be programmed must be in the erased state, prior to programming. The Word Program command programs the desired addresses word by word. During the Word Program cycle, the addresses are latched by the falling edge of WE#. The data is latched by the rising edge of WE#. (See Figure 4-1 for WE# or 4-2 for CE# controlled Word Program cycle timing waveforms, Table 3 for the command sequence, and Figure 15 for a flowchart.)

During the Erase or Program operation, the only valid reads from that bank are Data# Polling and Toggle Bit. The other bank may be read.

The specified Bank, Block, or Sector Erase time is the only time required to erase. There are no preprogramming or other commands or cycles required either internally or externally to erase the bank, block, or sector.

Erase Operations

The Bank Erase is initiated by a specific six-word load sequence (See Tables 3). A Bank Erase will typically be less than 70 ms.

An alternative to the Bank Erase in the Flash bank is the Block or Sector Erase. The Block Erase will erase an entire Block (32K words) in typically 15 ms. The Sector Erase will erase an entire sector (1024 words) in typically 15 ms. The Sector Erase provides a means to alter a single sector using the Sector Erase and Word Program modes. The Sector Erase is initiated by a specific six-word load sequence (see Table 3).

During any Sector, Block, or Bank Erase within a bank, any other bank may be read.

Bank Erase

The LE28BW168T provides a Bank Erase mode, which allows the user to clear the Flash bank to the "1"state. This is useful when the entire Flash must be quickly erased.

The software Flash Bank Erase mode is initiated by issuing the specific six-word loading sequence, as in the Software Data Protection operation. After the loading cycle, the device enters into an internally timed cycle.(See Table 3 for specific codes, Figure 5-1 for the timing waveform, and Figure12 for a flowchart.)

Block Erase

The LE28BW168T provides a Block Erase mode, which allows the user to clear any block in the Flash bank to the "1"state. The software Block Erase mode is initiated by issuing the specific six-word loading sequence, as in the Software Data Protect operation. After the loading cycle, the device enters into an internally timed Erase cycle. (See Table 3 for specific codes, Figure 5-2 for the timing waveform, and Figure 13 for a flowchart.) During the Erase operation, the only valid reads are Data# Polling and Toggle Bit from the selected bank, other banks may perform normal read.

Sector Erase

The LE28BW168T provides a Sector Erase mode, which allows the user to clear any sector in the Flash bank to the

"1"state. The software Sector Erase mode is initiated by issuing the specific six-word loading sequence, as in the Software Data Protect operation. After the loading cycle, the device enters into an internally timed Erase cycle.(See Table 3 for specific codes, Figure 5-3 for the timing waveform, and Figure 14 for a flowchart.) During the Erase operation, the only valid reads are Data# Polling and Toggle Bit from the selected bank, other banks may perform normal read.

Write Operation Status Detection

The LE28BW168T provides two software means to detect the completion of a Flash bank Program cycle, in order to optimize the system Write cycle time. The software detection includes two status bits : Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of Write Detection mode is enabled after the rising edge of WE#, which initiates the internal Erase or Program cycle.

The actual completion of the nonvolatile write is a synchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system will possibly get an erroneous result, i.e. valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious device rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

There is no provision to abort an Erase or Program operation, once initiated. For the SANYO Flash technology, the associated Erase and Program times are so fast, relative to system reset times, there is no value in aborting the operation. Note, reads can always occur from any bank not performing an Erase or Program operation.

Should the system reset, while a Block or Sector Erase or Word Program is in progress in the bank where the boot code is stored, the system must wait for the completion of the operation before reading that bank. Since the maximum time the system would have to wait is 25 ms (for a Block Erase), the system ability to read the boot code would not be affected.

Data# Polling (DQ_7)

When the LE28BW168T is in the internal Flash bank Program cycle, any attempt to read DQ_7 of the last word loaded during the Flash bank Word Load cycle will receive the complement of the true data. Once the Write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. (See Figure 6 for the Flash bank Data Polling timing waveforms and Figure 16 for a flowchart.)

Toggle Bit (DQ_6)

During the Flash bank internal Write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e. toggling between 0 and 1. When the Write cycle is completed, the toggling will stop. The device is then ready for the next operation. (See Figure 7 for Flash bank Toggle Bit timing waveforms and Figure 16 for a flowchart.)

Data Protection

The LE28BW168T provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5 volts.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The LE28BW168T provides the JEDEC approved software data protection scheme as a requirement for initiating a Write, Erase, or Program operation. With this scheme, any Write operation requires the inclusion of a series of three word-load operations to precede the Word Program operation. The three-word load sequence is used to initiate the Program cycle, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. The six-word sequence is required to initiate any Bank, Block, or Sector Erase operation.

The requirements for JEDEC compliant SDP are in byte format. The LE28BW168T is organized by word; therefore, the contents of DQ_8 to DQ_{15} are "Don't Care"during any SDP (3-word or 6-word) command sequence.

During the SDP load command sequence, the SDP load cycle is suspended when WE# is high. This means a read may occur to any other bank during the SDP load sequence.

The bank reserve in SDP load sequence is reserved by the bus cycle of command materialization. If the command sequence is aborted, e.g., an incorrect address is loaded, or incorrect data is loaded, the device will return to the Read mode within T_{RC} of execution of the load error.

Concurrent Read and Write Operations

The LE28BW168T provides the unique benefit of being able to read any bank, while simultaneously erasing, or programming one other bank. This allows data alteration code to be executed from one bank, while altering the data in another bank. The next table lists all valid states.

Concurrent Read/Write State Table

Bank1	Bank2
Read	No Operation
Read	Write
Write	Read
No Operation	Write
Write	No Operation
No Operation	Read

Note: For the purposes of this table, write means to Block, Sector, or Bank Erase, or Word Program as applicable to the appropriate bank.

The device will ignore all SDP commands and toggling of WE# when an Erase or Program operation is in progress. Note, Product Identification entry commands use SDP; therefore, this command will also be ignored while an Erase or Program, operation is in progress.

Product Identification

The product identification mode identifies the device manufacturer as SANYO and provides a code to identify each bank. The manufacturer ID is the same for each bank; however, each bank has a separate device ID. Each bank is individually accessed using the applicable Bank Address and a software command. Users may wish to use the device ID operation to identify the write algorithm requirements for each bank.

(For details, see Table 3 for software operation and Figures 8 for timing waveforms.)

Product Identification Table

	Word	Data
Maker ID	0000H	0062H
Device Code(Bank1)	0001H	2595H
Device Code(Bank2)	0001H	2596H

Device ID codes are unique to each bank. Should a chip ID be required, any of the bank IDs may be used as the chip ID. While in the read software ID mode, no other operation is allowed until after exiting these modes.

Product Identification Mode Exit

In order to return to the standard Read mode, the Product Identification mode must be exited. Exit is accomplished by issuing the Software ID exit command, which returns the device to normal operation. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. For details, (see Table 3 for software operation and Figures 9 for timing waveforms.)

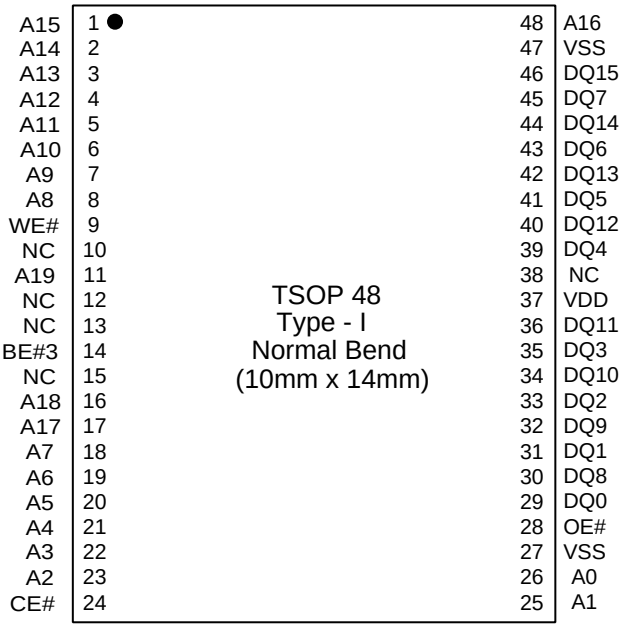


Figure 1 : Pin Description : TSOP-1 (10mm x 14mm)

Symbol	Pin Name	Function
A19	Bank Select address	To activate the Bank1 when low, to activate the Bank2 when high.
A18-A0	Flash Bank addresses	To provide Flash Bank address
A18-A15	Flash Bank Block addresses	To select a Flash Bank Block for erase
A18-A10	Flash Bank Sector addresses	To select a Flash Bank Sector for erase
DQ15-DQ0	Data Input/Output	To output data during read cycle and receive input data during write cycle. The outputs are in tristate when OE# is high or CE# is high.
CE#	Chip Enable	To activate the Flash Bank when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write, erase or program operations.
V_{DD}	Power Supply	To provide 3.0 volts supply.(3.0 volts ± 3.3volts)
GND	Ground	
NC	No Connection	Unconnected Pins

Note)BE3# should be connected to V_{DD} signal as usual.

Table1: Pin Description

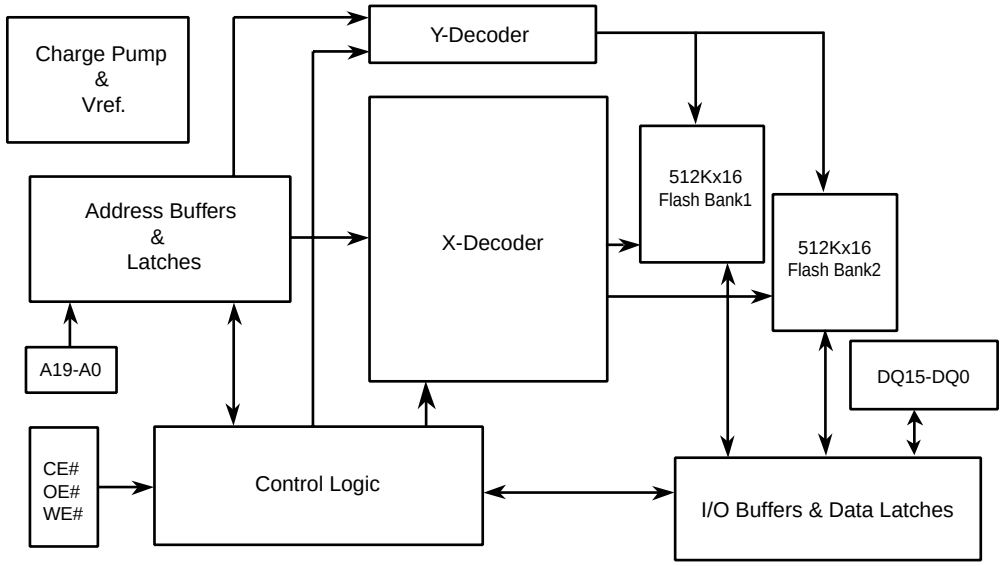


Figure2: Functinaly Block Diagram

Array Operating Mode	CE#	OE#	WE#	DQ	A19	A18-A0
Read						
Bank1	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_{IL}	A_{IN}
Bank2	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_{IH}	A_{IN}
Block Erase						
Bank1	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IL}	See Table:3
Bank2	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IH}	See Table:3
Sector Erase						
Bank1	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IL}	See Table:3
Bank2	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IH}	See Table:3
Program						
Bank1	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IL}	See Table:3
Bank2	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IH}	See Table:3
Standby	V_{IH}	X	X	High Z	X	X
Write Inhibit	V_{IH}	V_{IL}	V_{IL}	X	X	X
Bank Erase						
Bank1	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IL}	See Table:3
Bank2	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IH}	See Table:3
Status Operating Mode	**CE#**	**OE#**	**WE#**	**DQ**	**A19**	**A18-A0**
Product Identification						
Bank1	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_{IL}	A_{18}-A_1 = V_{IL}
Bank2	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_{IH}	A_0 = V_{IL} or V_{IH}

Note: Entering illegal state during an Erase, Program, or Write operation will not affect the operation, i.e., the erase, program, or write will continue to normal completion.

Table:2 Operating Modes Selection

Table:3 Software Command Codes

Command Code	1stBus Cycle		2ndBus Cycle		3rdBus Cycle		4thBus Cycle		5thBus Cycle		6thBus Cycle	
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
	Note1,4	Note5	Note1,4	Note5	Note1,4	Note5	Note1,4	Note5	Note1,4	Note5	Note1,4	Note5
Software ID Entry	5555	AA	2AAA	55	5555 +BAX	90	Note2					
Software ID Exit	5555	AA	2AAA	55	5555 +BAX	F0	Note3					
Word Program	5555	AA	2AAA	55	5555	A0	Word Address	Data In				
Sector Erase	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SAX +BAX	30
Block Erase	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	LAX +BAX	50
Bank Erase	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555 +BAX	10

Notes for Software Product ID Command Code:

1. Command Code Address format : A14 - A0 are in HEX code.
2. With A14 - A0 = 0;
   Sanyo Manufacturer Code = 0062H is read with A0 = 0.
   Sanyo LE28BW168T Device code 2595H, 2596H is read with A0 = 1.
3. The device does not remain in software Product ID Mode if powered down.
4. Address form A14 to A18 are 'Don't Care' for Command sequences.
   A19 is bank selection address has been reserved in last bus cycle of Command sequence.
5. Data format DQ0 to DQ7 are in HEX and DQ8 to DQ15 are "Don't Care".
6. BAX = Bank address: A19, LAX = Block address:A18 to A15, SAX = Sector address: A18 to A10.

[Absolute Maximum Stress Ratings]

Applied conditions greater than those listed under "absolute maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Storage Temperature	: -65ºC to +150ºC
D. C. Voltage on Any Pin to Ground Potential	: -0.5V to V_{DD} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential	: -1.0V to V_{DD} + 1.0V
Package Power Dissipation Capability (Ta = 25ºC)	: 1.0W

[Operating Range]

Ambient Temperature	: -40ºC to +80ºC
V_{DD}	: 3.0V ± 0.3V

[AC condition of Test]

Input Rise/Fall Time	: 5 ns
Output Load	: C_L = 30 pF
(See Figures 10 and 11)	

[DC Operating Characteristics]

Symbol	Parameter	Min	Max	Unit	Test Condition
I_{DD}	Power Supply current Read		20	mA	CE# = V_{IL}, WE# = V_{IH}, I/O's open, Address Input = V_{IL}/V_{IH}, at f =10MHz, V_{DD} = V_{DD}(Max)
	Write		40	mA	CE# = WE# = V_{IL}, OE# = V_{IH}, V_{DD} = V_{DD}(Max)
	Read + Erase / Program		60	mA	CE# = V_{IL}, OE# = WE# = V_{IH} , Address Input = V_{IL}/V_{IH}, at f =10MHz, WE# = V_{IH}, V_{DD} = V_{DD}(Max)
I_{SB}	Standby current (CMOS input)		40	µA	CE# = V_{IHC} , V_{DD} = V_{DD}(Max)
I_{LI} I_{OL}	Input Leak current Output Leak current		10 10	µA µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD}(Max) V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD}(Max)
V_{IL} V_{ILC} V_{IH} V_{IHC}	Input Low Voltage Input Low Voltag (CMOS) Input High Voltag Input High Voltge (CMOS)	 V_{DD}*0.8 V_{DD}-0.2	V_{DD}*0.2 0.2	V V V V	
V_{OL} V_{OH}	Output Low Voltag Output High Voltag	V_{DD}-0.2	0.2	V V	I_{OL} = 100µA, V_{DD} = V_{DD}(Min) I_{OH} = -100µA, V_{DD} = V_{DD}(Min)

[Recommend System Power-up Timings]

Symbol	Parameter	Max	Units
$T_{PU-READ}$(1) $T_{PU-WRITE}$(1)	Power-up to Read Operation Power-up to Write Operation	200 200	µs µs

Note(1): This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

[Capacitance (Ta = 25°C, f = 1MHz, other pins open)]

Symbol	Parameter	Test Condition	Max
C_{DQ}(1) C_{IN}(1)	I/O Pin Capacitance Input Capacitance	V_{DQ} = 0V V_{IN} = 0V	12PF 6PF

Note(1): This parameter is measured only for initial qualirication and after a design or process change that could affect this parameter.

[Reliability Characteristic]

Symbol	Parameter	Min Spec	Units
N_{END}(1) T_{DR}(1)	Endurance Data Retention	10,000 10	Cycle/Sector Years

Note(1): This parameter is measured only for initial qualirication and after a design or process change that could affect this parameter.

[AC Characteristic]

Read Cycle Timing Parameters

Symbol	Parameter	8 0		9 0		Units
		Min	Max	Min	Max	
T_{RC}	Raed Cycle Time	80		90		ns
T_{CE}	CE# Access Time		80		90	ns
T_{AA}	Address Access Time		80		90	ns
T_{OE}	OE# Access Time		40		50	ns
T_{CLZ}(1)	BE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	BE# High to High-Z Output		30		30	ns
T_{OHZ}(1)	OE# High to High-Z Output		30		30	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

Write, Erase, Program Cycle, Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{BP}	Word Program Time		20	µs
T_{SE}	Sector Erase Time		25	ms
T_{LE}	Block Erase Time		25	ms
T_{BE}	Bank Erase Time		100	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CES}	CE# Setup Time	0		ns
T_{CEH}	CE# Hold Time	0		ns
T_{WES}	WE# Setup Time	0		ns
T_{WEH}	WE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{WP}	WE# Puls Low Width	50		ns
T_{WPH}	WE# Puls High Time	30		ns
T_{DS}	Data Setup Time	50		ns
T_{DH}	Data Hold Time	0		ns
T_{VDDR}(1)	V_{DD} Rise Time	0.1	50	ms
T_{IDA}	ID READ / Exit Cycle Time	150		ns

Note:(1) This parameter is measured only for initial qualification and after a desgin or process change that could affect this parameter.

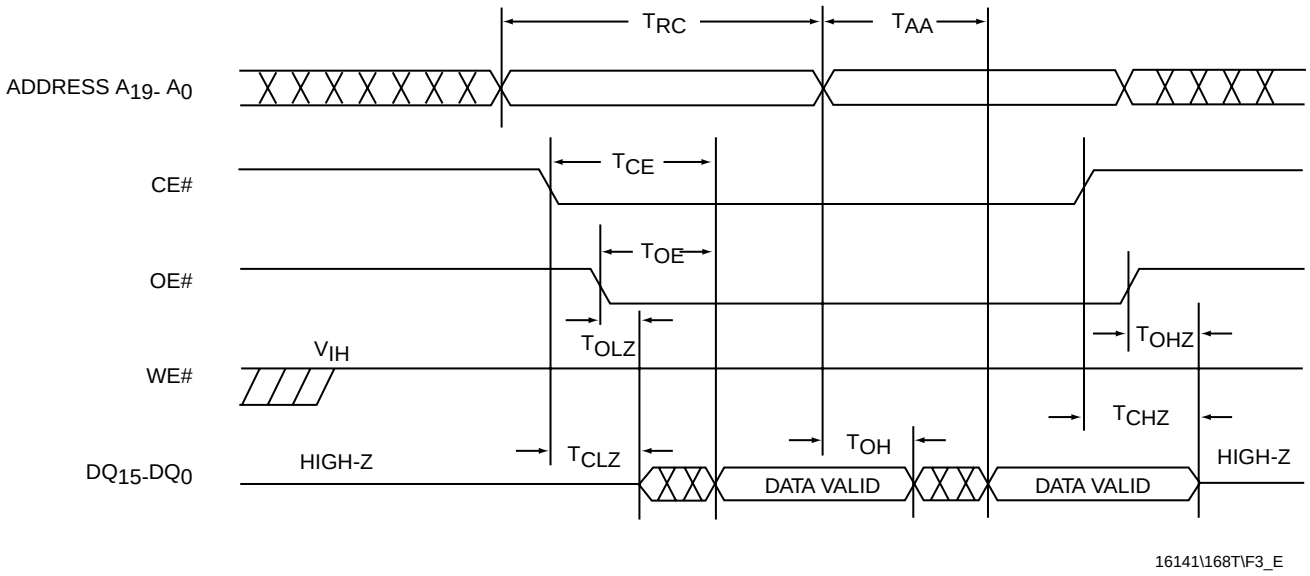


Figure 3: Read Cycle Timing Diagram

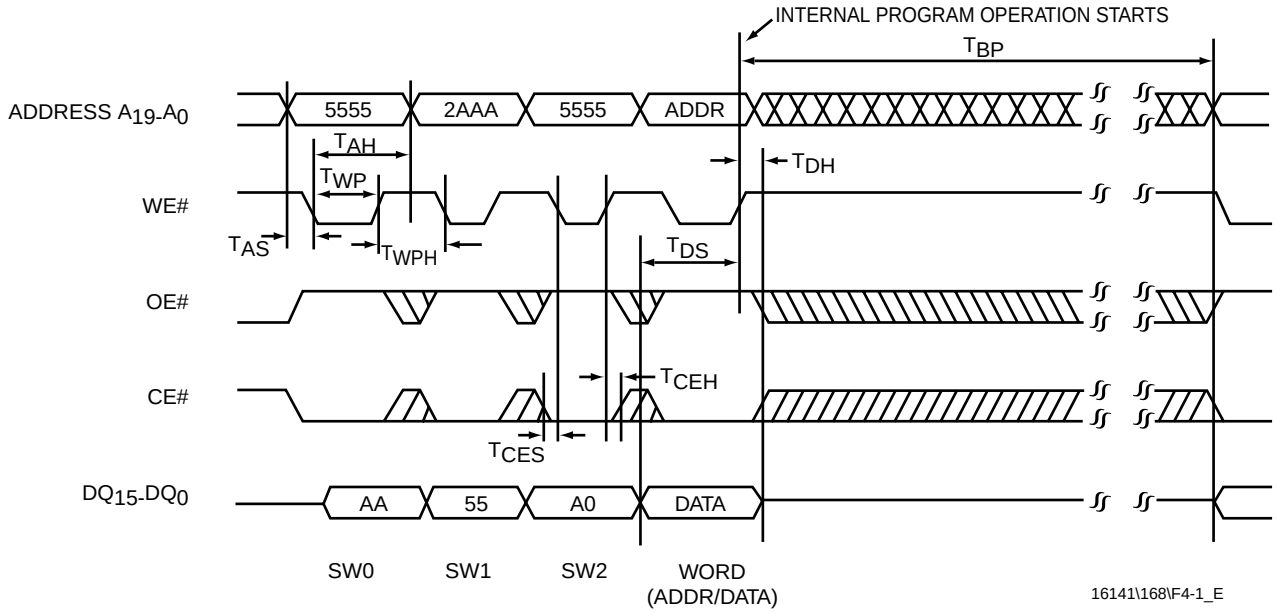


Figure 4-1: WE# Controlled Word Program Cycle Timing Diagram

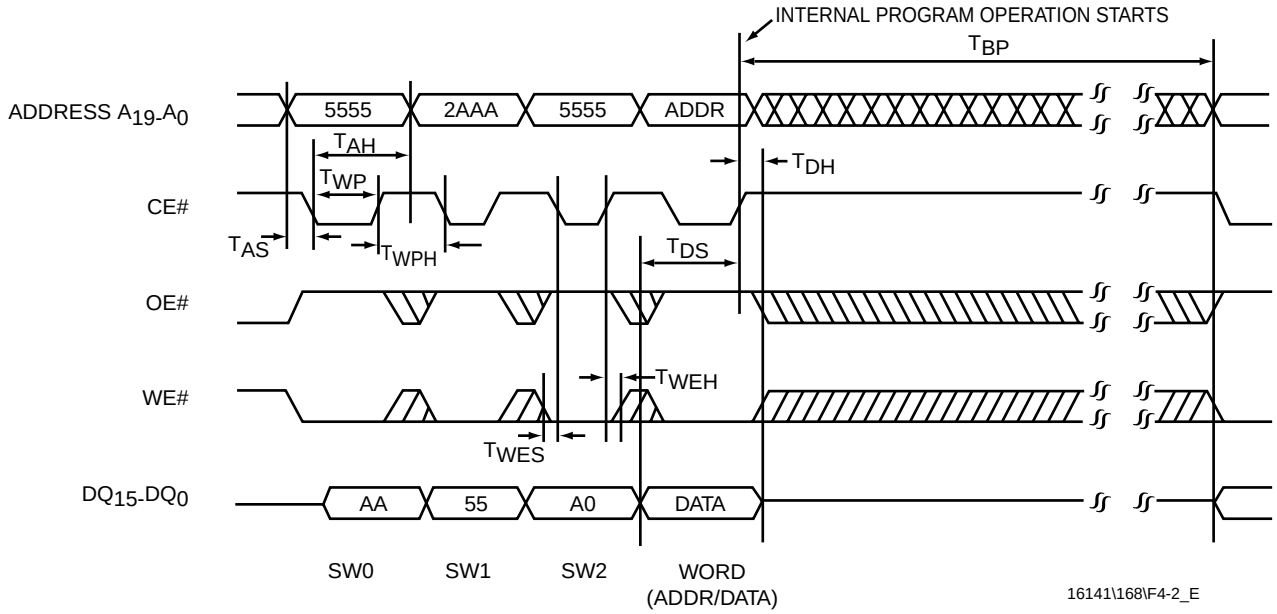


Figure 4-2: CE# Controlled Word Program Cycle Timing Diagram

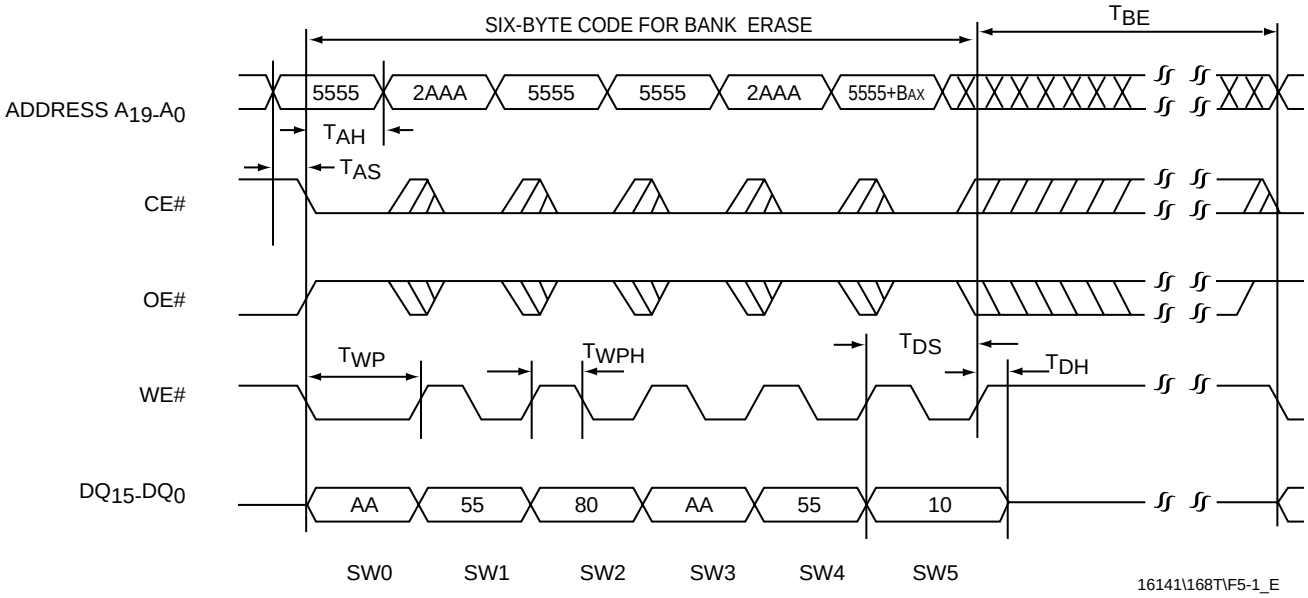


Figure 5-1: Bank Erase Cycle Timing Diagram

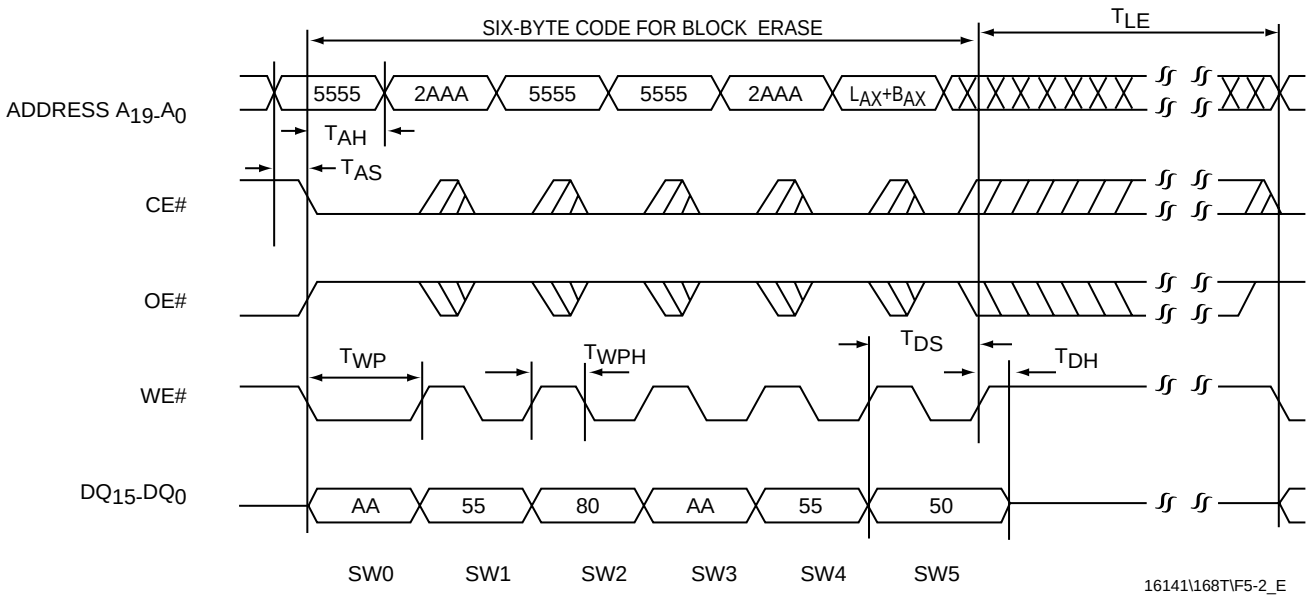


Figure 5-2: Block Erase C ycle Timing Diagram

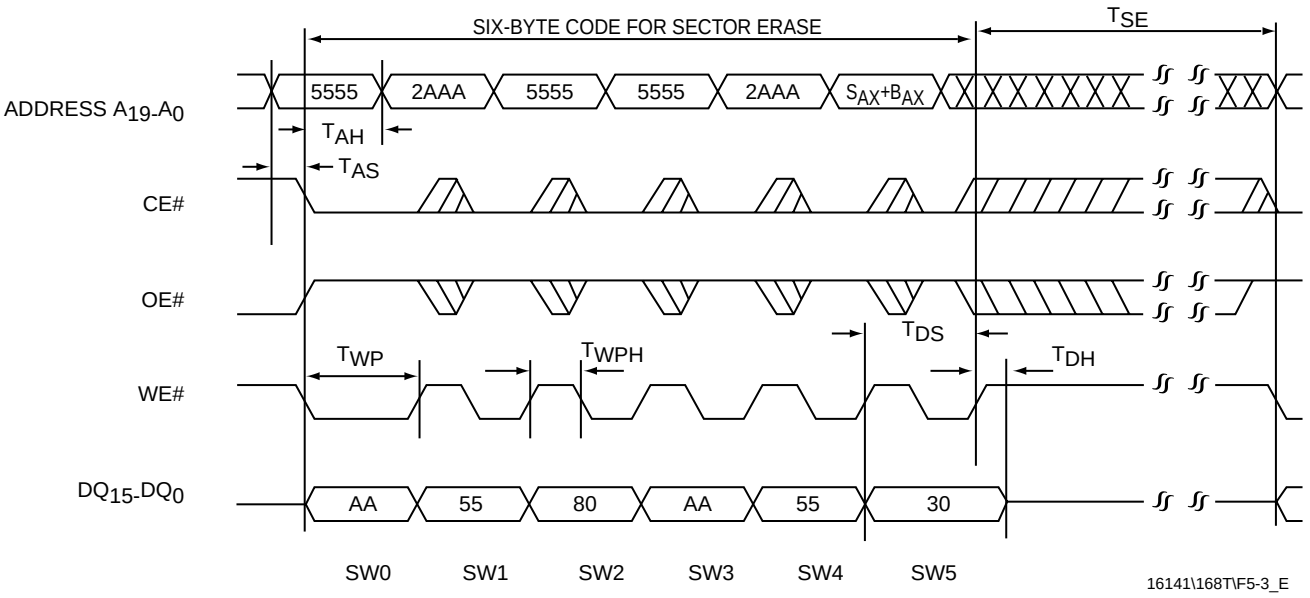


Figure 5-3: Sector Erase Cycle Timing Diagram

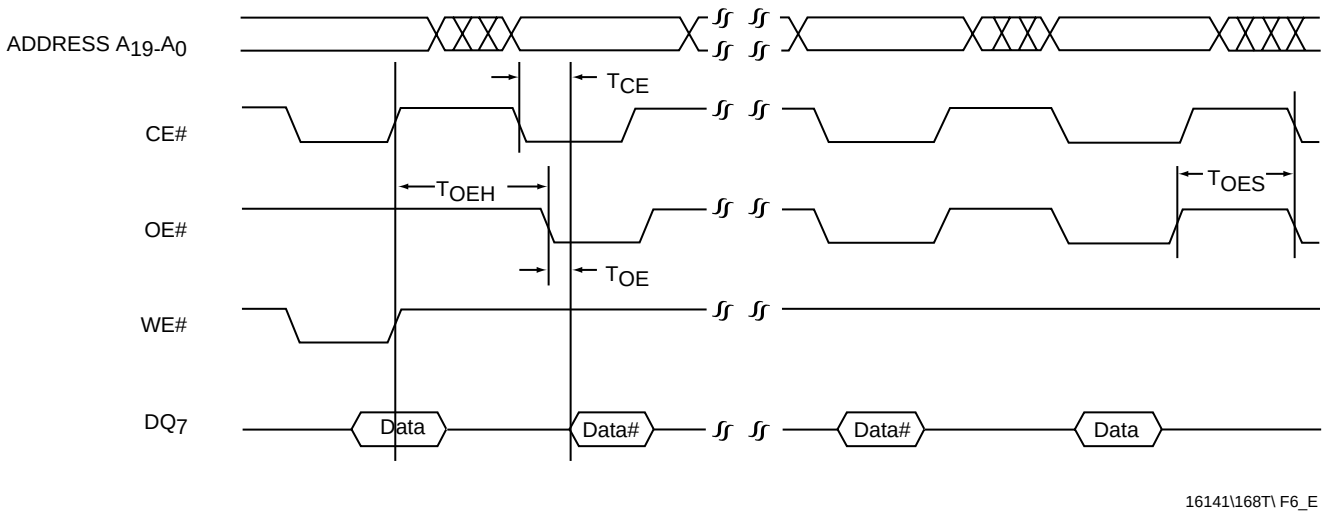


Figure 6: Data Polling Timing Diagram

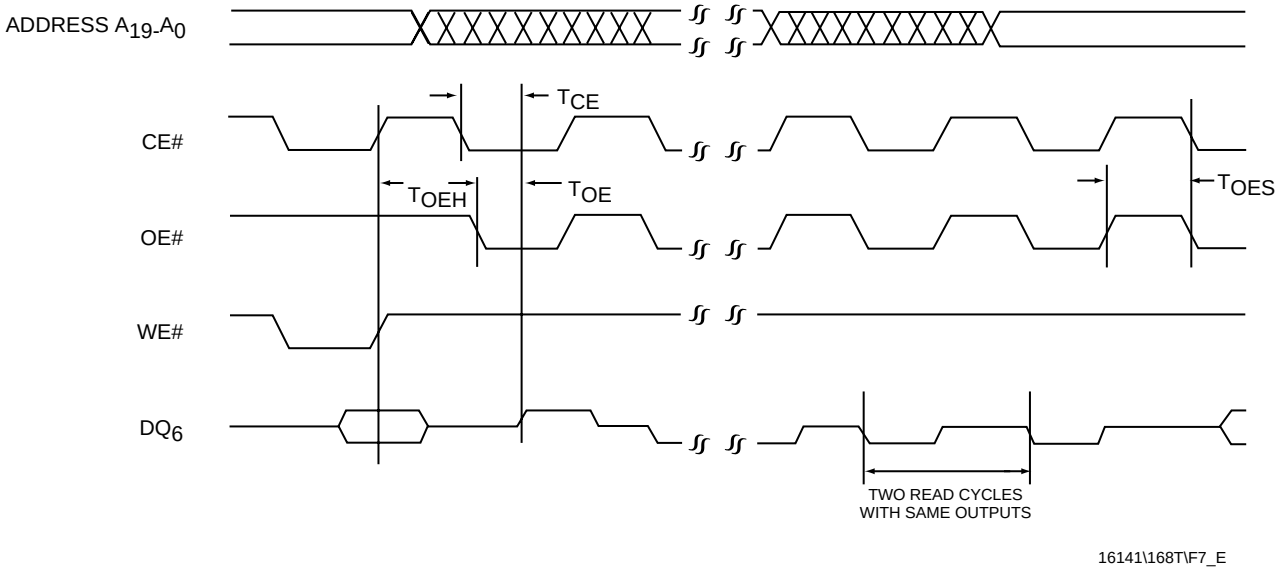


Figure 7: Toggle Bit Timing Diagram

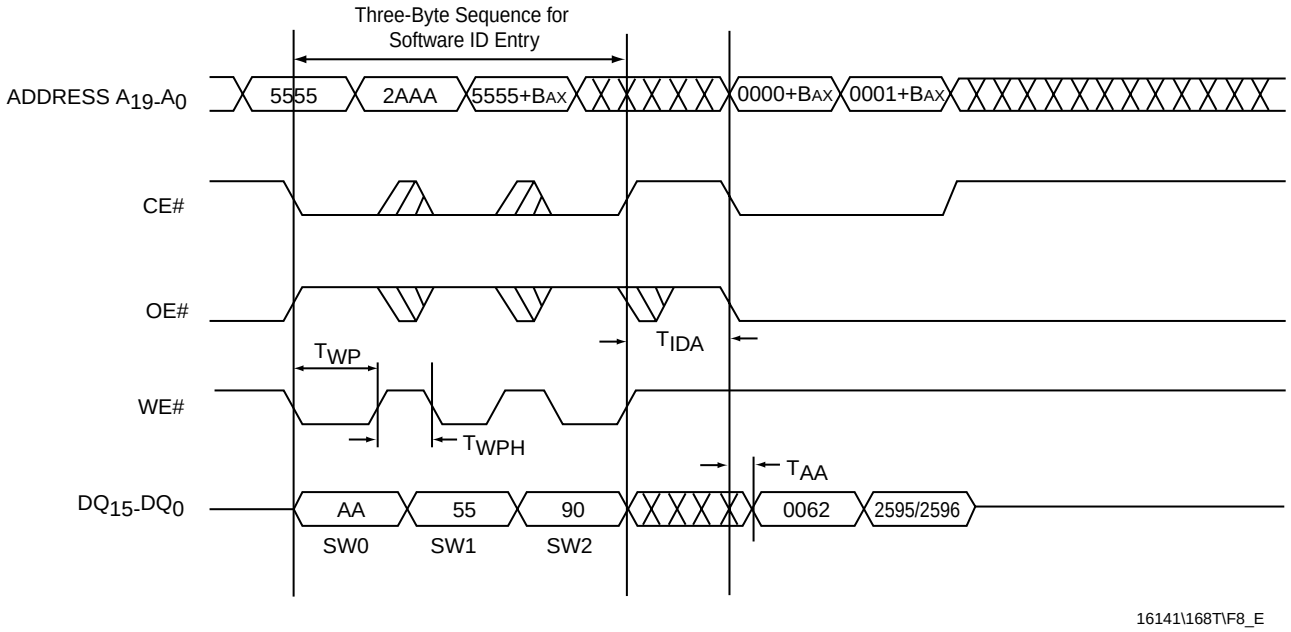


Figure 8: Software ID Entry and Read

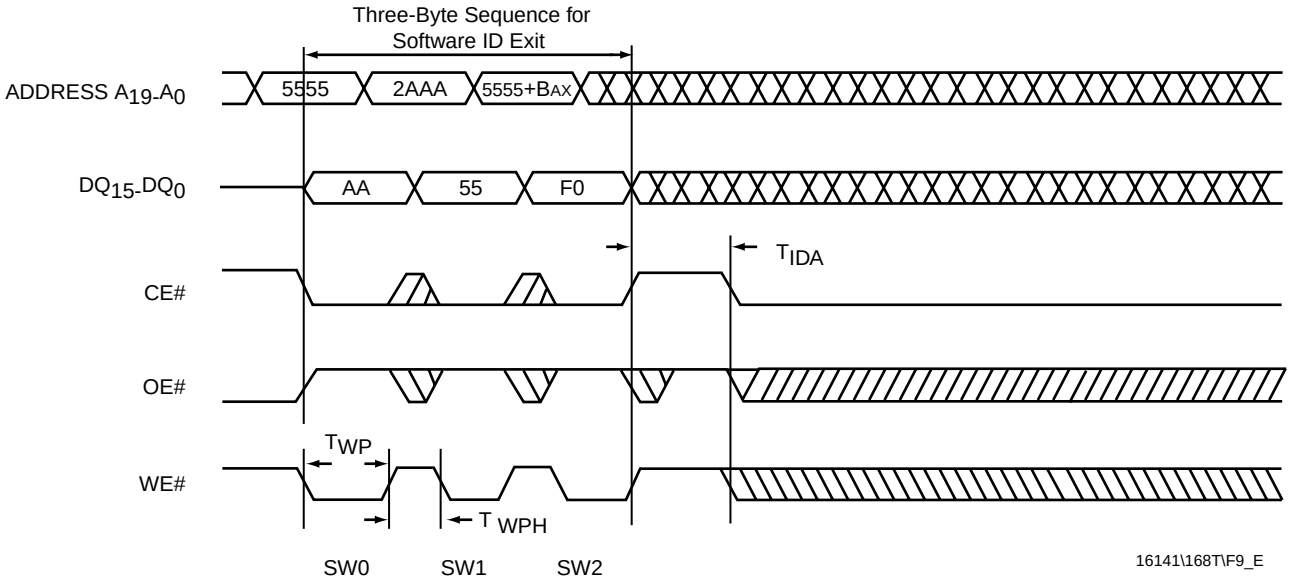
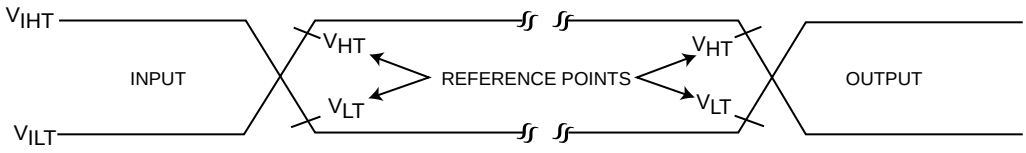


Figure 9: Software ID Exit



AC test inputs are driven at V_{IHT} (V_{DD}*0.9) for a logic "1"and V_{ILT} (V_{DD}*0.1) for a logic "0"
Measurement reference points for inputs and outputs are at V_{HT} (V_{DD}*0.7) and V_{LT} (V_{DD}*0.3)
Input rise and fall times (10% « 90%) are <10 ns.

Figure 10: AC I/O ReferenceWaveforms

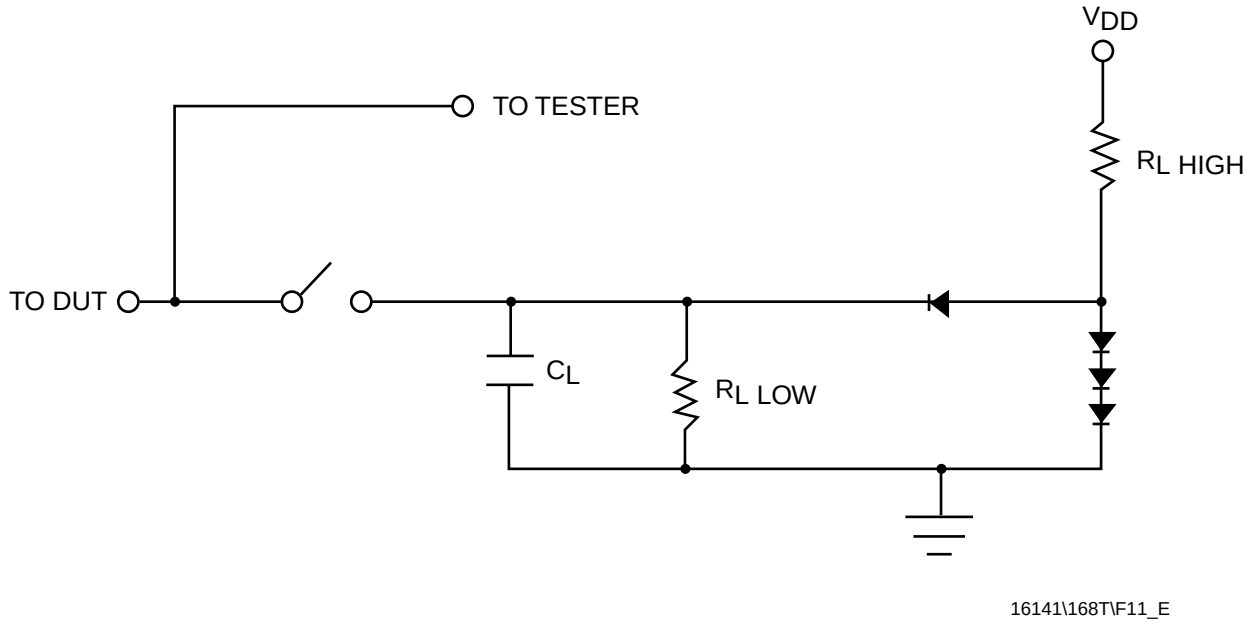


Figure 11: A Test Load Example

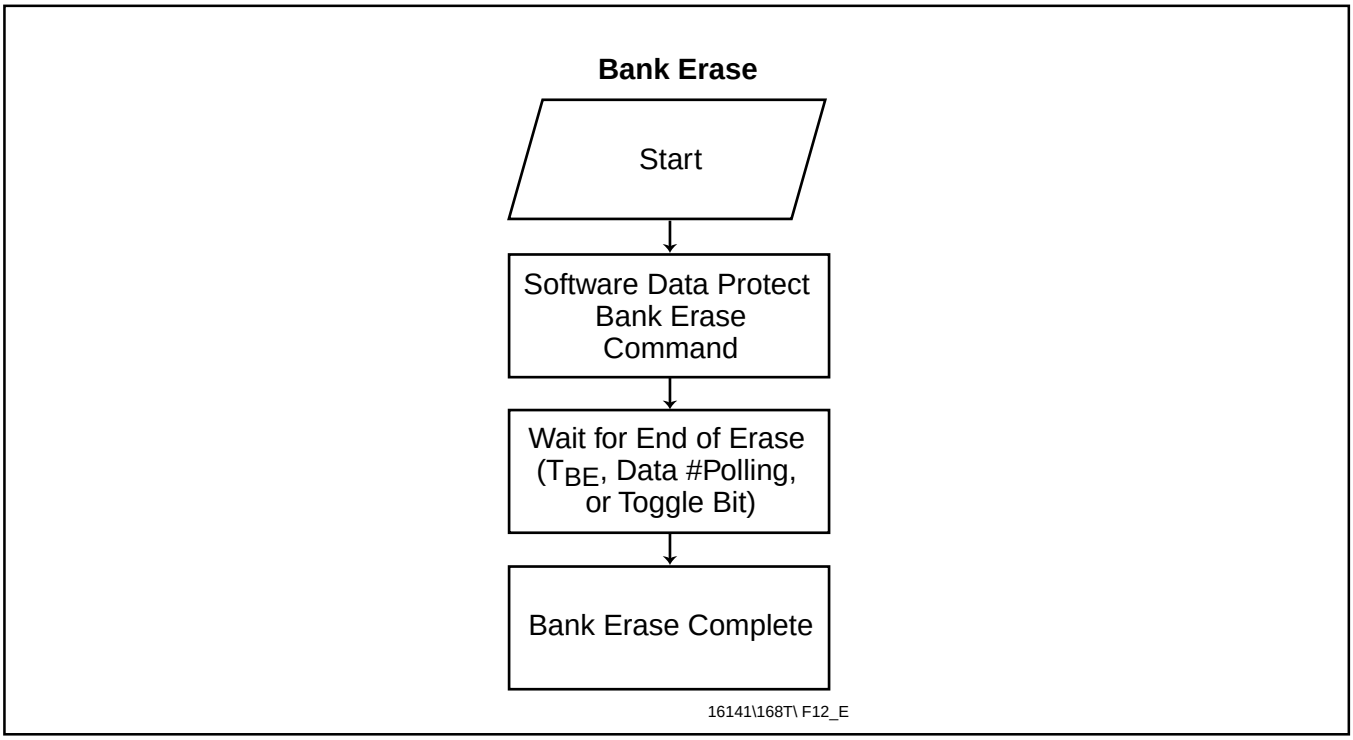


Figure 12: Bank Erase Flowchart

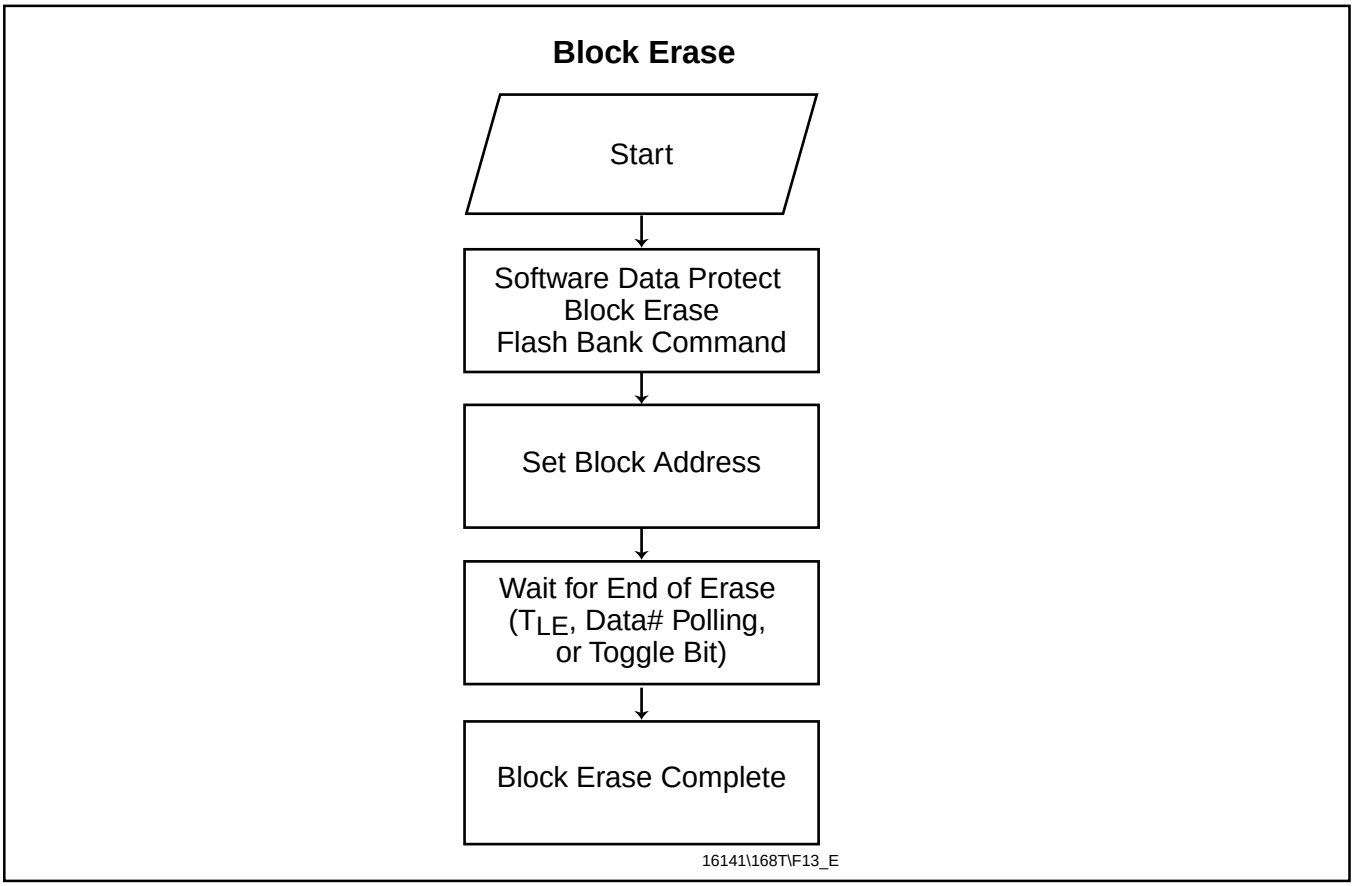


Figure 13: Block Erase Flowchart

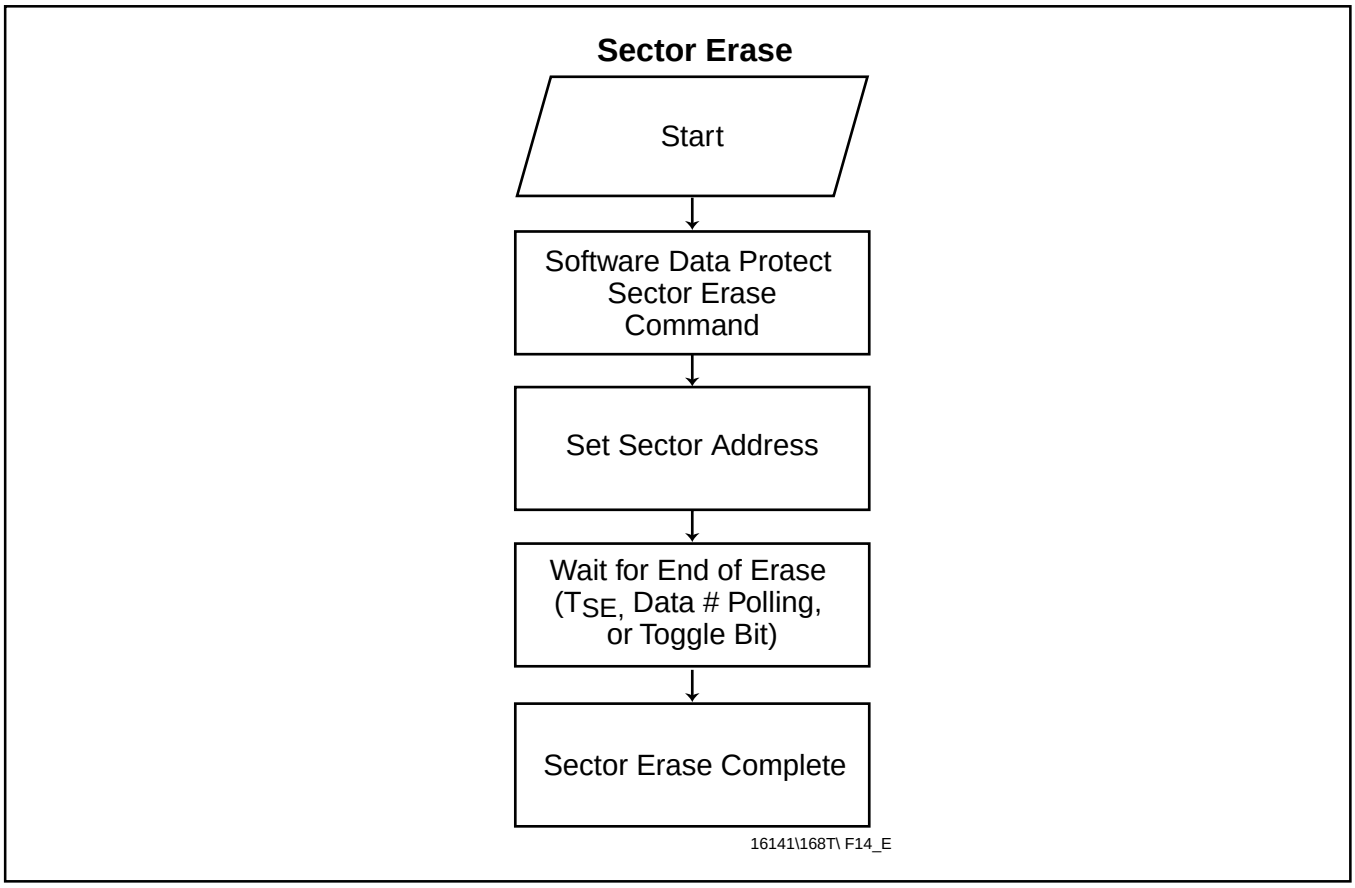


Figure 14: Sector Erase Flowchart

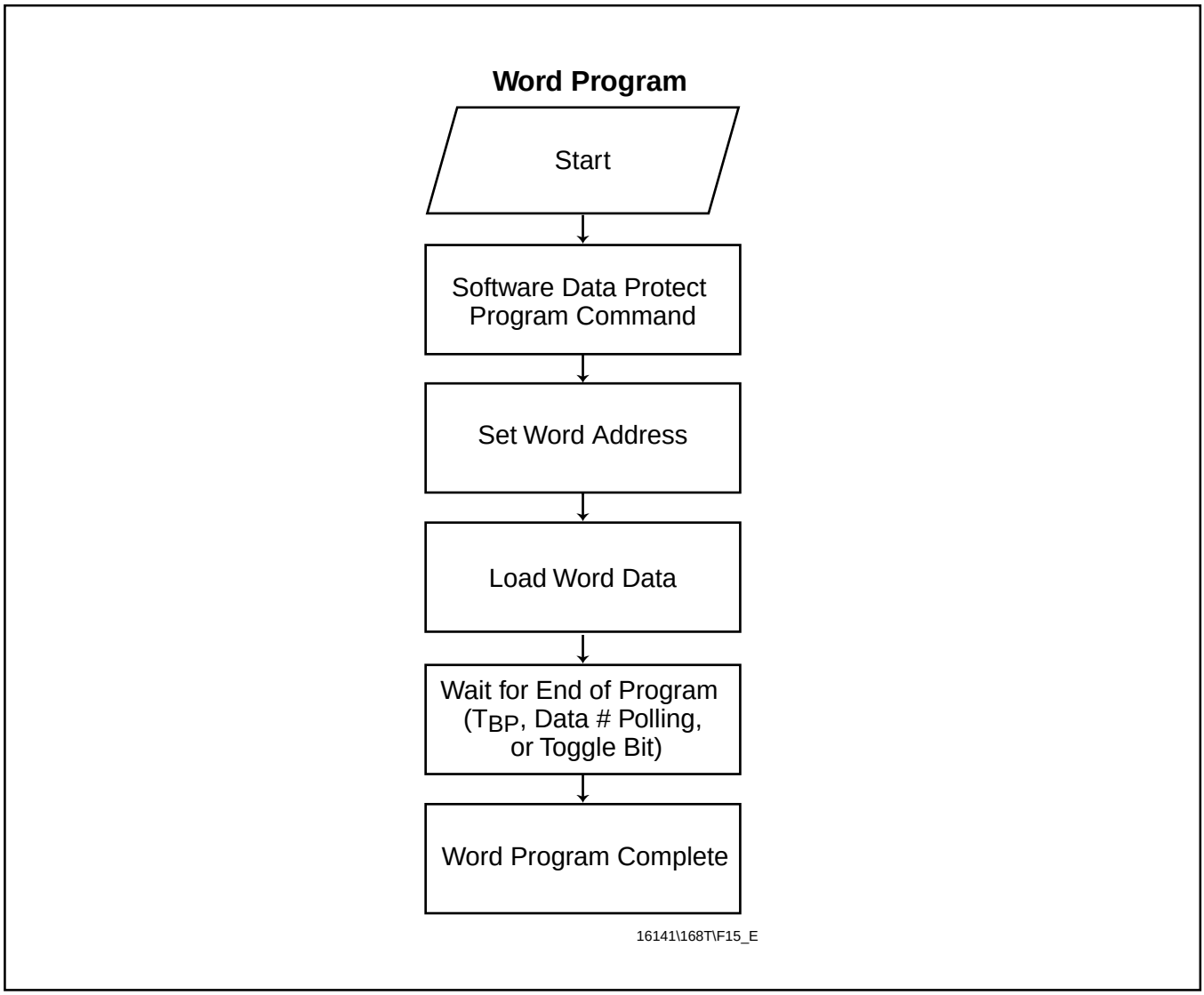


Figure 15: Word Program Flowchart

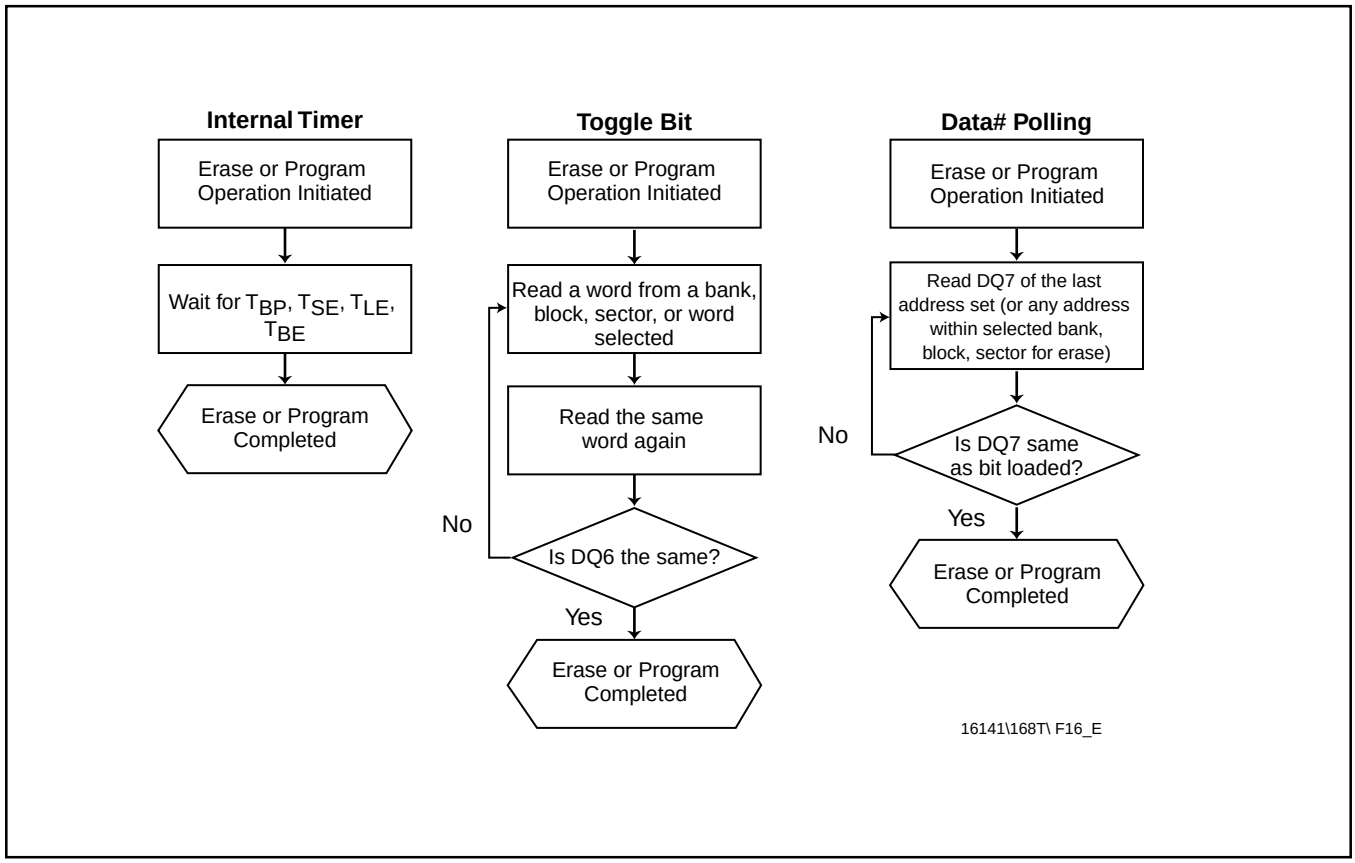


Figure 16: End of Erase or Program Wait Options Flowchart