



L6743B

High current MOSFET driver

Features

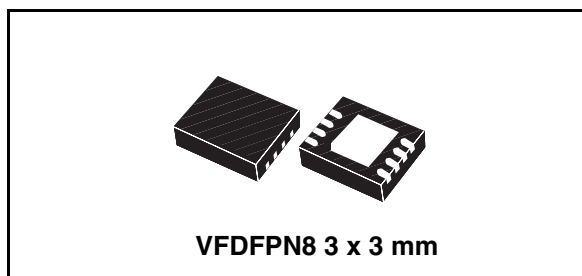
- Dual MOSFET driver for synchronous rectified converters
- High driving current for fast external MOSFET switching
- Integrated bootstrap diode
- High frequency operation
- Enable pin
- Adaptive dead-time management
- Flexible gate-drive: 5 V to 12 V compatible
- High-impedance (HiZ) management for output stage shutdown
- Preliminary OV protection
- VFDFPN8 3 x 3 mm package

Applications

- High current VRM / VRD for desktop / server / workstation CPUs
- High current and high efficiency DC / DC converters

Description

L6743B is a flexible, high-frequency dual-driver specifically designed to drive N-channel MOSFETs connected in synchronous-rectified buck topology.



Combined with ST PWM controllers, the driver allows implementing complete voltage regulator solutions for modern high-current CPUs and DC-DC conversion in general. L6743B embeds high-current drivers for both high-side and low-side MOSFETs. The device accepts flexible power supply (5 V to 12 V) to optimize the gate-drive voltage for high-side and low-side maximizing the system efficiency.

The bootstrap diode is embedded saving the use of external diodes. Anti shoot-through management avoids high-side and low-side MOSFET to conduct simultaneously and, combined with adaptive dead-time control, minimizes the LS body diode conduction time.

L6743B embeds preliminary OV protection: after Vcc overcomes the UVLO and while the device is in HiZ, the LS MOSFET is turned ON to protect the load in case the output voltage overcomes a warning threshold protecting the output against HS failures.

The driver is available is VFDFPN8 3 x 3 mm packages.

Table 1. Device summary

Order code	Package	Packing
L6743B	VFDFPN8	Tube
L6743BTR		Tape and reel

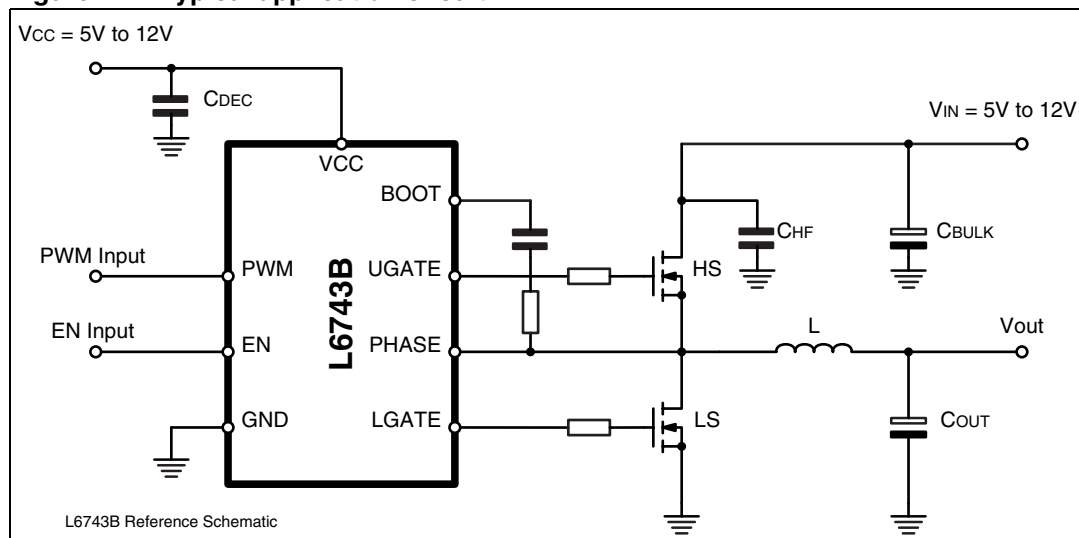
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1 Typical application circuit and block diagram

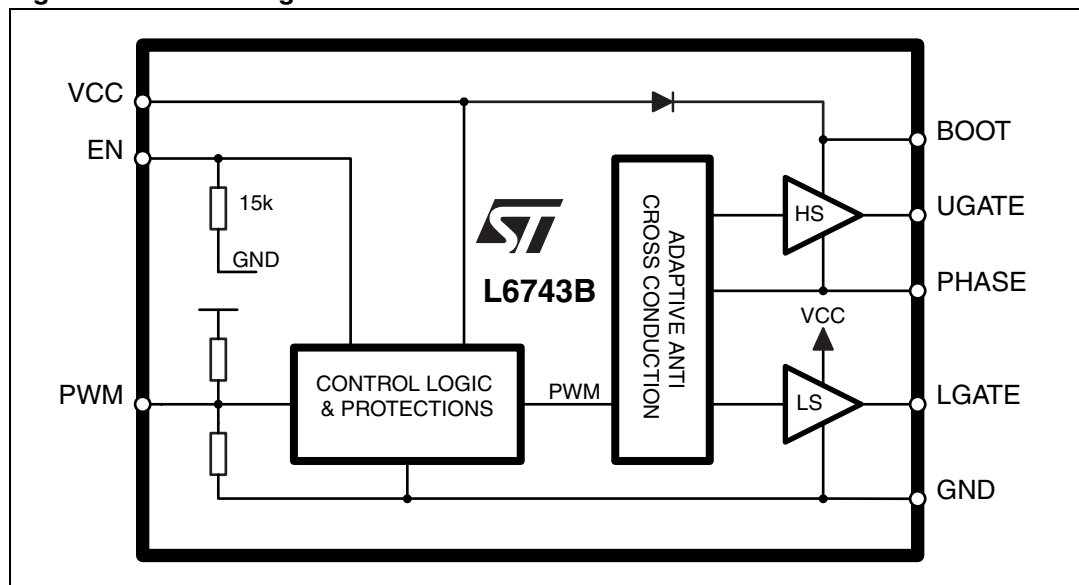
1.1 Application circuit

Figure 1. Typical application circuit



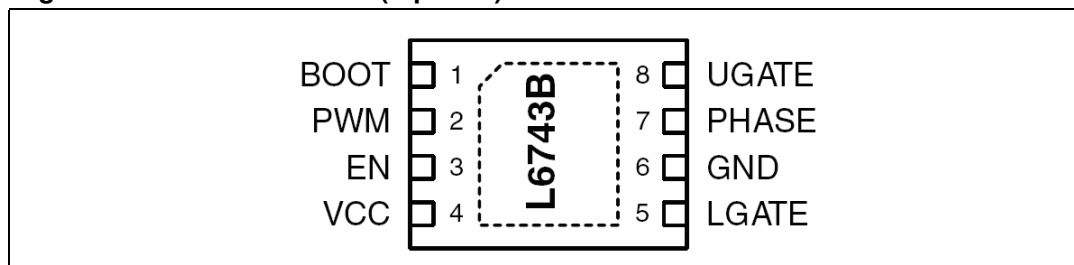
1.2 Block diagram

Figure 2. Block diagram



2 Pins description and connection diagrams

Figure 3. Pins connection (top view)



2.1 Pin description

Table 1. Pin description

Pin #	Name	Function
1	BOOT	High-side driver supply. This pin supplies the high-side floating driver. Connect through a $R_{BOOT} - C_{BOOT}$ capacitor to the PHASE pin. Internally connected to the cathode of the integrated bootstrap diode. See Section 5.3 for guidance in designing the capacitor value.
2	PWM	Control input for the driver, 5 V compatible. This pin controls the state of the driver and which external MOSFET have to be turned-ON according to EN status. If left floating and in conjunction with EN asserted, it causes the driver to enter the high-impedance (HiZ) state which causes all MOSFETs to be OFF. See Section 5.1 for details about HiZ.
3	EN	Enable input for the driver. Internally pulled low by 15 k Ω . Pull high to enable the driver according to the PWM status. If pulled low will cause the drive to enter HiZ state with all MOSFET OFF regardless of the PWM status. See Section 5.1 for details about HiZ.
4	VCC	Device and LS driver power supply. Connect to any voltage between 5 V and 12 V. Bypass with low-ESR MLCC capacitor to GND.
5	LGATE	Low-side driver output. Connect directly to the low-side MOSFET gate. A small series resistor can be useful to reduce dissipated power especially in high frequency applications.
6	GND	All internal references, logic and drivers are referenced to this pin. Connect to the PCB ground plane.
7	PHASE	high-side driver return path. Connect to the high-side MOSFET source. This pin is also monitored for the adaptive dead-time management and pre-OV protection.
8	UGATE	high-side driver output. Connect to high-side MOSFET gate.
-	TH. PAD	Thermal pad connects the silicon substrate and makes good thermal contact with the PCB. Connect to the PGND plane.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}, V_{PVCC}	to GND	-0.3 to 15	V
V_{BOOT}, V_{UGATE}	to GND to PHASE	41 15	V
V_{PHASE}	to GND	-8 to 26	V
V_{LGATE}	to GND	-0.3 to $V_{CC} + 0.3$	V
V_{PWM}, V_{EN}	to GND	-0.3 to 7	V
V_{CC}, V_{PVCC}	to GND	-0.3 to 15	V

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction to ambient (Device soldered on 2s2p, 67 mm x 69 mm board)	45	°C/W
R_{THJC}	Thermal resistance junction to case	5	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	0 to 150	°C
T_J	Junction temperature range	0 to 125	°C
P_{TOT}	Maximum power dissipation at 25 °C (Device soldered on 2s2p PC board)	2.25	W

4 Electrical specifications

4.1 Electrical characteristics

Table 4. Electrical characteristics

($V_{CC} = 12 V \pm 15\%$, $T_J = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	UGATE and LGATE = OPEN BOOT = 12 V		5		mA
I_{BOOT}	BOOT supply current	UGATE = OPEN; PHASE to GND; BOOT = 12 V		2		mA
$UVLO_{VCC}$	VCC turn-ON	VCC rising			4.1	V
	VCC turn-OFF	VCC falling	3.5			V
PWM and EN input						
PWM	Input high - V_{PWM_IH}	PWM rising	2			V
	Input low - V_{PWM_IL}	PWM falling			0.8	V
	Input leakage	PWM = 3.3 V		270		μA
		PWM = 0 V		-360		μA
t_{HiZ}	HiZ hold-off time	See Figure 4		150		ns
t_{prop_L}	Propagation delays	See Figure 4		50	75	ns
t_{prop_H}				30	45	ns
EN	Input high - V_{EN_IH}	EN rising	2			V
	Input low - V_{EN_IL}	EN falling			0.8	V
	Input resistance	to GND		15		k Ω
	Input leakage	EN = 3.3 V		220		μA
Gate drivers						
R_{HIHS}	HS source resistance	BOOT - PHASE = 12 V; 100 mA		2.3	2.8	Ω
I_{UGATE}	HS source current ⁽¹⁾	BOOT - PHASE = 12 V; C_{UGATE} to PHASE = 3.3 nF		2		A
R_{LOHS}	HS sink resistance	BOOT - PHASE = 12 V; 100 mA		2	2.5	Ω
R_{HILS}	LS source resistance	100 mA		1.3	1.8	Ω
I_{LGATE}	LS source current ⁽¹⁾	C_{LGATE} to GND = 5.6 nF		3		A
R_{LOLS}	LS sink resistance	100 mA		1	1.5	Ω
Protections						
V_{PRE_OV}	Pre-OV threshold	PHASE rising		1.8		V

1. Parameter(s) guaranteed by designed, not fully tested in production

5 Device description and operation

L6743B provides high-current driving control for both high-side and low-side N-channel MOSFETS connected as step-down DC-DC converter driven by an external PWM signal. The integrated high-current drivers allow using different types of power MOSFETs (also multiple MOS to reduce the equivalent $R_{DS(on)}$), maintaining fast switching transition.

The driver for the high-side MOSFET use BOOT pin for supply and PHASE pin for return. The driver for the low-side MOSFET use the VCC pin for supply and PGND pin for return.

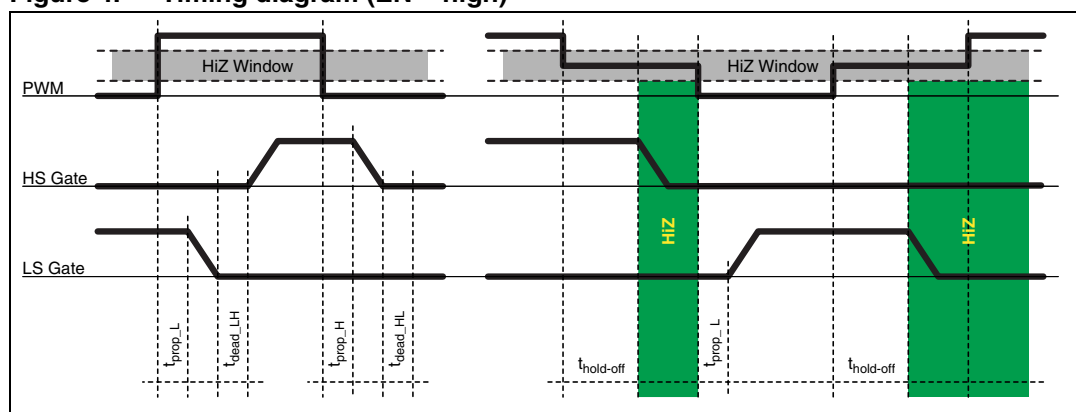
The driver embodies a anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time maintaining good efficiency saving the use of Schottky diodes: when the high-side MOSFET turns off, the voltage on its source begins to fall; when the voltage reaches about 2 V, the low-side MOSFET gate drive voltage is suddenly applied. When the low-side MOSFET turns off, the voltage at LGATE pin is sensed. When it drops below about 1 V, the high-side MOSFET gate drive voltage is suddenly applied. If the current flowing in the inductor is negative, the source of high-side MOSFET will never drop. To allow the low-side MOSFET to turn-on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET doesn't drop, the low-side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Before VCC to overcome the UVLO threshold, L6743B keeps firmly-OFF both high-side and low-side MOSFETS then, after the UVLO has been crossed, the EN and PWM inputs take the control over driver's operations. EN pin enables the driver: if low will keep all MOSFET OFF (HiZ) regardless of the status of PWM. When EN is high, the PWM input takes the control: if left floating, the internal resistor divider sets the HiZ State: both MOSFETS are kept in the OFF state until PWM transition.

After UVLO crossing and while in HiZ, the preliminary-OV protection is activated: if the voltage senses through the PHASE pin overcomes about 1.8 V, the low-side MOSFET is latched ON in order to protect the load from dangerous over-voltage. The Driver status is reset from a PWM transition.

Driver power supply as well as power conversion input are flexible: 5 V and 12 V can be chosen for high-side and low-side MOSFET voltage drive.

Figure 4. Timing diagram (EN = high)



5.1 High-impedance (HiZ) management

The driver is able to manage high-impedance state by keeping all MOSFETs in off state in two different ways.

- If the EN signal is pulled low, the device will keep all MOSFETs OFF careless of the PWM status.
- When EN is asserted, if the PWM signal remains in the HiZ window for a time longer than the hold-off time, the device detects the HiZ condition so turning off all the MOSFETs. The HiZ window is defined as the PWM voltage range comprised between V_{PWM_IL} and V_{PWM_IH} .

The device exits from the HiZ state only after a PWM transition to logic zero ($V_{PWM} < V_{PWM_IL}$).

See [Figure 4](#) for details about HiZ timings.

The implementation of the high-impedance state allows the controller that will be connected to the driver to manage high-impedance state of its output, avoiding to produce negative undershoot on the regulated voltage during the shut-down stage. Furthermore, different power management states may be managed such as pre-bias start-up.

5.2 Preliminary OV protection

After VCC has overcome its UVLO threshold and while in HiZ, L6743B activates the preliminary-OV protection.

The intent of this protection is to protect the load especially from high-side MOSFET failures during the system start-up. In fact, VRM, and more in general PWM controllers, have a 12 V bus compatible turn-on threshold and results to be non-operative if VCC is below that turn-on thresholds (that results being in the range of about 10 V). In case of a high-side MOSFET failure, the controller won't recognize the over voltage until $VCC = \sim 10$ V (unless other special features are implemented): but in that case the output voltage is already at the same voltage (~ 10 V) and the load (CPU in most cases) already burnt.

L6743B by-pass the PWM controller by latching on the low-side MOSFET in case the PHASE pin voltage overcome 2 V during the HiZ state. When the PWM input exits form the HiZ window, the protection is reset and the control of the output voltage is transferred to the controller connected to the PWM input.

Since the driver has its own UVLO threshold, a simple way to provide protection to the output in all conditions when the device is OFF consists in supplying the controller through the 5 V_{SB} bus: 5 V_{SB} is always present before any other voltage and, in case of high-side short, the low-side MOSFET is driven with 5 V assuring a reliable protection of the load.

Preliminary OV is active after UVLO and while the driver is in HiZ state and it is disabled after the first PWM transition. The controller will have to manage its output voltage from that time on.

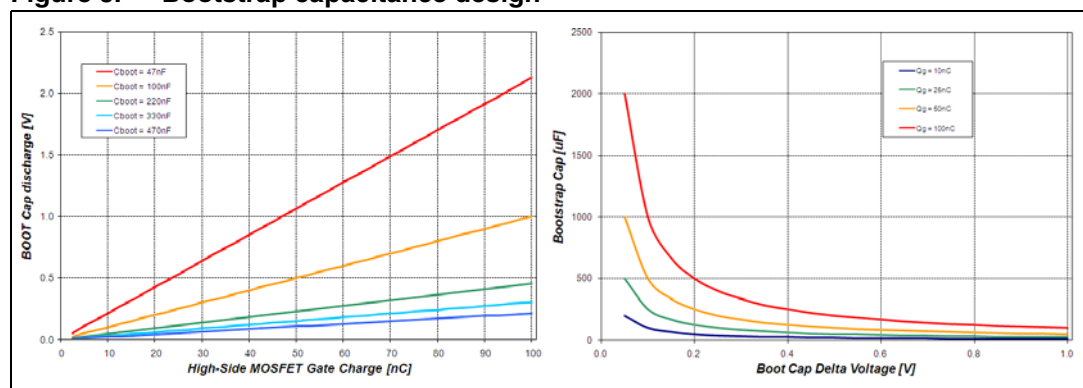
5.3 Internal BOOT diode

L6743B embeds a boot diode to supply the high-side driver saving the use of an external component. Simply connecting an external capacitor between BOOT and PHASE complete the high-side supply connections.

To prevent bootstrap capacitor to extra-charge as a consequence of large negative spikes, an external series resistance R_{BOOT} (in the range of few ohms) may be required in series to BOOT pin.

Bootstrap capacitor needs to be designed in order to show a negligible discharge due to the high-side MOSFET turn-on. In fact it must give a stable voltage supply to the high-side driver during the MOSFET turn-on also minimizing the power dissipated by the embedded Boot Diode. *Figure 5* gives some guidelines on how to select the capacitance value for the bootstrap according to the desired discharge and depending on the selected MOSFET.

Figure 5. Bootstrap capacitance design



5.4 Power dissipation

L6743B embeds high current drivers for both high-side and low-side MOSFETs: it is then important to consider the power that the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Device power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow:

$$P_{DC} = V_{CC} \cdot I_{CC} + V_{PVCC} \cdot I_{PVCC}$$

- Drivers' power is the power needed by the driver to continuously switch ON and OFF the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation.

The total power dissipated to switch the MOSFETs results:

$$P_{SW} = F_{SW} \cdot (Q_{GHS} \cdot PVCC + Q_{GLS} \cdot VCC)$$

When designing an application based on L6743B it is recommended to take into consideration the effect of external gate resistors on the power dissipated by the driver. External gate resistors help the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

Referring to [Figure 6](#), classical MOSFET driver can be represented by a push-pull output stage with two different MOSFETs: P-MOSFET to drive the external gate high and N-MOSFET to drive the external gate low (with their own R_{dsON} : R_{hi_HS} , R_{lo_HS} , R_{hi_LS} , R_{lo_LS}). The external power MOSFET can be represented in this case as a capacitance (C_{G_HS} , C_{G_LS}) that stores the gate-charge (Q_{G_HS} , Q_{G_LS}) required by the external power MOSFET to reach the driving voltage (PVCC for HS and VCC for LS). This capacitance is charged and discharged at the driver switching frequency F_{SW} .

The total power P_{sw} is dissipated among the resistive components distributed along the driving path. According to the external gate resistance and the power-MOSFET intrinsic gate resistance, the driver dissipates only a portion of P_{sw} as follow:

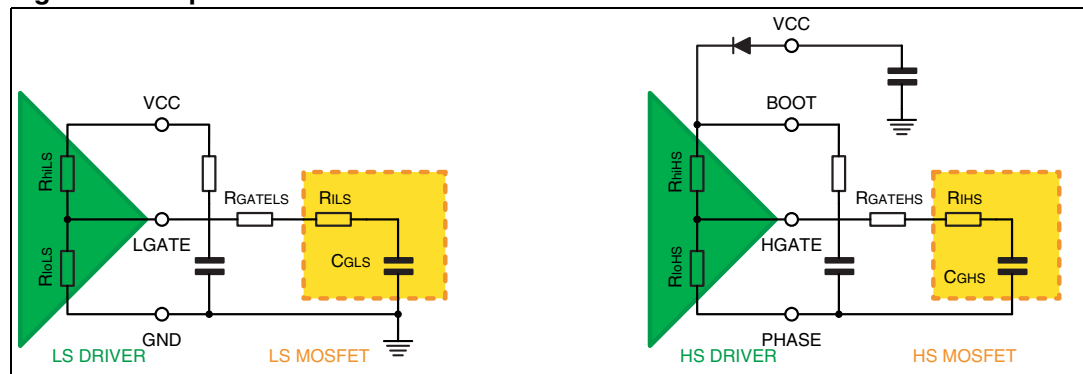
$$P_{SW-HS} = \frac{1}{2} \cdot C_{GHS} \cdot PVCC^2 \cdot F_{SW} \cdot \left(\frac{R_{hiHS}}{R_{hiHS} + R_{GateHS} + R_{iHS}} + \frac{R_{loHS}}{R_{loHS} + R_{GateHS} + R_{iHS}} \right)$$

$$P_{SW-LS} = \frac{1}{2} \cdot C_{GLS} \cdot VCC^2 \cdot F_{SW} \cdot \left(\frac{R_{hiLS}}{R_{hiLS} + R_{GateLS} + R_{iLS}} + \frac{R_{loLS}}{R_{loLS} + R_{GateLS} + R_{iLS}} \right)$$

The total power dissipated from the driver can then be determined as follow:

$$P = P_{DC} + P_{SW-HS} + P_{SW-LS}$$

Figure 6. Equivalent circuit for MOSFET drive



5.5 Layout guidelines

L6743B provides driving capability to implement high-current step-down DC-DC converters.

The first priority when placing components for these applications has to be reserved to the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (also EMI and losses) power connections must be a part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized. The critical components, such as the power MOSFETs, must be close one to the other. However, some space between the power MOSFET is still required to assure good thermal cooling and airflow.

Traces between the driver and the MOSFETs should be short and wide to minimize the inductance of the trace so minimizing ringing in the driving signals. Moreover, VIAs count needs to be minimized to reduce the related parasitic effect.

The use of multi-layer printed circuit board is recommended.

Small signal components and connections to critical nodes of the application as well as bypass capacitors for the device supply are also important. Locate the bypass capacitor (VCC, PVCC and BOOT capacitors) close to the device with the shortest possible loop and use wide copper traces to minimize parasitic inductance.

Systems that do not use Schottky diodes in parallel to the low-side MOSFET might show big negative spikes on the phase pin. This spike can be limited as well as the positive spike but has an additional consequence: it causes the bootstrap capacitor to be over-charged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the abs.max.ratings also causing device failures. It is then suggested in this cases to limit this extra-charge by adding a small resistor R_{BOOT} in series to the boot capacitor. The use of R_{BOOT} also contributes in the limitation of the spike present on the BOOT pin.

For heat dissipation, place copper area under the IC. This copper area may be connected with internal copper layers through several VIAs to improve the thermal conductivity. The combination of copper pad, copper plane and VIAs under the driver allows the device to reach its best thermal performances.

Figure 7. Driver turn-on and turn-off paths

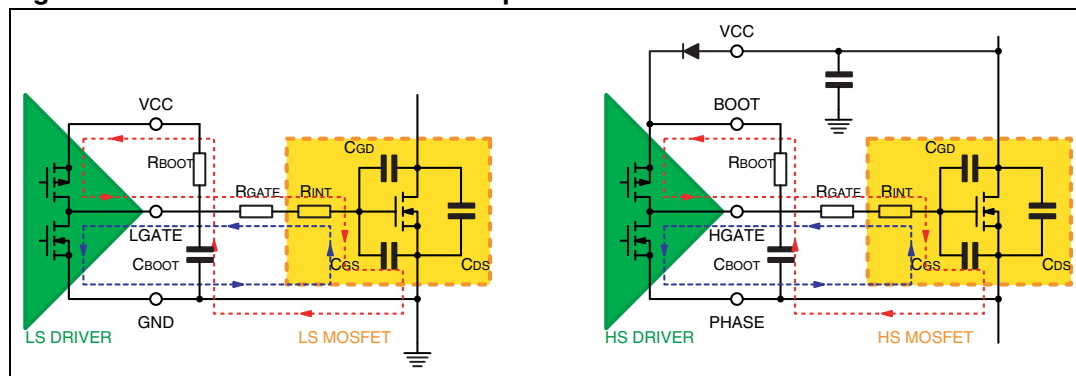
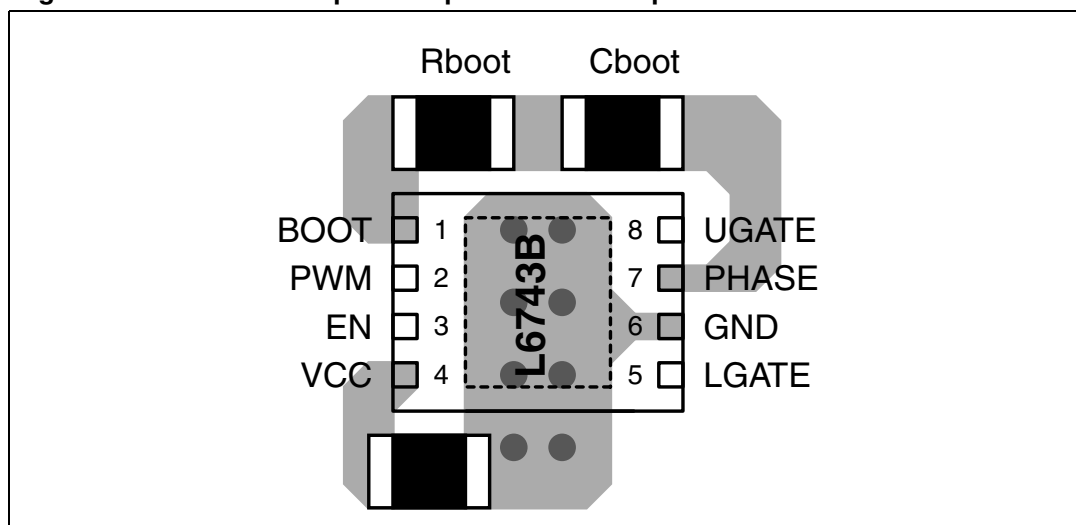


Figure 8. External components placement example



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 9. VFDFPN8 mechanical data and package dimensions

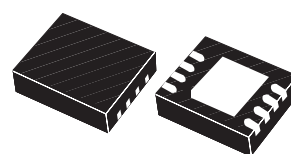
REF.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	31.49	35.43	39.37
A1		0.02	0.05		0.787	1.968
A2	0.55	0.65	0.80	21.65	25.59	31.49
A3		0.20			7.874	
b	0.18	0.25	0.30	7.086	9.842	11.81
D	2.85	3.00	3.15	112.2	118.1	124.0
D2	2.20		2.70	86.61		106.3
E	2.85	3.00	3.15	112.2	118.1	124.0
E2	1.40		1.75	55.11		68.89
e		0.50			19.68	
L	0.30	0.40	0.50	11.81	15.74	19.68
ddd			0.08			3.149



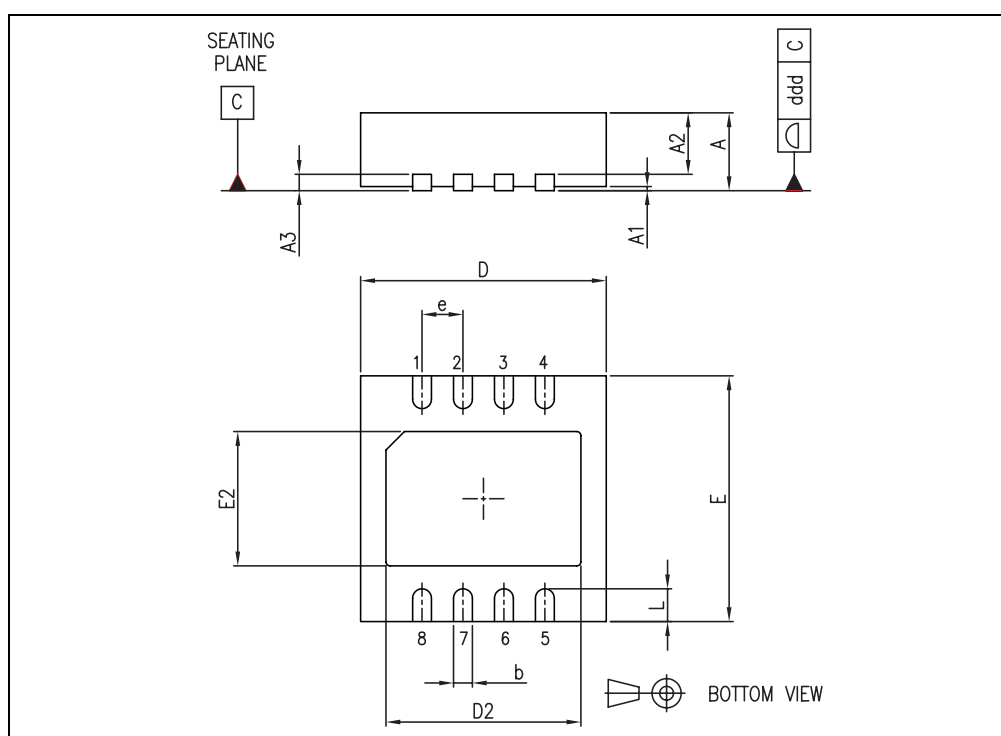
**PACKAGE AND
PACKING INFORMATION**

**Very thin Fine pitch Dual
Flat Package no Lead**

Weight: not available



VFDFPN8 (3x3)



7 Revision history

Table 5. Document revision history

Date	Revision	Changes
17-Jun-2008	1	Initial release

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