查询"74LVTH16500MEAX"供应商

March 2001
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74LVTH16500
Low Voltage 18-Bit Universal Bus Transceivers with Bushold and 3-STATE Outputs

General Description

The LVTH16500 is an 18-bit universal bus transceiver combining D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs.

The LVTH16500 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The transceiver is designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH16500 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power up/down high impedance provides glitch-free bus loading
- Outputs source/sink –32 mA/+64 mA
- Functionally compatible with the 74 series 16500
- ESD Performance:
  - Human-Body Model > 2000V
  - Machine Model > 200V
  - Charged-Device Model > 1000V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Ordering Code:

Order Number	Package Number	Package Description
74LVTH16500GX (Note 1)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LVTH16500MEA (Note 2)	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVTH16500MTD (Note 2)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 1: BGA package available in Tape and Reel only.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix "X" to the ordering code.

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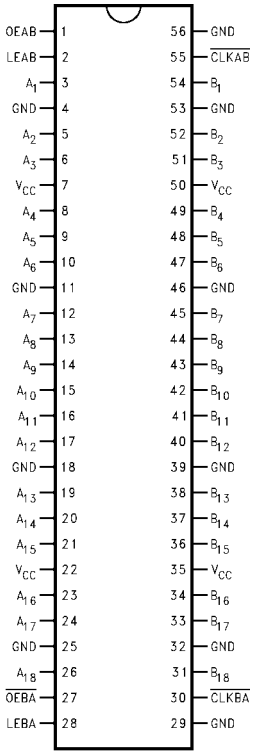
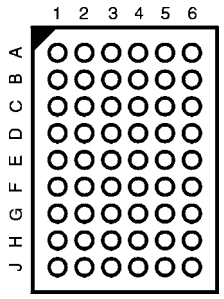
Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
A_1–A_{18}	Data Register A Inputs/3-STATE Outputs
B_1–B_{18}	Data Register B Inputs/3-STATE Outputs
$\overline{CLKAB}$, $\overline{CLKBA}$	Clock Pulse Inputs
LEAB, LEBA	Latch Enable Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	A_2	A_1	OEAB	GND	B_1	B_2
B	A_4	A_3	LEAB	$\overline{CLKAB}$	B_3	B_4
C	A_6	A_5	V_{CC}	V_{CC}	B_5	B_6
D	A_8	A_7	GND	GND	B_7	B_8
E	A_{10}	A_9	GND	GND	B_9	B_{10}
F	A_{12}	A_{11}	GND	GND	B_{11}	B_{12}
G	A_{14}	A_{13}	V_{CC}	V_{CC}	B_{13}	B_{14}
H	A_{16}	A_{15}	$\overline{OEAB}$	$\overline{CLKBA}$	B_{15}	B_{16}
J	A_{17}	A_{18}	LEBA	GND	B_{18}	B_{17}

Function Table (Note 3)

Inputs				Output
OEAB	**LEAB**	**$\overline{CLKAB}$**	**A_n**	**B_n**
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0 (Note 4)
H	L	L	X	B_0 (Note 5)

H = HIGH Voltage Level L = LOW Voltage Level
X = Immaterial Z = High Impedance
↓ = HIGH-to-LOW Clock Transition

Note 3: A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. $\overline{OEBA}$ is active LOW.

Note 4: Output level before the indicated steady-state input conditions were established.

Note 5: Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.

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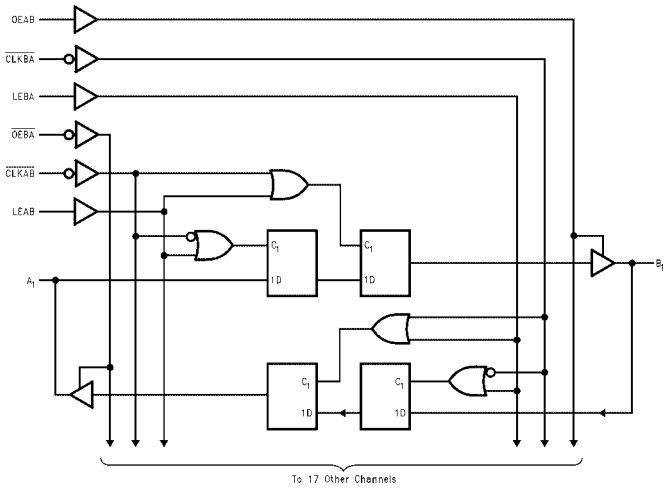
Functional Description

For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{CLKAB}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CLKAB}$. Output-enable OEAB is active-HIGH. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active-HIGH and $\overline{OEBA}$ is active-LOW).

Logic Diagram



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Absolute Maximum Ratings(Note 6)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 7)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at HIGH State	mA
		128	V_O > V_{CC} Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		−32	mA
I_{OL}	LOW-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V – 2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 6: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 7: I_O Absolute Maximum Rating must be observed.

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DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Conditions
				Min	Max		
V_{IK}	Input Clamp Diode Voltage		2.7		−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \le 0.1V$ or $V_O \ge V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage		2.7–3.6		0.8	V	
V_{OH}	Output HIGH Voltage		2.7–3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100$ µA
			2.7	2.4		V	$I_{OH} = -8$ mA
			3.0	2.0		V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	$I_{OL} = 100$ µA
			2.7		0.5	V	$I_{OL} = 24$ mA
			3.0		0.4	V	$I_{OL} = 16$ mA
			3.0		0.5	V	$I_{OL} = 32$ mA
			3.0		0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$	Bushold Input Minimum Drive		3.0	75		µA	$V_I = 0.8V$
				−75		µA	$V_I = 2.0V$
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State		3.0	500		µA	(Note 8)
				−500		µA	(Note 9)
I_I	Input Current		3.6		10	µA	$V_I = 5.5V$
		Control Pins	3.6		±1	µA	$V_I = 0V$ or V_{CC}
		Data Pins	3.6		−5	µA	$V_I = 0V$
					1	µA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0		±100	µA	$0V \le V_I$ or $V_O \le 5.5V$
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current		0–1.5V		±100	µA	$V_O = 0.5V$ to $3.0V$, V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		−5	µA	$V_O = 0.0V$
I_{OZH}	3-STATE Output Leakage Current		3.6		5	µA	$V_O = 3.6V$
I_{OZH+}	3-STATE Output Leakage Current		3.6		10	µA	$V_{CC} < V_O \le 5.5V$
I_{CCH}	Power Supply Current		3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current		3.6		5	mA	Outputs LOW
I_{CCZ}	Power Supply Current		3.6		0.19	mA	Outputs Disabled
I_{CCZ+}	Power Supply Current		3.6		0.19	mA	$V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 10)		3.6		0.2	mA	One Input at $V_{CC} - 0.6V$, Other Inputs at V_{CC} or GND

Note 8: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 9: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 10: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 11)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions
			Min	Typ	Max		$C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 12)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 12)

Note 11: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 12: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output under test held LOW.

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AC Electrical Characteristics

Symbol	Parameter		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\ \Omega$				Units
			$V_{CC} = 3.3 \pm 0.3V$		$V_{CC} = 2.7V$		
			Min	Max	Min	Max	
f_{MAX}	$\overline{CLKAB}$ or $\overline{CLKBA}$ to B or A		150		150		MHz
t_{PLH}	Propagation Delay		1.3	5.2	1.3	5.8	ns
t_{PHL}	Data to Outputs		1.3	4.7	1.3	5.3	
t_{PLH}	Propagation Delay		1.5	5.5	1.5	6.3	ns
t_{PHL}	LEBA or LEAB to B or A		1.5	5.1	1.5	5.7	
t_{PLH}	Propagation Delay		1.3	5.8	1.3	6.9	ns
t_{PHL}	$\overline{CLKBA}$ or $\overline{CLKAB}$ to B or A		1.2	5.0	1.3	5.9	
t_{PZH}	Output Enable Time		1.2	5.0	1.3	5.7	ns
t_{PZL}			1.3	5.5	1.3	6.5	
t_{PHZ}	Output Disable Time		1.7	6.0	1.7	6.7	ns
t_{PLZ}			1.6	5.8	1.7	6.3	
t_{SU}	Setup Time	A before $\overline{CLKAB}$	2.9		2.9		ns
		B before $\overline{CLKBA}$	2.9		2.9		
		A or B before LE, $\overline{CLK}$ HIGH	1.8		0.9		
		A or B before LE, $\overline{CLK}$ LOW	2.9		2.3		
t_H	Hold Time	A or B after $\overline{CLK}$	0.5		0.9		ns
		A or B after LE	1.6		1.6		
t_W	Pulse Duration	LE HIGH	3.3		3.3		ns
		$\overline{CLK}$ HIGH or LOW	3.3		3.3		
t_{OSLH}	Output to Output Skew (Note 13)			1.0		1.0	ns
t_{OSHL}				1.0		1.0	

Note 13: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 14)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

Note 14: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

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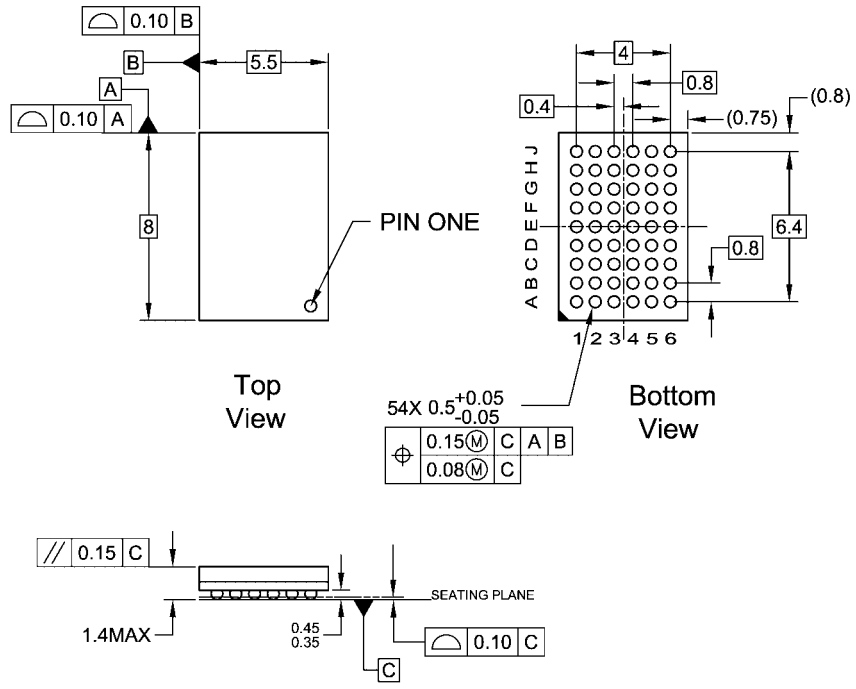
Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary

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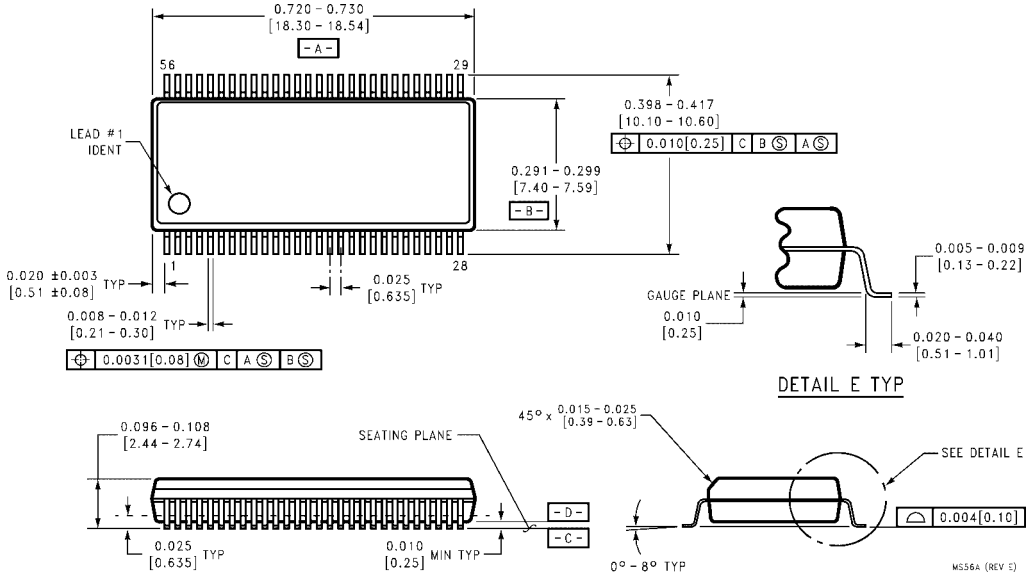

56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

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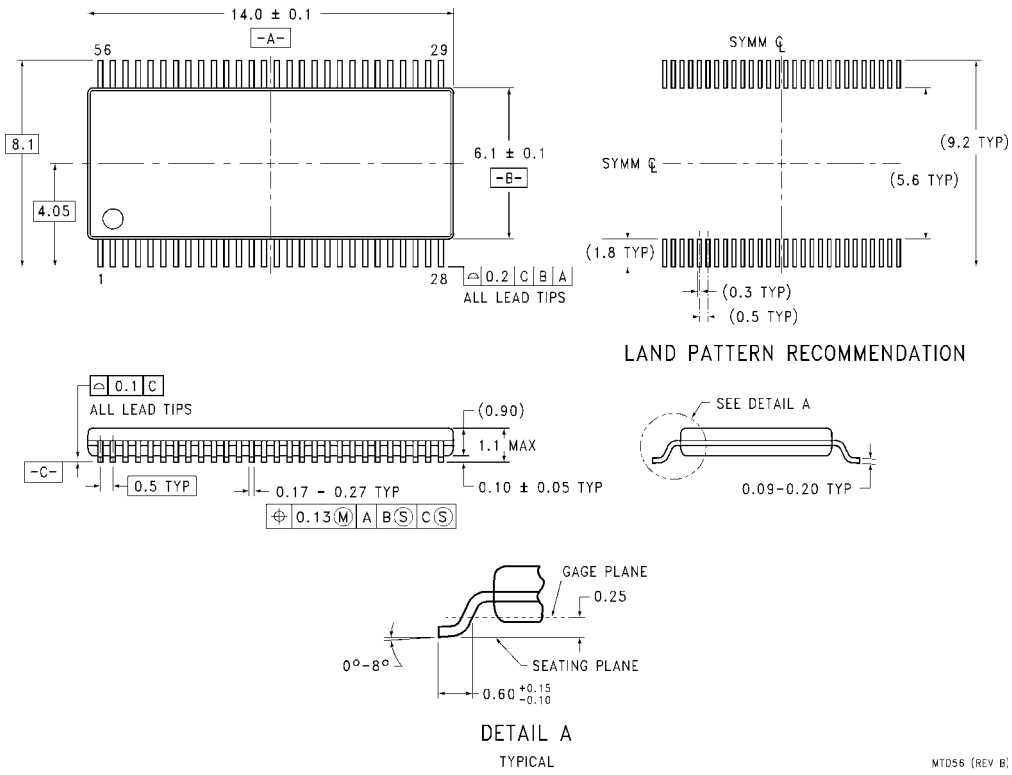
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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