REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to boilerplate. Add column for data retention to section 1.2.1. Convert case outline X reference to MIL-STD-1835. Add device types 06 and 07. Add CAGE codes 65786 and 0EU86 as sources of supply for device types 06 and 07. Editorial changes throughout.	94-03-24	M. A. Frye

REV																			
SHEET																			
REV	A	A	A	A															
SHEET	15	16	17	18															

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
1 December 1989

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 64K X 4 SRAM WITH OE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89524
A	67268	

SHEET 1 OF 18

DESC FORM 193
JUL 91

5962-E028-94

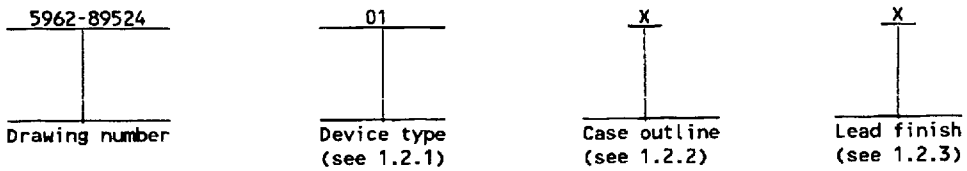
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0001330 989

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Data retention	Access time
01	(See 6.6)	64K X 4 CMOS static RAM	Yes	70 ns
02	(See 6.6)	64K X 4 CMOS static RAM	Yes	55 ns
03	(see 6.6)	64K X 4 CMOS static RAM	Yes	45 ns
04	(see 6.6)	64K X 4 CMOS static RAM	Yes	35 ns
05	(see 6.6)	64K X 4 CMOS static RAM	Yes	25 ns
06	(see 6.6)	64K X 4 CMOS static RAM	No	20 ns
07	(see 6.6)	64K X 4 CMOS static RAM	No	15 ns

1.2.2 Case outlines. The case outlines shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	dual-in-line
Y	CQCC3-N28	28	rectangular leadless chip carrier

1.3 Absolute maximum ratings.

Terminal voltage with respect to ground	-0.5 V dc to +7.0 V dc
DC output current	50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Y	See MIL-STD-1835
Junction temperature (T_J)	+150°C 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.2 V dc to 6.0 V dc
Low level input voltage range (V_{IL})	-0.5 V dc to +0.8 V dc 2/
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady state life.
2/ V_{IL}(min) = -3.0 V dc for pulse width less than 20 ns.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Die overcoat. Polyimide and silicon coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-I-38535) shall be subjected to and pass the internal moisture content test, (test method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IL} = 0.8 V, V_{IH} = 2.2 V	1,2,3	All		0.4	V
Input leakage current	I_{LI}	V_{CC} = 5.5 V, GND $\le V_{IN} \le V_{CC}$	1,2,3	All		±10.0	µA
Output leakage current	I_{LO}	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}, GND $\le V_{OUT} \le V_{CC}$	1,2,3	All		±10.0	µA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, $\overline{CE}$ = 0.8 V, $f = 1/t_{AVQV}$, $\overline{OE}$ = 2.4 V	1,2,3	01-05		120	mA
				06		150	
				07		160	
Standby supply current (TTL)	I_{CC2} 1/	V_{CC} = 5.5 V, $\overline{CE}$ = 2.4 V, f = 0 Hz, $\overline{OE}$ = 2.4 V	1,2,3	01-05		20	mA
				06,07		40	
Standby supply current (CMOS)	I_{CC3} 1/	V_{CC} = 5.5 V, $\overline{CE}$ = V_{CC} - 0.3 V, f = 0 Hz	1,2,3	01-05		10	mA
				06,07		20	
Data retention supply current	I_{CC4} 1/	V_{CC} = 2.0 V, $\overline{CE} \ge V_{CC}$ - 0.2 V f = 0 MHz, Applies only to devices with data retention.	1,2,3	01-05		1	mA
Input capacitance	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C, see 4.3.1c	4	All		11	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0 V, f = 1.0 MHz, T_A = +25°C see 4.3.1c	4	All		11	pF
Functional tests		See 4.3.1d	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}	See figures 3 and 4 2/	9,10,11	01	70		ns
				02	55		
				03	45		
				04	35		
				05	25		
				06	20		
				07	15		
Address access time	t_{AVQV}		9,10,11	01		70	ns
				02		55	
				03		45	
				04		35	
				05		25	
				06		20	
				07		15	
Output hold from address change	t_{AVQX}		9,10,11	All	3.0		ns
Chip select access time	t_{ELQV}		9,10,11	01		70	ns
				02		55	
				03		45	
				04		35	
				05		25	
				06		20	
				07		15	
Chip select to output in low Z	t_{ELQX}	See figures 3 and 4 3/ 4/	9,10,11	All	3.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Chip deselect to output in high Z	t_{EHQZ}	See figures 3 and 4 3/ 4/	9,10,11	01		30	ns
				02		25	
				03		20	
				04,05		15	
				06		10	
				07		8	
Output enable to output valid	t_{OLQV}	See figures 3 and 4	9,10,11	01		45	ns
				02		35	
				03		30	
				04		25	
				05		15	
				06		10	
				07		8	
Output enable to output in low Z	t_{OLQX}	See figures 3 and 4 3/ 4/	9,10,11	All	0		ns
Output disable to output in high Z	t_{OHQZ}		9,10,11	01		25	ns
				02-04		20	
				05		15	
				06,07		9	
Write cycle time	t_{AVAV}	See figures 3 and 5 2/	9,10,11	01	70		ns
				02	55		
				03	45		
				04	35		
				05	25		
				06	20		
				07	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip select to end of write	t_{ELEH}	See figures 3 and 5 2/	9,10,11	01-03	30		ns
				04	25		
				05	20		
				06	15		
				07	10		
Address valid to end of write	t_{AVWH}		9,10,11	01-03	30		ns
				04	25		
				05	20		
				06	15		
				07	10		
Address setup time	t_{AVWL}		9,10,11	All	0		ns
Write pulse width	t_{WLWH}		9,10,11	01-03	30		ns
				04	25		
				05	20		
				06	15		
				07	10		
Write recovery time	t_{WHAX} t_{EHAX}		9,10,11	All	0		ns
Data valid to end of write	t_{DVWH}		9,10,11	01-04	20		ns
				05	15		
				06	10		
				07	9		
Data hold time	t_{WHDX}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write enable to output in high Z	t_{WLQZ}	See figures 3 and 5 3/ 4/	9,10,11	01		30	ns
				02		25	
				03		20	
				04,05		15	
				06		10	
				07		7	
Output active from end of write	t_{WHQX}		9,10,11	All	0		ns
Chip deselect to data retention time	t_{CDR}	$\overline{CS} \ge V_{CC}$ -0.2 V, see figure 6 3/	9,10,11	All	0		ns
Operation recovery time	t_R		9,10,11	All	t_{AVAV}		ns

1/ At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{AVAV}$. f = 0 means no input lines change.
2/ Test conditions assume signal transition times of 5.0 ns or less. Timing is referenced at input and output levels of 1.5 V and input pulse levels of 0 to 3.0 V. Output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 30 pF.
3/ If not tested, shall be guaranteed to the limits specified in table I.
4/ Test conditions assume signal transition times of 5.0 ns or less. Transition is measured at steady-state high level of -500 mV or steady-state low level of +500 mV on the output from 1.5 V level on the input with a load capacitance of 5.0 pF.

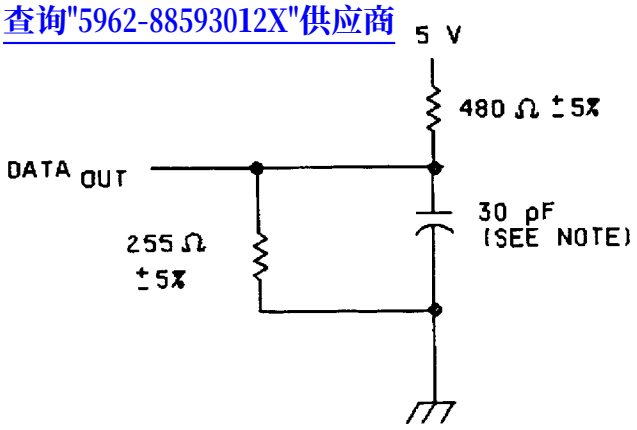
Device types	ALL	
Case outlines	X	Y
Terminal number	Terminal symbol	
1	NC	NC
2	A_0	A_0
3	A_1	A_1
4	A_2	A_2
5	A_3	A_3
6	A_4	A_4
7	A_5	A_5
8	A_6	A_6
9	A_7	A_7
10	A_8	A_8
11	A_9	A_9
12	$\overline{CE}$	$\overline{CE}$
13	OE	OE
14	GND	GND
15	$\overline{WE}$	NC
16	I/O_1	$\overline{WE}$
17	I/O_2	I/O_1
18	I/O_3	I/O_2
19	I/O_4	I/O_3
20	NC	I/O_4
21	NC	A_{10}
22	A_{10}	A_{11}
23	A_{11}	A_{12}
24	A_{12}	A_{13}
25	A_{13}	A_{14}
26	A_{14}	A_{15}
27	A_{15}	NC
28	V_{CC}	V_{CC}

NC = no connection

Figure 1. Terminal connections.

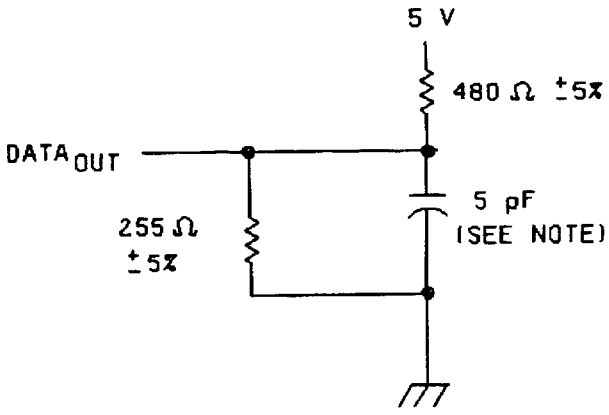
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	OUTPUTS	Power
Standby	H	X	X	High Z	Standby
Read	L	H	L	Data Out	Active
Write	L	L	X	Data In	Active
Deselect	L	H	H	High Z	Active

Figure 2. Truth table.



CIRCUIT A

Output load



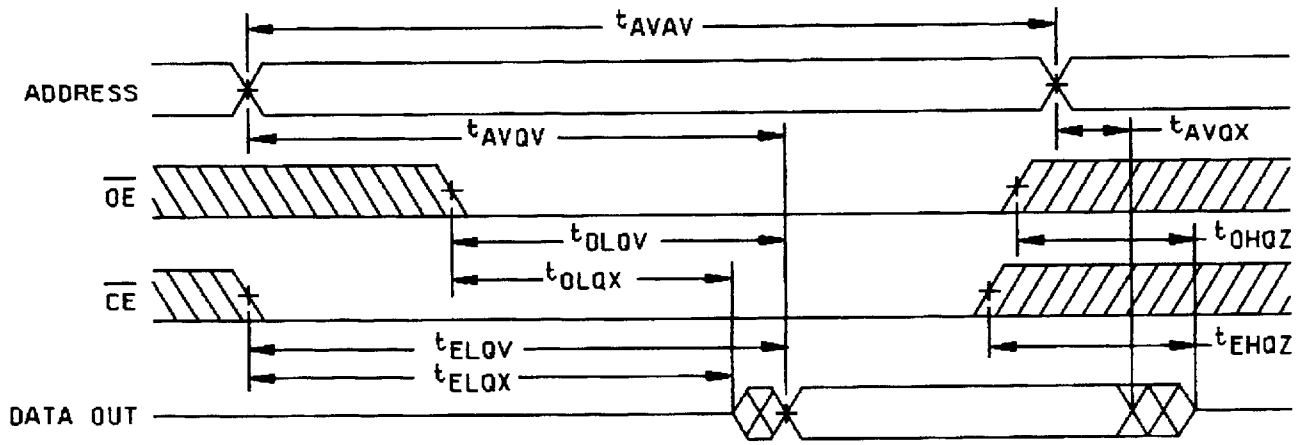
CIRCUIT B

(for t_{OLQX}, t_{ELQX}, t_{OHQZ}, t_{WLQZ}, t_{EHQZ}, t_{WHQX})

NOTE: Including scope and jig (minimum values).

FIGURE 3. Output load circuit.

READ CYCLE NUMBER 1
SEE NOTE 1



READ CYCLE NUMBER 2
SEE NOTES 1,2, AND 4

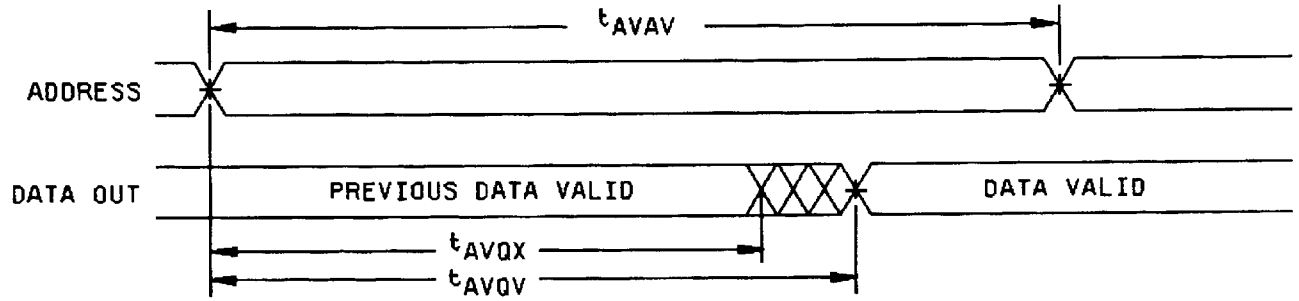
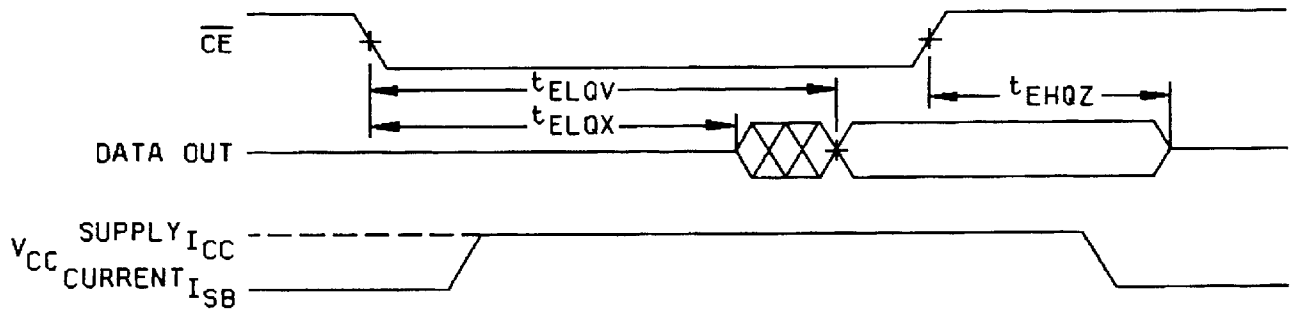


FIGURE 4. Read cycle timing diagrams.

READ CYCLE NUMBER 3
SEE NOTES 1,3, AND 4



NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected. $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

FIGURE 4. Read cycle timing diagrams - continued.

WRITE CYCLE NUMBER 1 - $\overline{WE}$ CONTROLLED
SEE NOTES 1,2,3, AND 6

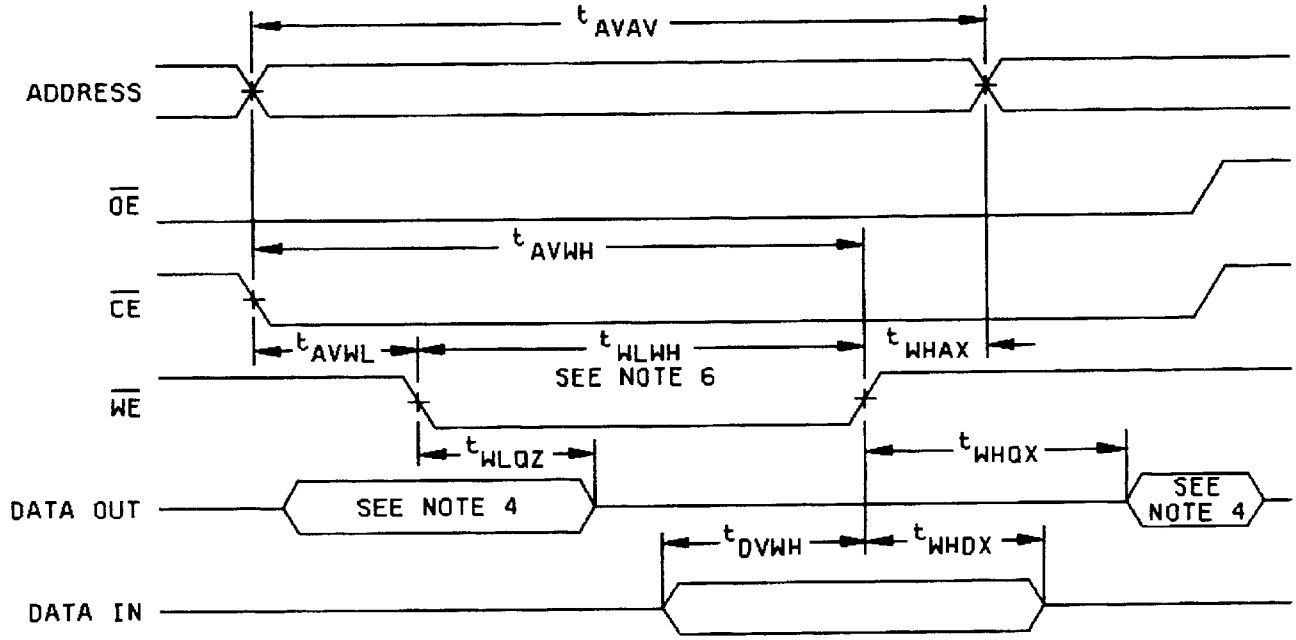
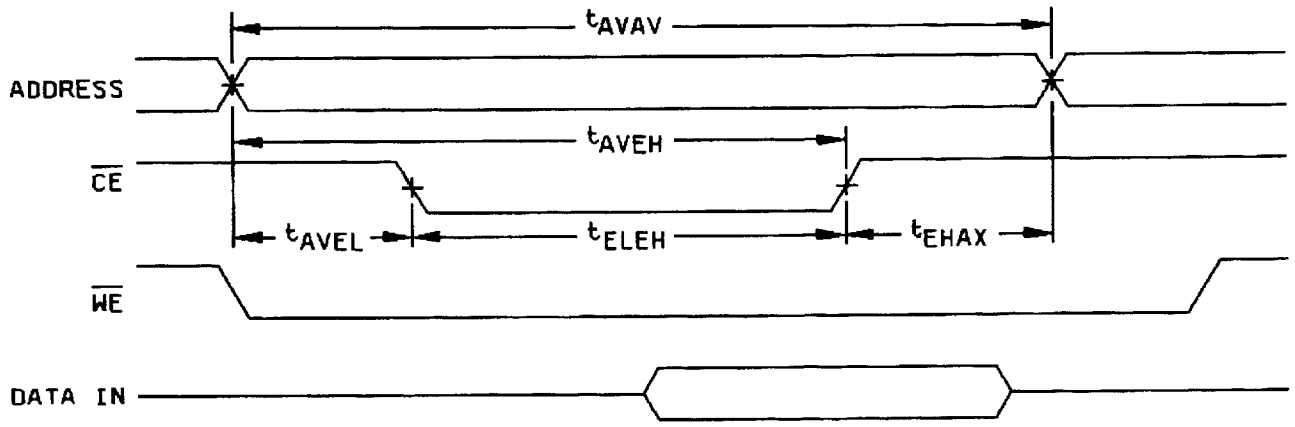


FIGURE 5. Write cycle timing diagrams.

WRITE CYCLE NUMBER 2 - $\overline{CS}$ CONTROLLED
SEE NOTES 1,2,3, AND 5



NOTES:
1. $\overline{WE}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{ELEH} or t_{WLWH}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WHAX} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WLWH} or (t_{WLQZ} + t_{DVWH}) to allow the I/O drivers to turn off and data to be placed on the bus for required t_{DVEH}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WLWH}.

FIGURE 5. Write cycle timing diagrams - continued.

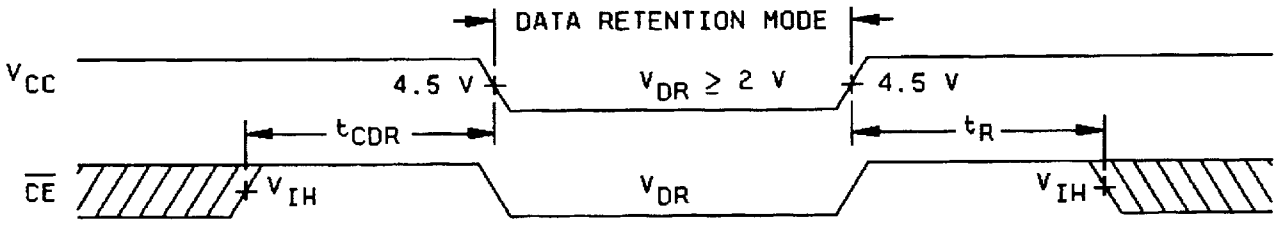


FIGURE 6. Low V_{CC} data retention timing diagram.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A,8B, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8A, 8B,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1c

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.