

2SK1697

Silicon N-Channel MOS FET

REJ03G1373-0200
(Previous: ADE-208-1313)
Rev.2.00
May 11, 2006

Application

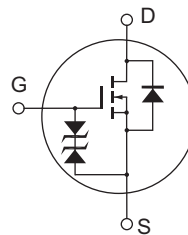
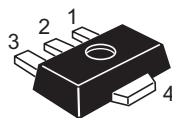
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source.
- Suitable for DC – DC converter, motor drive, power switch, solenoid drive

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK®)



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "EY".

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.5	A
Drain peak current	$I_{D(pulse)}^{*1}$	1.5	A
Body to drain diode reverse drain current	I_{DR}	0.5	A
Channel dissipation	P_{ch}^{*2}	1	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. When using the alumina ceramic board (12.5 × 20 × 0.7 mm)

Electrical Characteristics

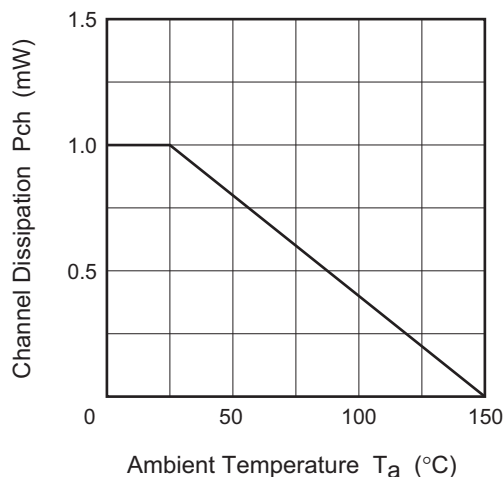
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	50	μA	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.3	1.7	Ω	$I_D = 0.3 \text{ A}$, $V_{GS} = 10 \text{ V}^{*1}$
		—	1.8	2.5	Ω	$I_D = 0.3 \text{ A}$, $V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	0.25	0.38	—	S	$I_D = 0.3 \text{ A}$, $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	33	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	17	—	pF	
Reverse transfer capacitance	C_{rss}	—	5	—	pF	
Turn-on delay time	$t_{d(on)}$	—	3	—	ns	$I_D = 0.3 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_L = 100 \Omega$
Rise time	t_r	—	8	—	ns	
Turn-off delay time	$t_{d(off)}$	—	18	—	ns	
Fall time	t_f	—	14	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1	—	V	$I_F = 0.5 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	45	—	ns	$I_F = 0.5 \text{ A}$, $V_{GS} = 0$, $di_F/dt = 50 \text{ A}/\mu\text{s}$

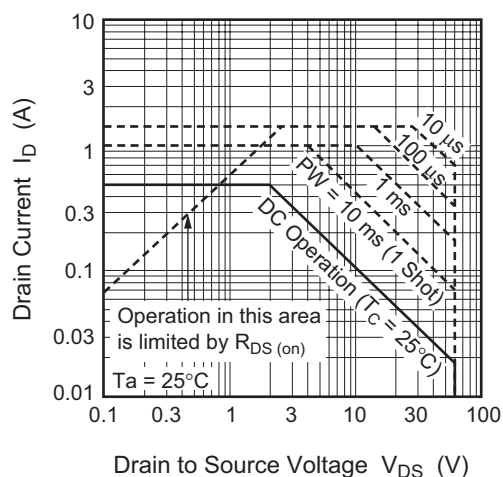
Note: 1. Pulse test

Main Characteristics

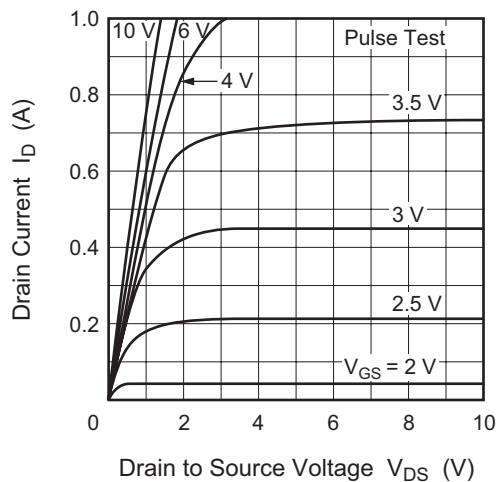
Power vs. Temperature Derating



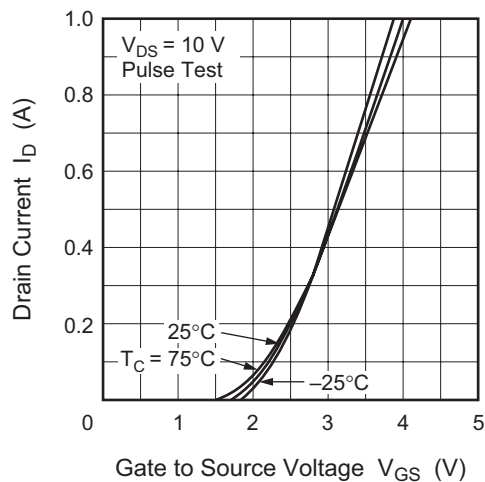
Maximum Safe Operation Area



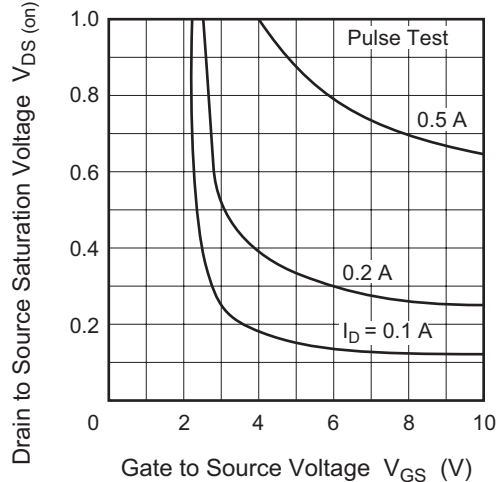
Typical Output Characteristics



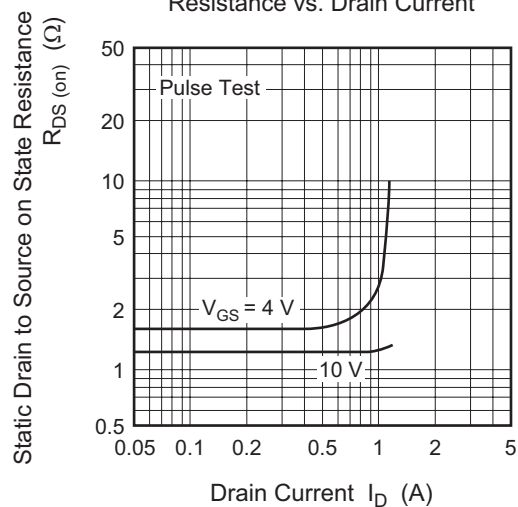
Typical Transfer Characteristics

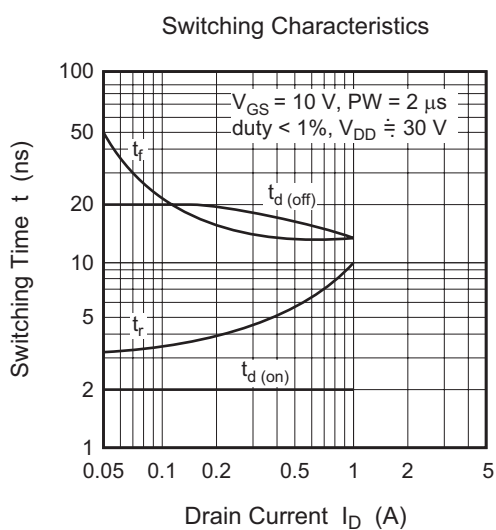
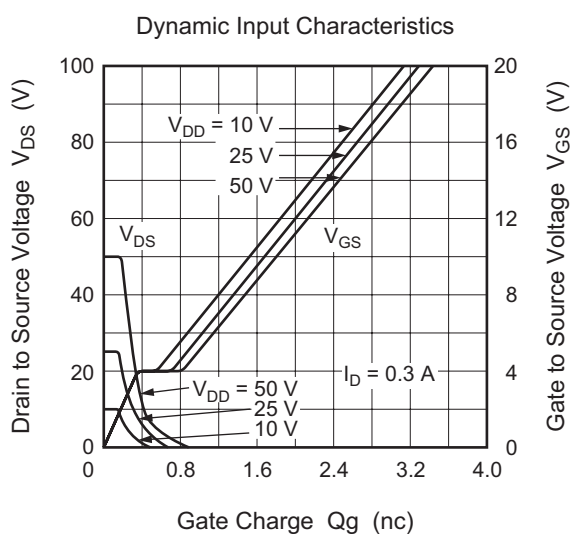
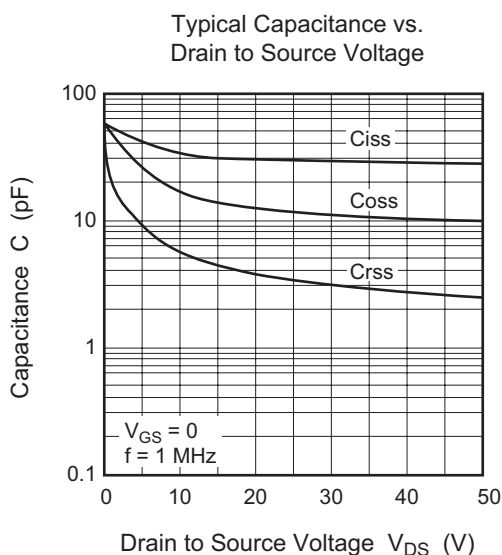
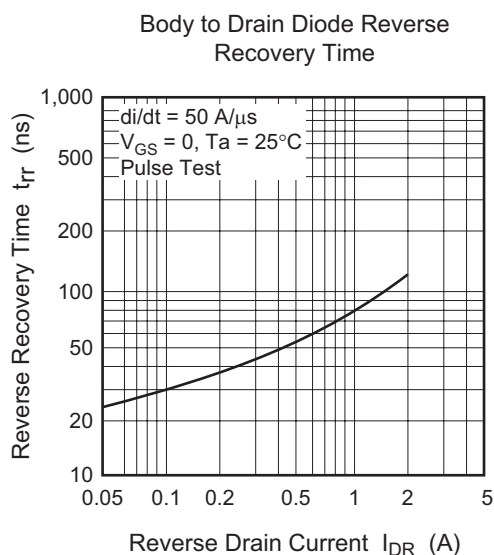
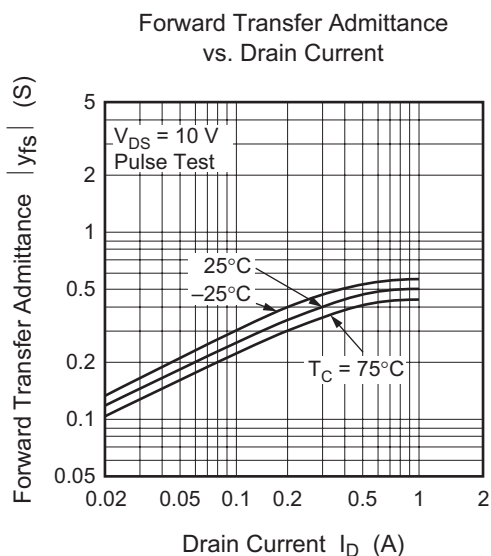
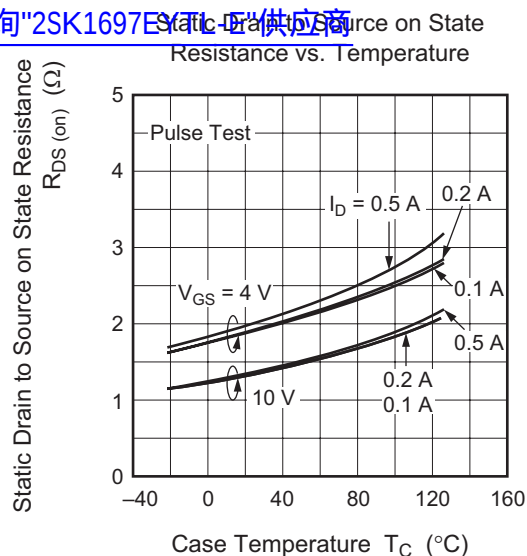


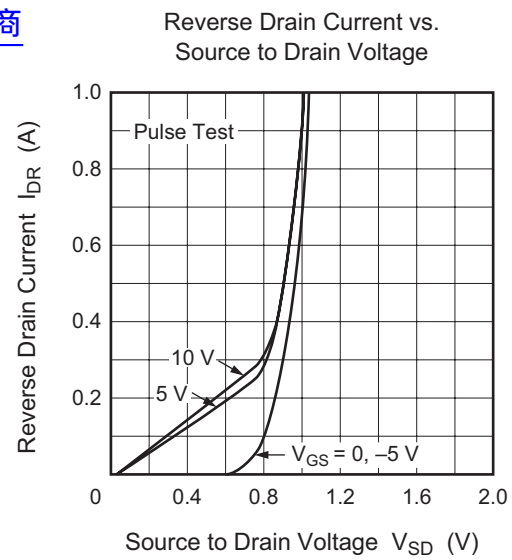
Drain to Source Saturation Voltage vs. Gate to Source Voltage



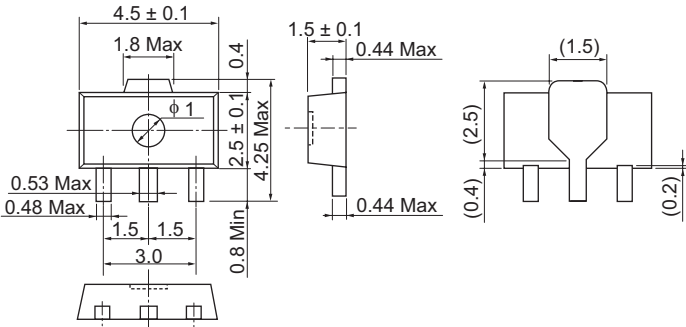
Static Drain to Source on State Resistance vs. Drain Current



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Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
UPAK	SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g	
 The drawing shows three views of the package: a top view, a side view, and a front view. The top view shows a rectangular package with a central circular feature of diameter 1.0 mm. Dimensions include a total width of 4.5 ± 0.1 mm, a top width of 1.8 Max mm, a central width of 1.5 mm, and a bottom width of 3.0 mm. The side view shows a height of 1.5 ± 0.1 mm and a base width of 0.44 Max mm. The front view shows a width of 1.5 mm and a height of 0.4 mm. Other dimensions include 0.53 Max mm, 0.48 Max mm, 2.5 ± 0.1 mm, 4.25 Max mm, and 0.8 Min mm.					

Ordering Information

Part Name	Quantity	Shipping Container
2SK1697EYTL-E	1000 pcs	φ178 mm Reel, 12 mm Emboss Taping
2SK1697EYTR-E		

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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