查询"ADG854BCPZ-REEL"供应商

1.6 Ω On Resistance, 15 V *i*CMOS SPST Switch

ADG1517

FEATURES

- 1.6 Ω on resistance
- 0.4 Ω on resistance flatness
- Up to 250 mA continuous current
- Fully specified at 15 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 8-lead 3 mm × 2 mm LFCSP package

APPLICATIONS

- Audio signal routing
- Video signal routing
- Battery-powered systems
- Communication systems
- Data acquisition systems
- Relay replacement

FUNCTIONAL BLOCK DIAGRAM

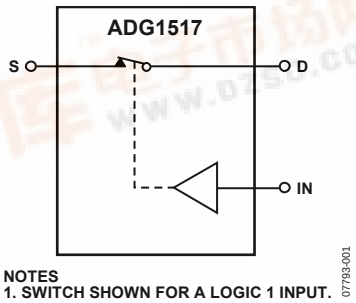

Figure 1.

GENERAL DESCRIPTION

The ADG1517 is a single-pole/single-throw (SPST) switch. Figure 1 shows that with a logic input of 1, the switch of the ADG1517 is closed. The switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The *i*CMOS™ (industrial CMOS) modular manufacturing process combines high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 1.85 Ω maximum on resistance at 25°C.
2. Minimum distortion.
3. 3 V logic-compatible digital inputs: V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. No V_L logic power supply required.

Rev. 0
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REVISION HISTORY

10/08—Revision 0: Initial Version

SPECIFICATIONS

SINGLE SUPPLY

V_{DD} = 15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	1.6			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 13
	1.85	2.4	2.75	Ω max	V_{DD} = 13.5 V
On Resistance Flatness ($R_{FLAT(ON)}$)	0.4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
LEAKAGE CURRENTS					V_{DD} = 16.5 V
Source Off Leakage, I_S (Off)	±10			nA typ	V_S = 1 V, V_D = 10 V; or V_S = 10 V, V_D = 1 V; see Figure 14
Drain Off Leakage, I_D (Off)	±10			nA typ	V_S = 1 V, V_D = 10 V; or V_S = 10 V, V_D = 1 V; see Figure 14
Channel On Leakage, I_D, I_S (On)	±10			nA typ	V_S = V_D = 1 V or 10 V, see Figure 15
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	135			ns typ	R_L = 300 Ω, C_L = 35 pF
	175	220	250	ns max	V_S = 10 V; see Figure 19
t_{OFF}	115			ns typ	R_L = 300 Ω, C_L = 35 pF
	155	190	220	ns max	V_S = 10 V; see Figure 19
Charge Injection	70			pC typ	V_S = 8 V, R_S = 0 Ω, C_L = 1 nF; see Figure 20
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 16
Total Harmonic Distortion + Noise (THD + N)	0.04			% typ	R_L = 110 Ω, 7.5 V p-p, f = 20 Hz to 20 kHz; see Figure 18
−3 dB Bandwidth	65			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 17
Insertion Loss	−0.16			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 17
C_S (Off)	68			pF typ	f = 1 MHz; V_S = 7.5 V
C_D (Off)	68			pF typ	f = 1 MHz; V_S = 7.5 V
C_D, C_S (On)	185			pF typ	f = 1 MHz; V_S = 7.5 V
POWER REQUIREMENTS					V_{DD} = 16.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	75			μA typ	Digital inputs = 5 V
			145	μA max	
V_{DD}			5/16.5	V min/max	GND = 0 V

[1] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT, S OR D

Table 2.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, S or D[1, 2]	250	150	100	mA max	V_{DD} = 13.5 V, GND = 0 V

[1] Guaranteed by design, not subject to production test.
[2] Data based on θ_{JA} data shown in Table 4.

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +25 V
Analog Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	Data in Table 2 + 10% (pulsed at 1 ms, 10% duty cycle max)
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a 4-layer board and with the exposed pad soldered to the board.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead LFCSP (CP-8-4)	50.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

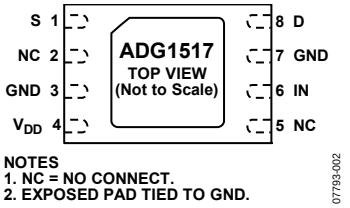

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S	Source Terminal. Can be an input or output.
2	NC	No Connect.
3	GND	Ground (0 V) Reference. Both GND pins must be connected to GND potential.
4	V_{DD}	Most Positive Power Supply Potential.
5	NC	No Connect.
6	IN	Logic Control Input.
7	GND	Ground (0 V) Reference. Both GND pins must be connected to GND potential.
8	D	Drain Terminal. Can be an input or output.
9 (EPAD)	Exposed Paddle (EPAD)	The exposed paddle should be tied to GND.

Table 6. Truth Table

ADG1517 IN Pin	Switch Condition
1	On
0	Off

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TYPICAL PERFORMANCE CHARACTERISTICS

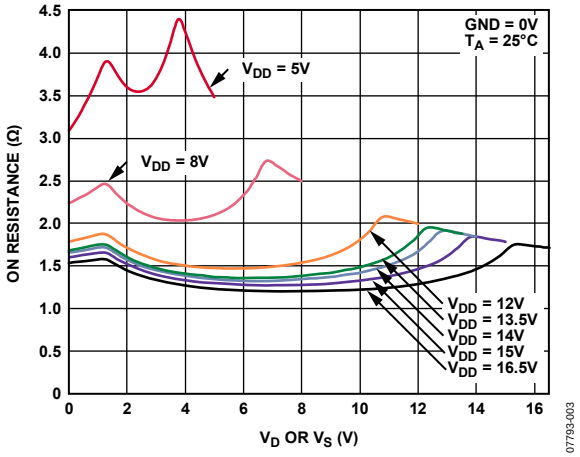

Figure 3. On Resistance as a Function of V_D or V_S for Single Supply

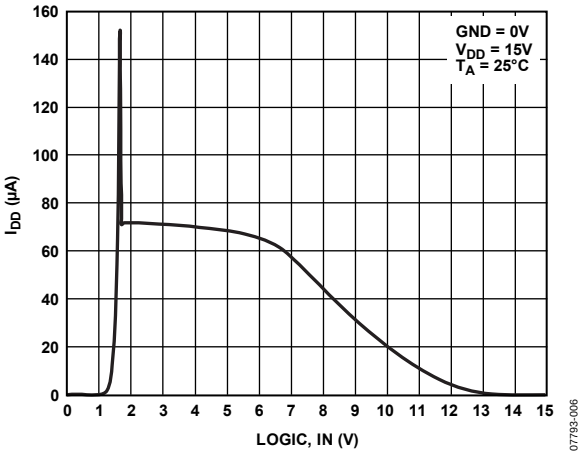

Figure 6. I_{DD} vs. Logic Level

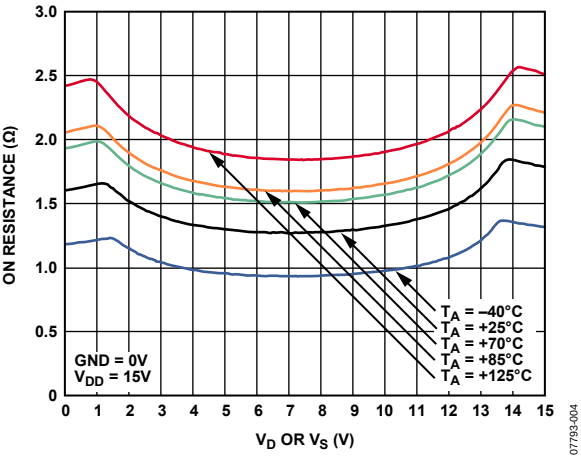

Figure 4. On Resistance as a Function of V_D or V_S for Different Temperatures, Single Supply

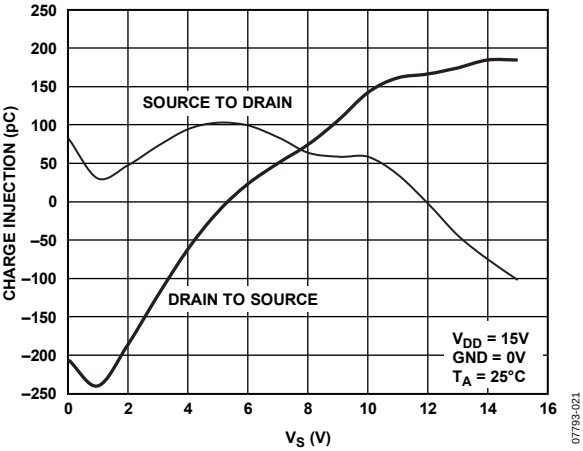

Figure 7. Charge Injection vs. Source Voltage

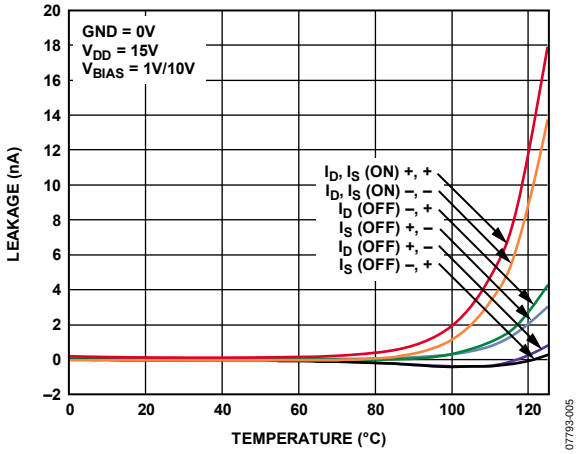

Figure 5. Leakage Currents as a Function of Temperature, Single Supply

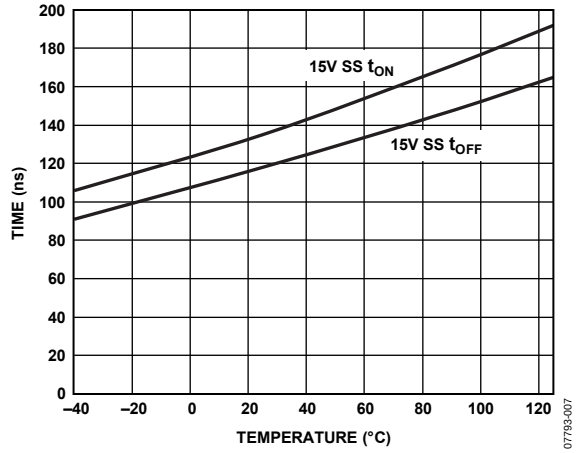

Figure 8. t_{ON}/t_{OFF} Times vs. Temperature

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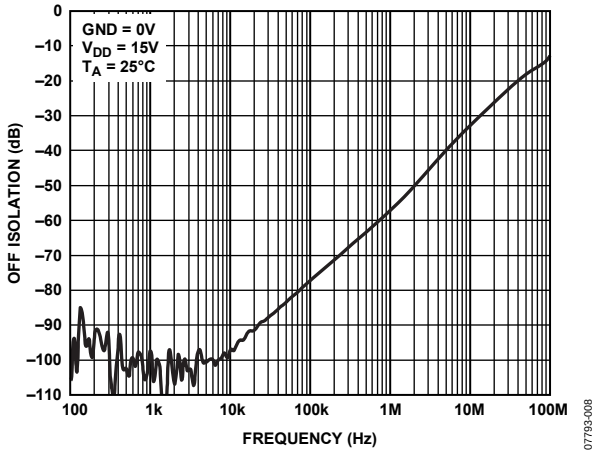

Figure 9. Off Isolation vs. Frequency

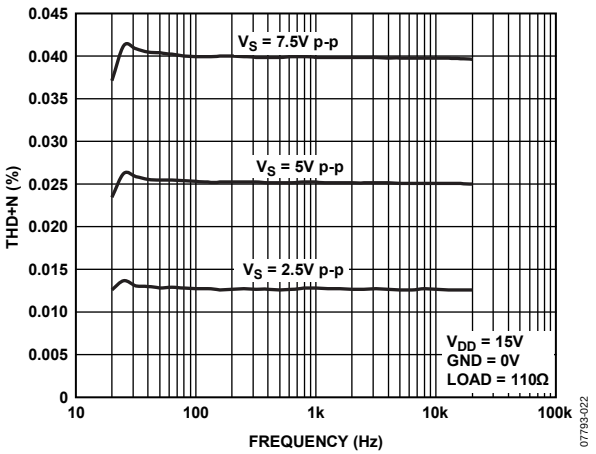

Figure 11. THD + N vs. Frequency

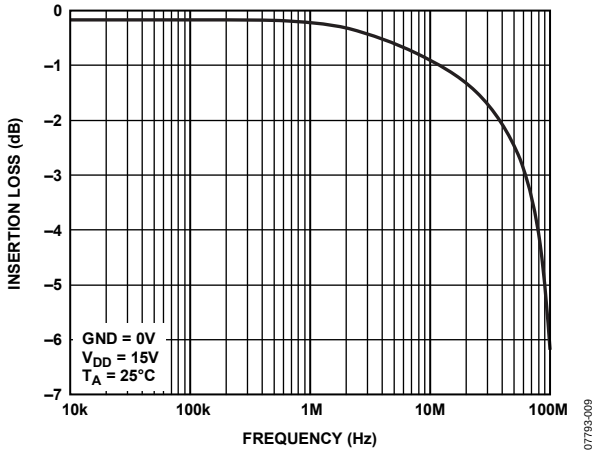

Figure 10. On Response vs. Frequency

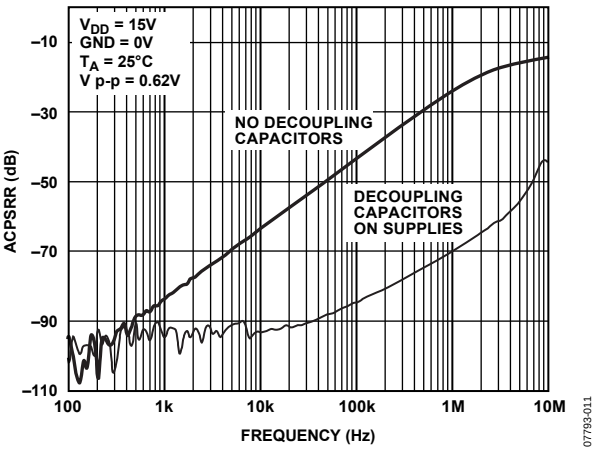

Figure 12. ACPSRR vs. Frequency

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TEST CIRCUITS

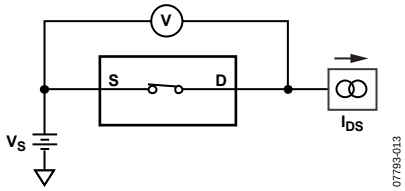

Figure 13. On Resistance

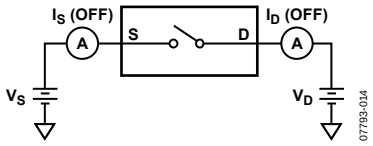

Figure 14. Off Resistance

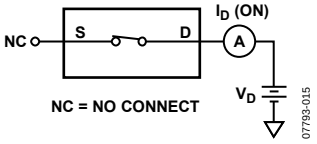

Figure 15. On Leakage

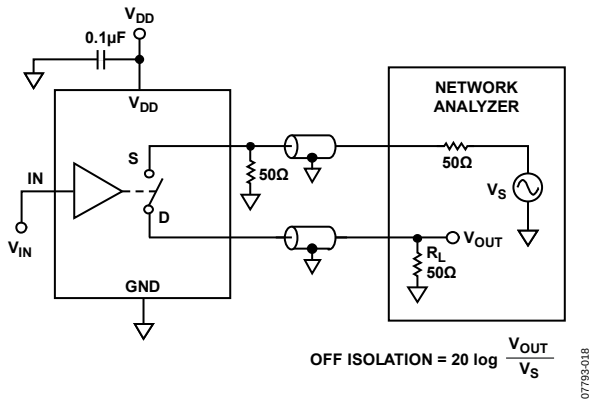

Figure 16. Off Isolation

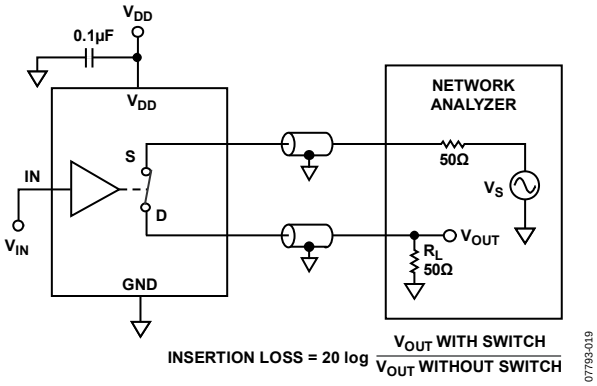

Figure 17. Bandwidth

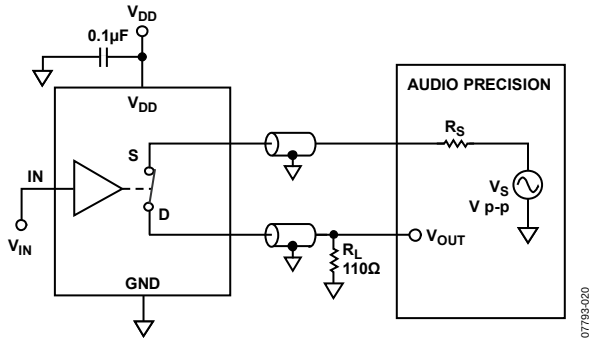

Figure 18. THD + Noise

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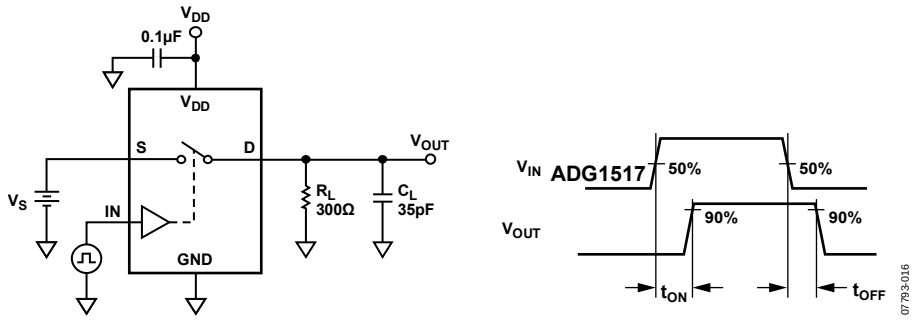

Figure 19. Switching Times

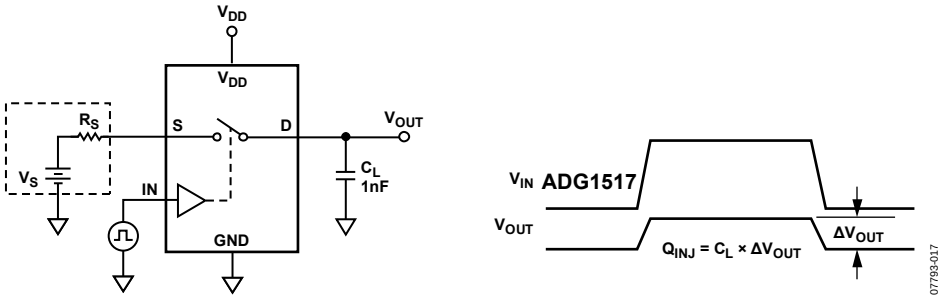

Figure 20. Charge Injection

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TERMINOLOGY

I_{DD}
The positive supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between D and S.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{ON}
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and 90% points of the digital input and switch off condition.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

ACPSRR (AC Power Supply Rejection Ratio)
Measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

OUTLINE DIMENSIONS

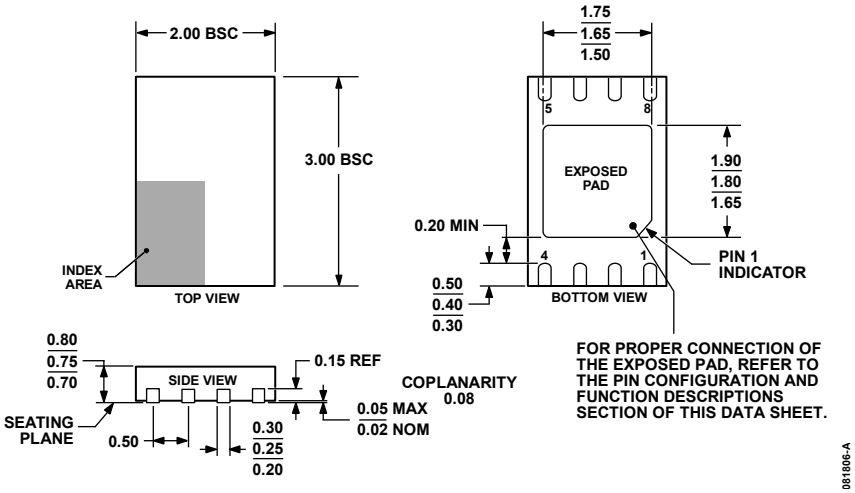

Figure 21. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 2 mm Body, Very Very Thin, Dual Lead
(CP-8-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG1517BCPZ-REEL7[1]	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_WD)	CP-8-4	1E

[1] Z = RoHS Compliant Part.

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NOTES

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