

MC3437

HEX BUS RECEIVER WITH INPUT HYSTERESIS

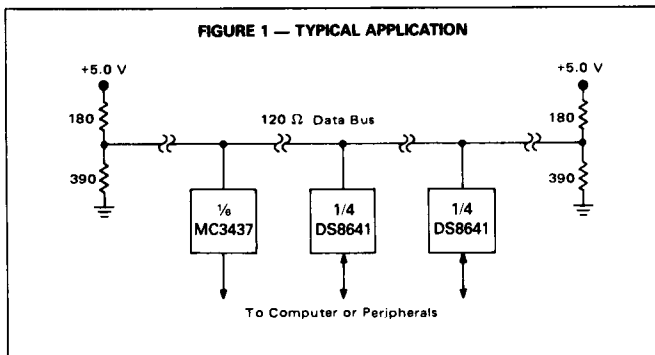
These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time—20 ns (Typ)
- Direct Replacement for DM8837

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

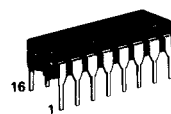
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

FIGURE 1 — TYPICAL APPLICATION

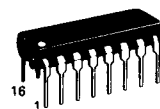


HEX BUS RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

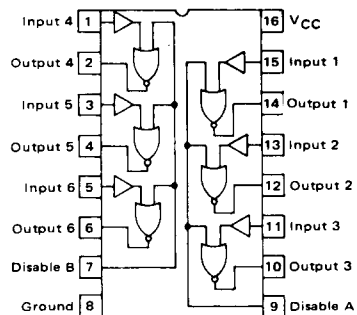


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

Input	Disable	Output
O	L	H
O	H	L
I	L	L
I	H	L

O = < 1.05 V
I = > 2.5 V
H = High Logic State
L = Low Logic State

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leq T_A \leq 70^\circ\text{C}$ and $4.75 \text{ V} \leq V_{CC} \leq 5.25 \text{ V}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Input Threshold Voltage – High Logic State ($V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$, $V_{OL} \leq 0.4 \text{ V}$)	$V_{ILH}(\text{R})$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage – Low Logic State ($V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$, $V_{OH} \geq 2.4 \text{ V}$)	$V_{IHL}(\text{R})$	1.05	1.30	1.55	V
Receiver Input Current ($V_{I(\text{R})} = 4.0 \text{ V}$, $V_{CC} = 5.25 \text{ V}$) ($V_{I(\text{R})} = 4.0 \text{ V}$, $V_{CC} = 0 \text{ V}$)	$I_{I(\text{R})}$	— —	15 1.0	50 50	μA
Disable Input Voltage – High Logic State ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{OL} \leq 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$)	$V_{IH}(\text{DA})$	2.0	—	—	V
Disable Input Voltage – Low Logic State ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{OH} \geq 2.4 \text{ V}$, $I_{OH} = -400 \mu\text{A}$)	$V_{IL}(\text{DA})$	—	—	0.8	V
Output Voltage – High Logic State ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$)	V_{OH}	2.4	—	—	V
Output Voltage – Low Logic State ($V_{I(\text{R})} = 4.0 \text{ V}$, $V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$)	V_{OL}	—	0.25	0.4	V
Disable Input Current – High Logic State ($V_{IH}(\text{DA}) = 2.4 \text{ V}$) ($V_{IH}(\text{DA}) = 5.5 \text{ V}$)	$I_{IH}(\text{DA})$	— —	— —	80 2.0	μA mA
Disable Input Current – Low Logic State ($V_{I(\text{R})} = 4.0 \text{ V}$, $V_{IL}(\text{DA}) = 0.4 \text{ V}$)	$I_{IL}(\text{DA})$	—	—	-3.2	mA
Output Short Circuit Current ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0 \text{ V}$, $V_{CC} = 5.25 \text{ V}$)	I_{OS}	-18	—	-55	mA
Power Supply Current ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0 \text{ V}$)	I_{CC}	—	45	65	mA
Input Clamp Diode Voltage ($I_{I(\text{R})} = -12 \text{ mA}$, $I_{I(\text{DA})} = -12 \text{ mA}$)	V_I	—	-1.0	-1.5	V

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Receiver Input to High Logic State Output	$t_{PLH}(\text{R})$	—	20	30	ns
Propagation Delay Time from Receiver Input to Low Logic State Output	$t_{PHL}(\text{R})$	—	18	30	ns
Propagation Delay Time from Disable Input to High Logic State Output	$t_{PLH}(\text{DA})$	—	9.0	15	ns
Propagation Delay Time from Disable Input to Low Logic State Output	$t_{PHL}(\text{DA})$	—	4.0	15	ns

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FIGURE 2 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

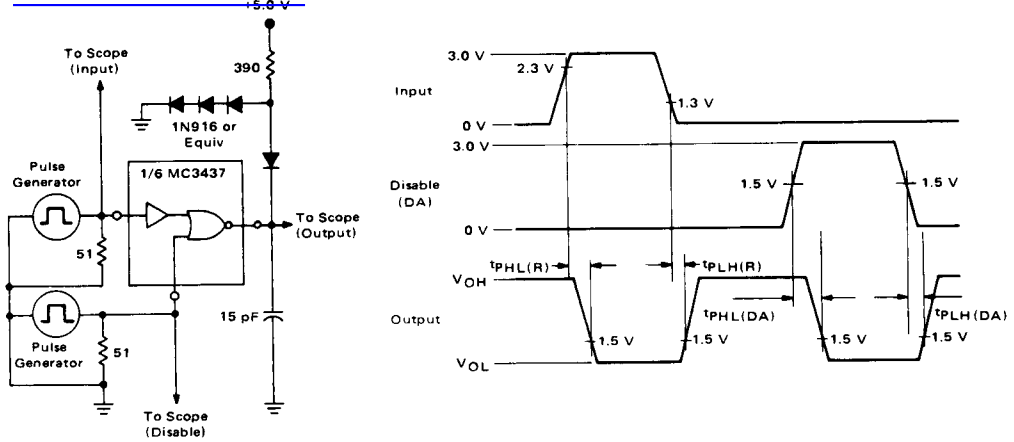


FIGURE 3 — TYPICAL HYSTERESIS

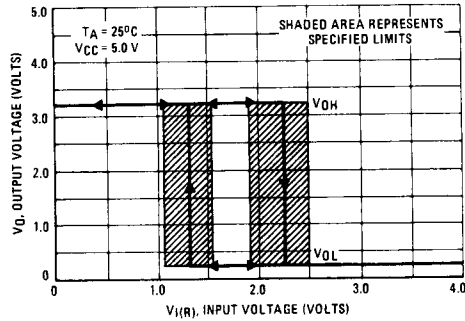


FIGURE 4 — REPRESENTATIVE CIRCUIT SCHEMATIC
(1/6 Shown)

