

**MILITARY DATA SHEET**

**MN100344-X REV 1A0**

Original Creation Date: 10/30/95  
 Last Update Date: 11/01/96  
 Last Major Revision Date: 10/16/96

**LOW POWER 8-BIT LATCH WITH CUT-OFF DRIVERS**

**General Description**

The F100344 contains eight D-type latches, individual inputs (Dn), outputs (Qn), a common enable pin (E), and a latch enable pin (LE), and output enable pin (OEN). A Q output follows its D input when both E and LE are low. When either E or LE (or both) are HIGH, a latch stores the last valid data present on its D input prior to E or LE going HIGH.

A HIGH on OEN holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is -2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loadshare the bus. The F100344 outputs are designed to drive a doubly terminated 50 ohms transmission line (25 ohm load impedance). All inputs have 50K ohm pull-down resistors.

**Industry Part Number**

100344

**NS Part Numbers**

100344DMQB  
 100344FMQB

**Prime Die**

F344

**Processing**

MIL-STD-883, Method 5004

**Quality Conformance Inspection**

MIL-STD-883, Method 5005

**Subgrp Description Temp (°C)**

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55



**Features**

- Cut-off Drivers
- Drive 25 ohm load
- Low Power operation
- 2000V ESD protection
- Voltage compensated operating range= -4.2V to -5.7V
- Available to MIL-STD-883

### **(Absolute Maximum Ratings)**

(Note 1)

Storage Temperature (Tstg)	-65C to +150C
Maximum Junction Temperature (Tj)	
Ceramic	+175C
Plastic	+150C
Vee Pin Potential to Ground Pin	
	-7.0V to +0.5V
Input Voltage (DC)	
	Vee to +0.5V
Output Current (DC Output HIGH)	
	-50 mA
ESD	
(Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

### **Recommended Operating Conditions**

Case Temperature (Tc)	
Commercial	0 C to +85 C
Industrial	-40 C to +85C
Military	-55C to +125C
Supply Voltage (Vee)	
	-5.7V to -4.2V

## Electrical Characteristics

### DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: Vee Range: -4.2V to -5.7V, Tc= -55C to +125C, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	VEE=-5.7V, VM=-0.87V	1, 3	INPUTS		240	uA	1, 2
			1, 3	INPUTS		340	uA	3
IIL	Input Low Current	VEE=-4.2V, VM=-1.83V	1, 3	INPUTS	0.5		uA	1, 2, 3
VOH	Output HIGH Voltage	VEE=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 25 Ohms to -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	VEE=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 25 Ohms to -2.0V, OEN =-1.87V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOL	Output LOW Voltage (cutoff voltage)	VEE=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 25 Ohms to -2.0V, OEN =-0.87V	1, 3	OUTPUTS		-1950	mV	1, 2
			1, 3	OUTPUTS		-1850	mV	3
VOHC	Output HIGH Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, Loading: 25 Ohms to -2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, Loading: 25 Ohms to -2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VIH	Input HIGH Voltage		1, 3, 7	INPUTS	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	INPUTS	-1830	-1475	V	1, 2, 3
IEE	Power Supply Current	VEE=-4.2/-4.8V	1, 3	VEE	-195	-73	mA	1, 2, 3
		VEE=-5.7V	1, 3	VEE	-205	-73	mA	1, 2, 3

## Electrical Characteristics

### AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
 AC: VEE Range: -4.2V to -5.7V, LOADING: 25 Ohms to -2.0V, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH/tpHL(1)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	Dn to Qn	0.7	2.6	ns	9
			2, 4	Dn to Qn	0.7	3.1	ns	10
			2, 4	Dn to Qn	0.5	2.6	ns	11
tpLH/tpHL(2)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	LE/E to Qn	1.0	3.3	ns	9
			2, 4	LE/E to Qn	1.1	3.8	ns	10
			2, 4	LE/E to Qn	0.8	3.3	ns	11
tpLH(3)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	QEN to Qn	1.1	4.2	ns	9
			2, 4	QEN to Qn	1.2	4.4	ns	10
			2, 4	QEN to Qn	1.0	4.6	ns	11
tpHL(3)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	QEN to Qn	0.7	2.8	ns	9
			2, 4	QEN to Qn	0.7	3.2	ns	10
			2, 4	QEN to Qn	0.7	3.0	ns	11
tTLH/tTHL	Transistion Time	VEE=-4.2/-5.7V	6	Qn	0.4	2.4	ns	9
			6	Qn	0.4	2.7	ns	10
			6	Qn	0.4	2.5	ns	11
tS	Setup Time	VEE=-4.2/-5.7V	6	Dn to LE/E	1.7		ns	9
			6	Dn to LE/E	1.5		ns	10, 11
tH	Hold Time	VEE=-4.2/-5.7V	6	Dn to LE/E	0.6		ns	9, 10, 11
tpW(H)	Pulse Width	VEE= -4.2/-5.7V	6	LE/E	2.4		ns	9, 10, 11

- Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.  
 Note 2: Screen tested 100% on each device at +25 C temp only, subgroup A9.  
 Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.  
 Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.

**(Continued)**

Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.

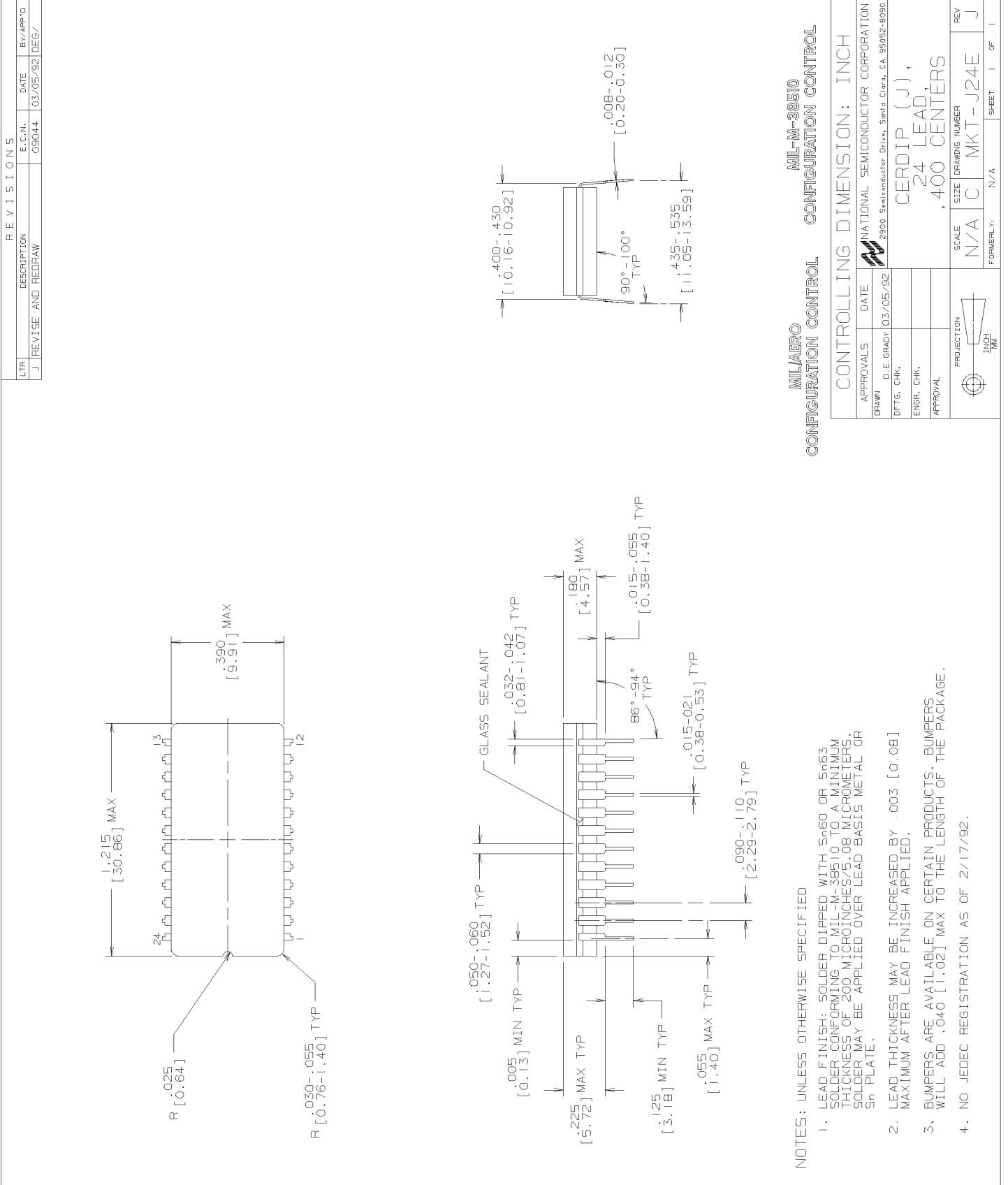
Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).

Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

### Graphics and Diagrams

GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP (J), 24LD .400 CENTERS (P/P DWG)
P000076A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000077A	CERPAC, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPAC, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.



MIL/AERO CONFIGURATION CONTROL		MIL-M-38510 CONFIGURATION CONTROL	
APPROVALS	DATE	CONTROLLING DIMENSION: INCH	
DRAWN D. E. GRADY	03/05/92	NATIONAL SEMICONDUCTOR CORPORATION	
DFTG. CHK.		2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
ENGR. CHK.		CERDIP (J),	
APPROVAL		24 LEAD	
		.400 CENTERS	
PROJECTION	SCALE	SIZE	DRAWING NUMBER
	N/A	C	MKT-J24E
FORMERLY:	N/A	SHEET	1 OF 1