General Description

The MAX7310 provides 8-bit parallel input/output port expansion for SMBus[™]-compatible and I²C[™]-compatible applications. The MAX7310 consists of an input port register, an output port register, a polarity inversion register, a configuration register, a bus timeout register, and an SMBus/I²C-compatible serial interface. The system master can invert the MAX7310 input data by writing to the active-high polarity inversion register. The system master can enable or disable bus timeout by writing to the bus timeout register.

Any of the eight I/O ports may be configured as input or output. An active-low reset input sets the eight I/Os as inputs. Three address select pins configure one of 56 slave ID addresses.

The MAX7310 is available in 16-pin thin QFN, TSSOP, and QSOP packages and is specified over the -40°C to +125°C automotive temperature range.

Applications
Servers
RAID Systems
Industrial Control
Medical Equipment

Instrumentation, Test Measurement

SMBus is a trademark of Intel Corp.

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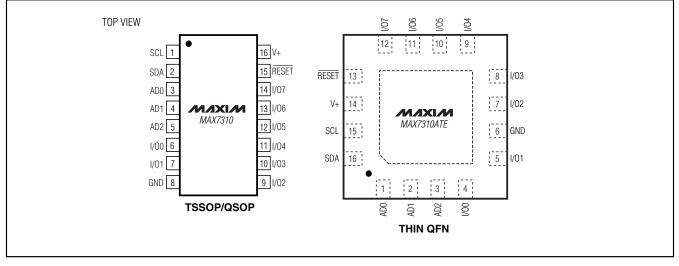
_Features

- ♦ 400kHz 2-Wire Interface
- ♦ 2.3V to 5.5V Operation
- Low Standby Current (1.7µA typ)
- Bus Timeout for Lock-Up-Free Operation
- ♦ 56 Slave ID Addresses
- Polarity Inversion
- Eight I/O Pins that Default to Inputs on Power-Up
- ♦ 5V Tolerant Open-Drain Output on I/O0
- ♦ 4mm x 4mm, 0.8mm Thin QFN Package
- ♦ -40°C to +125°C Operation

Ordering Information

PART	TEMP RANGE	PIN- PACKAGE	PKG CODE
MAX7310AUE	-40°C to +125°C	16 TSSOP	_
MAX7310AEE	-40°C to +125°C	16 QSOP	_
MAX7310ATE	-40°C to +125°C	16 Thin QFN	T1644-4

Pin Configurations



_ Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

6V
SV)
6V
6V
μA
nΑ
nΑ

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

 $(V + = 2.3V \text{ to } 5.5V, \text{GND} = 0, \overline{\text{RESET}} = V +, T_A = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at V + = 3.3V, T_A = +25^{\circ}\text{C}.)$ (Note 1)

PARAMETER	SYMBOL	CONDITIO	ONS	MIN	ТҮР	MAX	UNITS
Supply Voltage	V+			2.3		5.5	V
		All outputs floating,	V+ = 2.3V		19	30	
Supply Current	l+	all inputs at V+ or GND,	V+ = 3.3V		29	40	μA
		$f_{SCL} = 400 \text{kHz}$	V+ = 5.5V		65	80	
		All outputs floating,	V+ = 2.3V		1.5	3.4	
Standby Current		all inputs at V+ or GND,	V+ = 3.3V		1.7	3.9	μA
		$f_{SCL} = 0$	V+ = 5.5V		2.1	5	
Power-On Reset Voltage					1.6	2.1	V
SCL, SDA		•					
Input Voltage Low	VIL					0.8	V
Input Voltage High	VIH			2			V
Low-Level Output Voltage	Voil	I _{SINK} = 6mA				0.4	V
Leakage Current	١L			-1		+1	μA
Input Capacitance	CI				10		pF
I/Os							
Input Voltage Low	VIL					0.8	V
Input Voltage High	VIH			2			V
Input Leakage Current	١L	All inputs at V+ or GND		-1		+1	μA
		$V + = 2.3V, V_{OL} = 0.5V$		8	14		
Low-Level Output Current	IOL	V+ = 3.3V, V _{OL} = 0.5V	12.5	22		mA	
		V+ = 5.5V, V _{OL} = 0.5V		19	30		1
		V+ = 3.3V, V _{OH} = 2.4V		6.5	11		
High Output Current for I/O1–I/O7	ЮН	V+ = 5.5V, V _{OH} = 4.5V		12.5	18		mA
AD0, AD1, AD2, AND RESET							
Input Voltage Low						0.8	V
Input Voltage High				2			V

DC ELECTRICAL CHARACTERISTICS (continued)

 $(V + = 2.3V \text{ to } 5.5V, \text{GND} = 0, \overline{\text{RESET}} = V +, T_A = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}, \text{ unless otherwise noted}. Typical values are at V + = 3.3V, T_A = +25^{\circ}\text{C}.)$ (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
Leakage Current			-1		+1	μA
Input Capacitance				10		pF

AC ELECTRICAL CHARACTERISTICS

(V+ = 2.3V to 5.5V, GND = 0, $\overline{\text{RESET}}$ = V+, T_A = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS
SCL Clock Frequency	fscl	(Note 2)			400	kHz
BUS Timeout	TIMEOUT		30		60	ms
Bus Free Time Between STOP and START Condition	tBUF	Figure 2	1.3			μs
Hold Time (Repeated) START Condition	^t HD, STA	Figure 2	0.6			μs
Repeated START Condition Setup Time	ts∪, sta	Figure 2	0.6			μs
STOP Condition Setup Time	tsu, sто	Figure 2	0.6			μs
Data Hold Time	^t HD, DAT	Figure 2 (Note 3)			0.9	μs
Data Setup Time	tsu, dat	Figure 2	0.1			μs
SCL Low Period	tLOW	Figure 2	1.3			μs
SCL High Period	thigh	Figure 2	0.7			μs
SCL/SDA Fall Time (Transmitting)	tF	Figure 2 (Note 4)			250	ns
Pulse Width of Spike Supressed	tsp	(Note 5)		50		ns
PORT TIMING						
Output Data Valid	t _{PV}	Figure 9			1	μs
Input Data Setup Time	tps	Figure 10	29			μs
Input Data Hold Time	tрн	Figure 10	0			μs
RESET						
Reset Pulse Width			100			ns

Note 1: All parameters are 100% production tested at $T_A = +25^{\circ}C$. Specifications over temperature are guaranteed by design.

Note 2: Minimum SCL clock frequency is limited by the MAX7310 bus timeout feature, which resets the serial bus interface if either SDA or SCL is held low for a 30ms minimum.

Note 3: A master device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

Note 4: t_F measured between 90% to 10% of V+.

Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

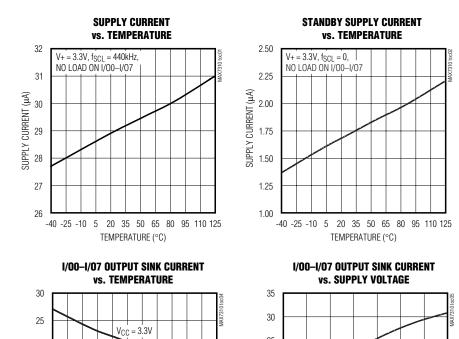
 $(T_A = +25^{\circ}C, unless otherwise noted.)$

 $V_{CC} = 2.3V$

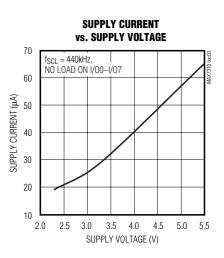
-40 -25 -10 5 20 35 50 65 80 95 110 125

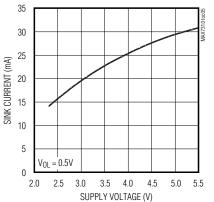
TEMPERATURE (°C)

MAX7310

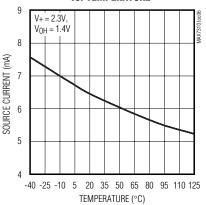


Typical Operating Characteristics





I/01–I/07 OUTPUT SOURCE CURRENT vs. TEMPERATURE



20

15

10

5

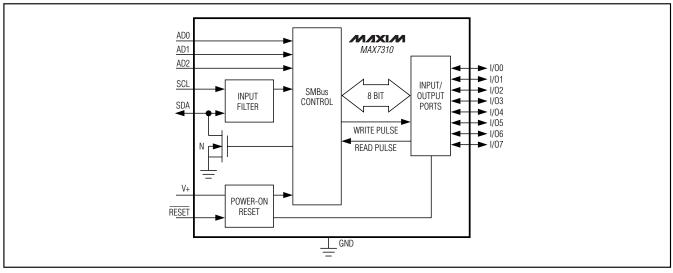
0

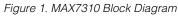
 $V_{0L}=0.5V$

SINK CURRENT (mA)

Pin Description

Р	IN		
TSSOP/ QSOP	THIN QFN	NAME	FUNCTION
1	15	SCL	Serial Clock Line
2	16	SDA	Serial Data Line
3	1	AD0	Address Input 0
4	2	AD1	Address Input 1
5	3	AD2	Address Input 2
6	4	I/O0	Input/Output Port 0 (Open Drain)
7	5	I/O1	Input/Output Port 1
8	6	GND	Supply Ground
9–14	7–12	1/02–1/07	Input/Output Port 2—Input/Output Port 7
15	13	RESET	External Reset (Active Low). Pull RESET low to configure I/O pins as inputs. Set RESET high for normal operation.
16	14	V+	Supply Voltage. Bypass with a 0.047µF capacitor to GND.
_	PAD	Exposed pad	Exposed Pad on Package Underside. Connect to GND.





Detailed Description

The MAX7310 general-purpose input/output (GPIO) peripheral provides up to eight I/O ports, controlled through an I²C-compatible serial interface. The MAX7310 consists of an input port register, an output

port register, a polarity inversion register, a configuration register, and a bus timeout register. An active-low reset input sets the eight I/O lines as inputs. Three slave ID address select pins (AD0, AD1, and AD2) choose one of 56 slave ID addresses (Figure 1).



Table 1 is the register address table. Tables 2–6 list register 0 through register 4 information.

Serial Interface

Serial Addressing

The MAX7310 operates as a slave that sends and receives data through a 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to and from the MAX7310, and generates the SCL clock that synchronizes the data transfer (Figure 2).

Each transmission consists of a start condition sent by a master, followed by the MAX7310 7-bit slave address plus an R/W bit, a register address byte, one or more data bytes, and finally a stop condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a start (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a stop (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit, which the recipient uses as a handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7310, the MAX7310 generates the acknowledge bit since the MAX7310 is the recipient. When the MAX7310 is transmitting to the master generates the acknowledge bit.

Slave Address

The MAX7310 has a 7-bit-long slave address (Figure 6). The 8th bit following the 7-bit slave address is the R/W bit. Set this bit low for a write command and high for a read command.

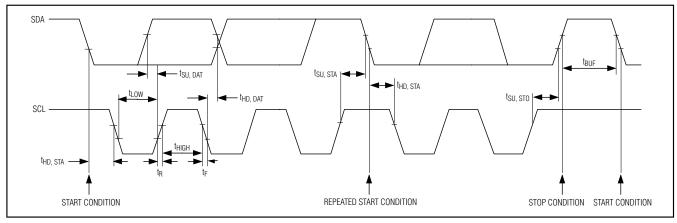


Figure 2. 2-Wire Serial Interface Timing Diagrams

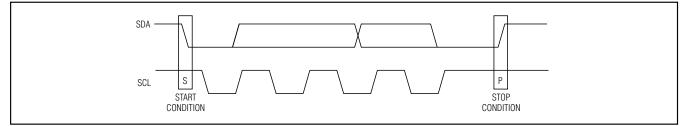


Figure 3. Start and Stop Conditions

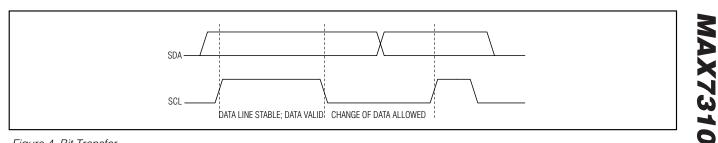


Figure 4. Bit Transfer

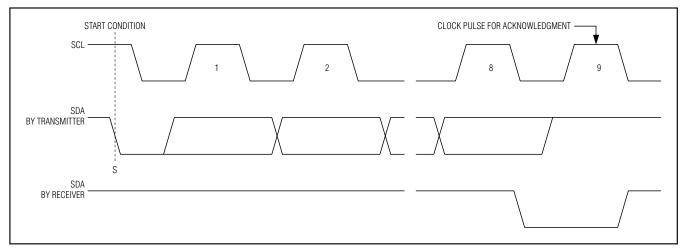


Figure 5. Acknowledge

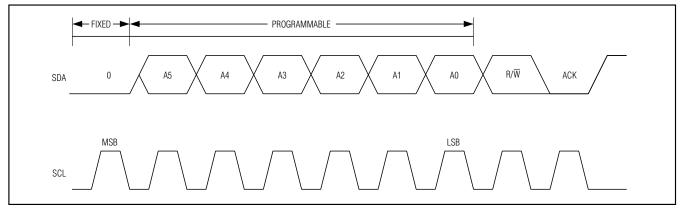


Figure 6. Slave Address

The first bits (MSBs) of the MAX7310 slave address are always zero. Slave address bits AD2, AD1, and AD0 choose 1 of 56 slave ID addresses (Table 7).

Registers

The register address byte is the first byte to follow the address byte during a read/write transmission. The reg-

ister address byte acts as a pointer to determine which register is written or read.

The input port register is a read-only port. It reflects the incoming logic levels of the I/O ports, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.



Table 1. Register Address

MAX7310

REGISTER ADDRESS (hex)	FUNCTION	PROTOCOL
0x00	Input port register	Read byte.
0x01	Output port register	Read/write byte.
0x02	Polarity inversion register	Read/write byte.
0x03	Configuration register	Read/write byte.
0x04	Timeout register	Read/write byte.
0xFF	Reserved register	Factory reserved. Do not write to this register.

Table 2. Register 0—Input Port Register

BIT	17	16	15	14	13	12	11	10
-----	----	----	----	----	----	----	----	----

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Reads from the output port register reflect the value that is in the flip-flop controlling the output selection, not the actual I/O value, which may differ if the output is overloaded.

The polarity inversion register enables polarity inversion of ports defined as inputs by the configuration register. Set the bit in the polarity inversion register (write with a 1) to invert the corresponding port pin's polarity. Clear the bit in the polarity inversion register (write with a zero) to retain the corresponding port pin's original polarity.

The configuration register configures the directions of the ports. Set the bit in the configuration register to enable the corresponding port pin as an input with a high-impedance output driver. Clear the bit in the configuration register to enable the corresponding port pin as an output.

Set bit T0 to enable the bus timeout function and low to disable the bus timeout function. Enabling the timeout feature resets the serial bus interface when SCL stops either high or low during a read or write access to the MAX7310. If either SCL or SDA is low for more than 30ms min and 60ms max after the start of a valid serial transfer, the interface resets itself. Resetting the serial bus interface sets up SDA as an input. The MAX7310 then waits for another start condition.

Standby

The MAX7310 goes into standby when all pins are set to V+ or GND. Standby supply current is typically 1.7μ A.

Table 3. Register 1—Output Port Register

BIT	07	O6	O5	04	O3	02	01	00
Default	0	0	0	0	0	0	0	0

Table 4. Register 2—Polarity Inversion Register

BIT	I/07	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Default	1	1	1	1	0	0	0	0

Table 5. Register 3—Configuration Register

BIT	I/07	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Default	1	1	1	1	1	1	1	1

Table 6. Register 4—Timeout Register

BIT	T7	Т6	T5	T4	Т3	T2	T1	Т0
Default	Х	х	х	х	х	х	х	1

8

Table 7. MAX7310 Address Map

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0
GND	SCL	GND	0	0	0	1	0	0	0
GND	SCL	V+	0	0	0	1	0	0	1
GND	SDA	GND	0	0	0	1	0	1	0
GND	SDA	V+	0	0	0	1	0	1	1
V+	SCL	GND	0	0	0	1	1	0	0
V+	SCL	V+	0	0	0	1	1	0	1
V+	SDA	GND	0	0	0	1	1	1	0
V+	SDA	V+	0	0	0	1	1	1	1
GND	GND	SCL	0	0	1	0	0	0	0
GND	GND	SDA	0	0	1	0	0	0	1
GND	V+	SCL	0	0	1	0	0	1	0
GND	V+	SDA	0	0	1	0	0	1	1
V+	GND	SCL	0	0	1	0	1	0	0
V+	GND	SDA	0	0	1	0	1	0	1
V+	V+	SCL	0	0	1	0	1	1	0
V+	V+	SDA	0	0	1	0	1	1	1
GND	GND	GND	0	0	1	1	0	0	0
GND	GND	V+	0	0	1	1	0	0	1
GND	V+	GND	0	0	1	1	0	1	0
GND	V+	V+	0	0	1	1	0	1	1
V+	GND	GND	0	0	1	1	1	0	0
V+	GND	V+	0	0	1	1	1	0	1
V+	V+	GND	0	0	1	1	1	1	0
V+	V+	V+	0	0	1	1	1	1	1
SCL	SCL	SCL	0	1	0	0	0	0	0
SCL	SCL	SDA	0	1	0	0	0	0	1
SCL	SDA	SCL	0	1	0	0	0	1	0
SCL	SDA	SDA	0	1	0	0	0	1	1
SDA	SCL	SCL	0	1	0	0	1	0	0
SDA	SCL	SDA	0	1	0	0	1	0	1
SDA	SDA	SCL	0	1	0	0	1	1	0
SDA	SDA	SDA	0	1	0	0	1	1	1
SCL	SCL	GND	0	1	0	1	0	0	0
SCL	SCL	V+	0	1	0	1	0	0	1
SCL	SDA	GND	0	1	0	1	0	1	0
SCL	SDA	V+	0	1	0	1	0	1	1
SDA	SCL	GND	0	1	0	1	1	0	0
SDA	SCL	V+	0	1	0	1	1	0	1
SDA	SDA	GND	0	1	0	1	1	1	0
SDA	SDA	V+	0	1	0	1	1	1	1

MAX7310

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0
SCL	GND	SCL	0	1	1	0	0	0	0
SCL	GND	SDA	0	1	1	0	0	0	1
SCL	V+	SCL	0	1	1	0	0	1	0
SCL	V+	SDA	0	1	1	0	0	1	1
SDA	GND	SCL	0	1	1	0	1	0	0
SDA	GND	SDA	0	1	1	0	1	0	1
SDA	V+	SCL	0	1	1	0	1	1	0
SDA	V+	SDA	0	1	1	0	1	1	1
SCL	GND	GND	0	1	1	1	0	0	0
SCL	GND	V+	0	1	1	1	0	0	1
SCL	V+	GND	0	1	1	1	0	1	0
SCL	V+	V+	0	1	1	1	0	1	1
SDA	GND	GND	0	1	1	1	1	0	0
SDA	GND	V+	0	1	1	1	1	0	1
SDA	V+	GND	0	1	1	1	1	1	0
SDA	V+	V+	0	1	1	1	1	1	1

Table 7. MAX7310 Address Map (continued)

Applications Information

Chip Information

Power-Supply Consideration

The MAX7310 operates from a supply voltage of 2.3V to 5.5V. Bypass the power supply to GND with a 0.047 μ F capacitor as close to the device as possible. For the QFN version, connect the underside exposed pad to GND.

TRANSISTOR COUNT: 10,256 PROCESS: BICMOS

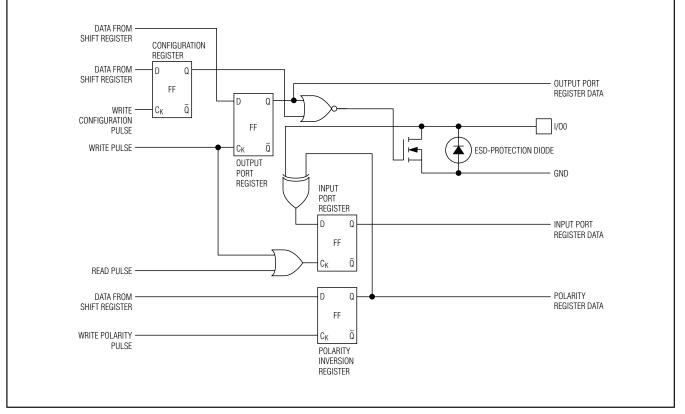


Figure 7. Simplified Schematic of I/O0

MAX7310

MAX7310

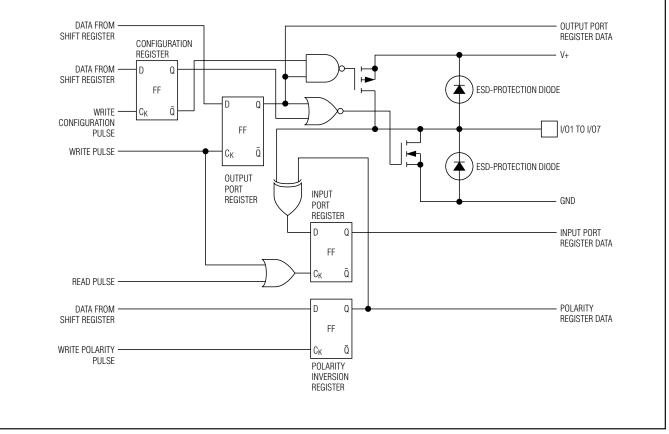


Figure 8. Simplified Schematic of I/O1–I/O7

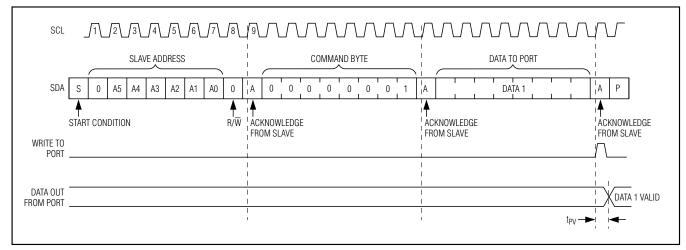


Figure 9. Write to Output Port Register Through Write-Byte Protocol

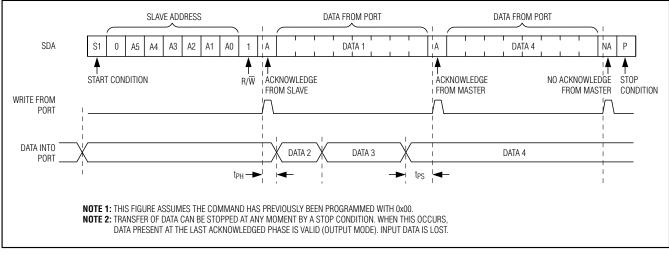
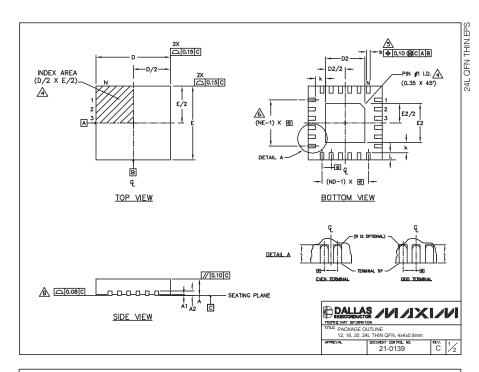


Figure 10. Read Input Port Register Through Receive-Byte Protocol

Package Information

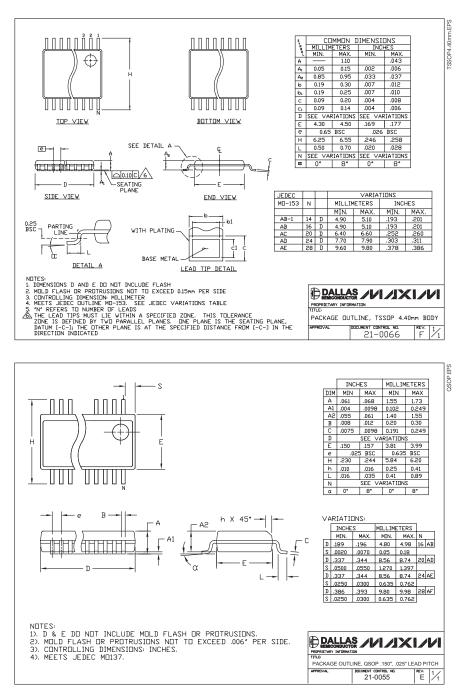
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



REF. HDN. NDH. HAX. MIN. NDR. MAX. MIN. <th< th=""><th></th><th></th><th></th><th>1</th><th></th><th>10N</th><th>DIME</th><th>INSI</th><th>SNE</th><th></th><th></th><th></th><th></th><th></th><th>E</th><th>XPDS</th><th>ED</th><th>PAD</th><th>VAR</th><th>ITAI</th><th>ONS</th><th></th></th<>				1		10N	DIME	INSI	SNE						E	XPDS	ED	PAD	VAR	ITAI	ONS	
EFr. IDN. NDK MAX. NIN. NDK. MAX. NIN. NDK. MAX. MIX. MIX. NDK. MAX. MIX.	PKG	12	2L 4×	4	16	5L 4×	4	20	IL 4×	4	2	4L 4×	(4		PVC		D2			£2		
AL 0.0 0.02 0.0 0.02 0.0 0.02 0.0 <th< td=""><td>REF.</td><td>MIN,</td><td>NDM.</td><td>MAX.</td><td>MIN</td><td>NDM.</td><td>NAX.</td><td>MIN.</td><td>NDM.</td><td>MAX.</td><td>MIN.</td><td>NDM.</td><td>MAX.</td><td></td><td>CODES</td><td>MIN.</td><td>NDM.</td><td>MAX.</td><td>MIN.</td><td>NDM.</td><td>MAX.</td><td>ALLOVEI</td></th<>	REF.	MIN,	NDM.	MAX.	MIN	NDM.	NAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.		CODES	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	ALLOVEI
R2 0.20 REF 0.20 0.20 0.21 0.20 0.21 0.20 0.21 0.20 0.225 0.21 0.225 0.21 0.225 0.21 0.225 0.25 0.01 0.25 ND 10 0.450 0.50 0.50 0.55 0.55	A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80		T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	ND
b 0.25 0.30 0.35 0.25 0.30 0.25 0.30 0.25 0.30 0.25 0.30 0.21 0.22 0.30 0.31 0.23 0.30 0.30 10 0.33 0.40 4.10 3.30 4.00 4.10 4.30 5.30 0.30 0.30 0.10 1.10 1.10 1.21 1.10 2.25 1.01 2.25 ND N N 3 4 5 <t< td=""><td>A1</td><td>0.0</td><td>0.02</td><td>0.05</td><td>0.0</td><td>0.02</td><td>0.05</td><td>0.0</td><td>20.0</td><td>0.05</td><td>0.0</td><td>0.02</td><td>0.05</td><td></td><td>T1244-3</td><td>1.95</td><td>2.10</td><td>2,25</td><td>1.95</td><td>2.10</td><td>2.25</td><td>YES</td></t<>	A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	20.0	0.05	0.0	0.02	0.05		T1244-3	1.95	2.10	2,25	1.95	2.10	2.25	YES
0 3.30 4.00 4.00 3.30 4.00 4.10 3.30 4.00 4.10 E 3.30 4.00 4.00 3.30 4.00 4.10 3.30 4.00 4.10 e 0.00 BSC. 0.05 BSC. 0.05 BSC. 0.05 BSC. 0.00 1.01 1.03 3.00 4.00 4.10 k 0.23 - - 0.23 - - 0.25 BSC. 0.50 BS	A2	0	.20 RE	F	0	.20 RE	F	0.	20 RE	F	0	.20 RE	F		T1244-4	1.95	2.10	2,25	1.95	2.10	2.25	ND
0 0.00 0.00 0.00 1.00 <t< td=""><td>ю</td><td>0.25</td><td>0.30</td><td>0.35</td><td>0.25</td><td>0.30</td><td>0.35</td><td>0.20</td><td>0.25</td><td>0.30</td><td>0.18</td><td>0.23</td><td>0.30</td><td></td><td>T1644-2</td><td>1.95</td><td>2.10</td><td>2,25</td><td>1.95</td><td>2.10</td><td>2.25</td><td>ND</td></t<>	ю	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30		T1644-2	1.95	2.10	2,25	1.95	2.10	2.25	ND
Image: Construct of the construction of the	D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10		T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
Image: Notes: Image: Notes:<	£	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3,90	4.00	4.10		T1644-4	1.95	2.10	2,25	1.95	2.10	2.25	ND
L 0.43 0.33 0.45 0.33 0.45 0.33 0.46 0.50 N 12 16 20 24 172 1	e	0	28 08.	č	0.	65 BS	c.	0	50 BS	с.	0	.50 BS	i.		T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	ND
N 12 16 20 24 N1 12 16 20 24 N1 3 4 5 6 Medeo VGGB VGGC VGGD-1 VGGD-2 NOTES: 10 DE24 15 2.00 2.25 1.55 2.10 2.25 VGC VGGD-1 NOTES: 1 DEMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2 2.41 2.45 2.60 2.63 2.45 2.60 2.63 ND 1 DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2 ALL DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2 ALL DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES. 3 N I IT ETEMINAL #1 DEGREES. 3. N IS THE TOTAL. NUMBER OF TERMINAL MOMBERING CONVENTION SHALL CONFORM TO TOTAL DETHING MAY DEBUTHER ARE OFTONALL BUT MUST BE LOCATD WITHIN THE ZONE INCOLTAGE AND TERMINAL #1 DEDRIFIER AND ERO MOL OF MARKED FATURE. A THE TERMINAL #1 DEDRIFIER MAY DEBUTHER AND TERMINAL MOL OF MARKED FATURE. DEDRIFTER MAY DEBUTHER AND TERMINAL MO	ĸ	0.25	-		0.25	-	-		-	-	0.25	-	-		T2044-2	1.95	2.10	2,25	1.95	2.10	2.25	YES
ND 3 4 3 6 NE 3 4 3 6 NE 3 4 5 6 NE 3 4 5 6 VGGB VGGB VGGC VGGD-1 VGGD-2 NOTES: 1 DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2. ALL DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2.4.2 2.4.2 2.60 2.63 2.45 2.60 2.63 ND NOTES: 1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES. NI 1 DIMENSION JOINER AND TERMINAL SIME CONFORM TO ASME Y14.5M-1994. 3. N IS THE TOTAL NUMBER OF TERMINAL MIMBERING CONFERITION SHALL CONFORM TO TO TO DETERMINAL FUNCTION INFORMANCE JUNCTION INFORMATION INFORMANCE JUNCTION SHALL CONFORM TO MILLION TO MILLION TO ADD TERMINAL JUNCTON INFORMANCE JUNCTION SHALL CONFORM TO ADD ON THE MILLION TO THE MILLION TO DETERMINAL JUNCTON IN BOOSTICE AND THE MAND REPORT TO ADD O.30 mm RROW TERMINAL JUNCTION IN SPOSIBLE IN A SYMMETRICAL FASHION. 3. DIMENSION & APPLIES TO THE MARDER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY. DEMENSION & APPLIES TO THE EXPOSED HAT SINK SLUG AS WELL AS THE TERMINALS. 4. COPLINANATITY APPLIES TO THE EXPOSED HAT SINK SLUG AS WELL AS THE TERM	L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50		T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	ND
NOTES: 1. DME minute 3 4 3 6 NOTES: 1. DMENSIONING & TOLERANDING CONFORM TO ASME Y14.5M-1994. 2.43 2.43 2.60 2.63 2.45 2.60 2.63 NT NOTES: 1. DMENSIONING & TOLERANDING CONFORM TO ASME Y14.5M-1994. 2. ALL DMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES. 3. N IS THE TOTAL NUMBER OF TERMINAL. AM DEGREES. 4. THE TERMINAL #1 IDENTIFIER AND DETRIMINAL SMEETING. CONFORM TO MIST BE LIDCATED WITHIN THE ZONE NOICATED. THE TERMINAL #1 DENTIFIER ARE OFTOMAL, BLU TUST BE LIDCATED WITHIN THE ZONE NOICATED. THE TERMINAL #1 DENTIFIER ARE OFTOMAL, BLU TUST BE LIDCATED TO MAND 0.30 mm M THE TERMINAL #1 DENTIFIER AND TERMINAL SON EACH D AND E SIDE RESPECTIVELY. 7. DEOPOPULATION IS POSSIBLE IN A SYMMETRICIAL FASHION. M DAND NE REFER TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. 9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4. THE DOPULATION IS POSSIBLE IN A SYMMETRICIAL FASHION. M OPPOPULATION IS POSSIBLE IN A SYMMETRICIAL FASHION. M M M AND NE REFER TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. M	N		12			16			20			24			T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	ND
OPERATION VGGB VGGC VGGD-1 VGGD-2 T2744-4 2.45 2.60 2.63 2.45 2.60 2.63 ND 1. DMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2. ALL DIMENSIONISG & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2. ALL DIMENSIONISG & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2. ALL DIMENSIONISG & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES. 3. N IS THE TOTAL INVIBER OF TERMINAL SUBJECTIVE ARE OFTONAL BUT MUST BE LOCATED WITHIN THE ZORE NUCLECAED OFTER MUNAL SUT MUST BE LOCATED WITHIN THE ZORE NUCLECAED UT TERMINAL \$10 DETINETER MAY ENTRE MARE OFTONAL BUT MUST BE LOCATED WITHIN THE ZORE NUCLECAED UT TERMINAL \$10 DETINETER MAY ENTRE MARE DETINED OR MARED DETINE NUCLECAED UT THE NUMBER OF TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TP. M DAND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY. TOE PROPULATION IS POSSIBLE IN A SYMMETRICAL FASHION. M DOW TERMINAL TRP. COPPOLATION IS POSSIBLE IN A SYMMETRICAL FASHION. TOE PROPULATION IS POSSIBLE IN A SYMMETRICAL FASHION. M DAND NE REFER TO THE NUMBER OF TERMINALS AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TO JEDUCED HEAT SINK SLUG AS WELL AS THE TERMINALS. TOE PROPULATION IS POSSIBLE IN A SYMMETRICAL FASHION. TOE PROPULATION IS POSSIBLE IN A SYMMETRICAL FASHION. M DRAW	ND		3			4			5			6			T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
NOTES: 1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. 2. ALL DIMENSIONS ARE IN MILLIMETERS. ANALES ARE IN DEGREES. 3. N IS THE TOTAL NUMBER OF TERMINAL, MUMBERING CONVENTION SHALL CONFORM TO MED 95-1 SPP-012. DETALS OF TERMINAL & DISMIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZORN INCLATED. THE TERMINAL & DISTIFIER MAY BE ETHER A NOLD OF MARKED FATURE. 5. DIMENSION & APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP. 5. DOMENSION & APPLIES TO METALLIZED TERMINALS ON EACH D AND E SIDE RESPECTIVELY. 7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION. 6. COPUNARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. 9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.						4			5			6			T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994. ALL DIMENSIONS ARE IN MILLIMETERS. ANALES ARE IN DEGREES. N IS THE TOTAL NUMBER OF TERMINAL. ALL DIMENSIONS ARE IN MILLIMETERS. ANALES ARE IN DEGREES. THE TERMINAL #1 IDENTIFIER AND TERMINAL #1 IDENTIFIER ARE OFTONAL, BUT MUSS BE LOCATED WITHIN JESD 35-1 SPF-012. DETALS OF TERMINAL #1 IDENTIFIER AND COMPONENTION JESD 35-1 SPF-012. DETALS OF TERMINAL #1 IDENTIFIER AND COMPONENTION SYMLL CONFORM TO JESD 35-1 SPF-012. DETALS OF TERMINAL #1 IDENTIFIER AND COMPONENT TO THE ZONE NOTANIES BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER AND COMPONENT TO THE ZONE INDICATED. ALL DENTIFIER AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP. ADA ND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. DRAWING CONFORMS TO JEDEC M0220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4. THE DOPOLUTIONE 12, 16, 20, 24L THIN OFN. 4440.8mm THOUR TERMINAL	Ver.		WGGB			WGGC		۱ ۱	/GGD-:	1		WGGD-	-2		T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	ND
FROM TERNINAL TIP. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY. 7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION. 6. COPLUNARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. 9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4. 10. LOCAL THIN OFM. 4x4x0.8mm AMB/OL TO THE PLANE TO THE LIPPORT	NOTES																					
12, 16, 20, 24L THIN QFN, 4X400.8mm APPROVAL TOCKENT TAXING. NO. PEV.	1. D 2. A 3. N 4. T J	IMENSIO IL DIME I IS THE HE TERI ESD 95- HE ZON	insions total Ninal J -1 SPF E Indik	ARE NUME 1 IDEI -012. CATED.	in Milli Ber of Ntifier Detail The T	imeter Termi And 1 S of 1 Ermina	ts. And Nals. Terminy Ermina L #1 II	ales af Al Num L #1 II Dentifi	re in Ibering Dentifi Er may	degree G Conv Er Are Y Be E	es. /Ention Optic Ither	NAL, B A MOLI	UT MUS D OR N	arke	LOCATED WITH D FEATURE,							
	1. D 2. A 3. N 4. T 5. D F N 7. D 6. N 7. D	IMENSIG ILL DIME I IS THE ESD 95- ESD 95- HE ZON IMENSIG ROM TE ID AND EPOPUL COPLANA	Ensions Total 1 SPF E INDK IN 6 AF RMINAL NE RE ATION RITY AF	ARE I NUNE - NUNE - 012. CATED. PPLIES TIP. FER TO IS POS PPLIES	In Mill Ber of Detail The te To me Shell Shelle To the	Limeter Termi S of T Erminai Tallizi NUMBEI IN A S	IS, ANC NALS, IERMIN ERMINA L #1 II ED TER R OF T YMMETI DSED H	GLES AF AL NUM L #1 II DENTIFII MINAL FERMINA RICAL F	RE IN I DENTIFIER MAY AND IS LIS ON ASHION	DEGREE G CONV ER ARE Y BE E G MEAS EACH N. UG AS	es. (Ention Optic Ither Ured D Ani Well	NAL, B A MOLI BETWEE D E SIG AS THE	UT MUS D OR N D O.25 DE RES E TERMI	ST BE MARKE mm PECTIV NALS.	LOCATED WITH ED FEATURE. AND 0.30 m VELY.		RIETARY I	NFORMATIC	IN	И	/1>	<i <="" td=""></i>
	1. D 2. A 3. N 4. T 5. D F N 7. D 6. N 7. D	IMENSIG ILL DIME I IS THE ESD 95- ESD 95- HE ZON IMENSIG ROM TE ID AND EPOPUL COPLANA	Ensions Total 1 SPF E INDK IN 6 AF RMINAL NE RE ATION RITY AF	ARE I NUNE - NUNE - 012. CATED. PPLIES TIP. FER TO IS POS PPLIES	In Mill Ber of Detail The te To me Shell Shelle To the	Limeter Termi S of T Erminai Tallizi NUMBEI IN A S	IS, ANC NALS, IERMIN ERMINA L #1 II ED TER R OF T YMMETI DSED H	GLES AF AL NUM L #1 II DENTIFII MINAL FERMINA RICAL F	RE IN I DENTIFIER MAY AND IS LIS ON ASHION	DEGREE G CONV ER ARE Y BE E G MEAS EACH N. UG AS	es. (Ention Optic Ither Ured D Ani Well	NAL, B A MOLI BETWEE D E SIG AS THE	UT MUS D OR N D O.25 DE RES E TERMI	ST BE MARKE mm PECTIV NALS.	LOCATED WITH ED FEATURE. AND 0.30 m VELY.		PACK 12, 16	NFORMATIC AGE OU , 20, 241	ITLINE . THIN G	QFN, 4x4	x0.8mm	1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information. go to www.maxim-ic.com/packages.)



MAX731

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