Oki, Network Solutions for a Global Society

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OKI Semiconductor

ML2240

4-Channel Mixing Oki ADPCM Algorithm-Based Speech Synthesis LSI

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

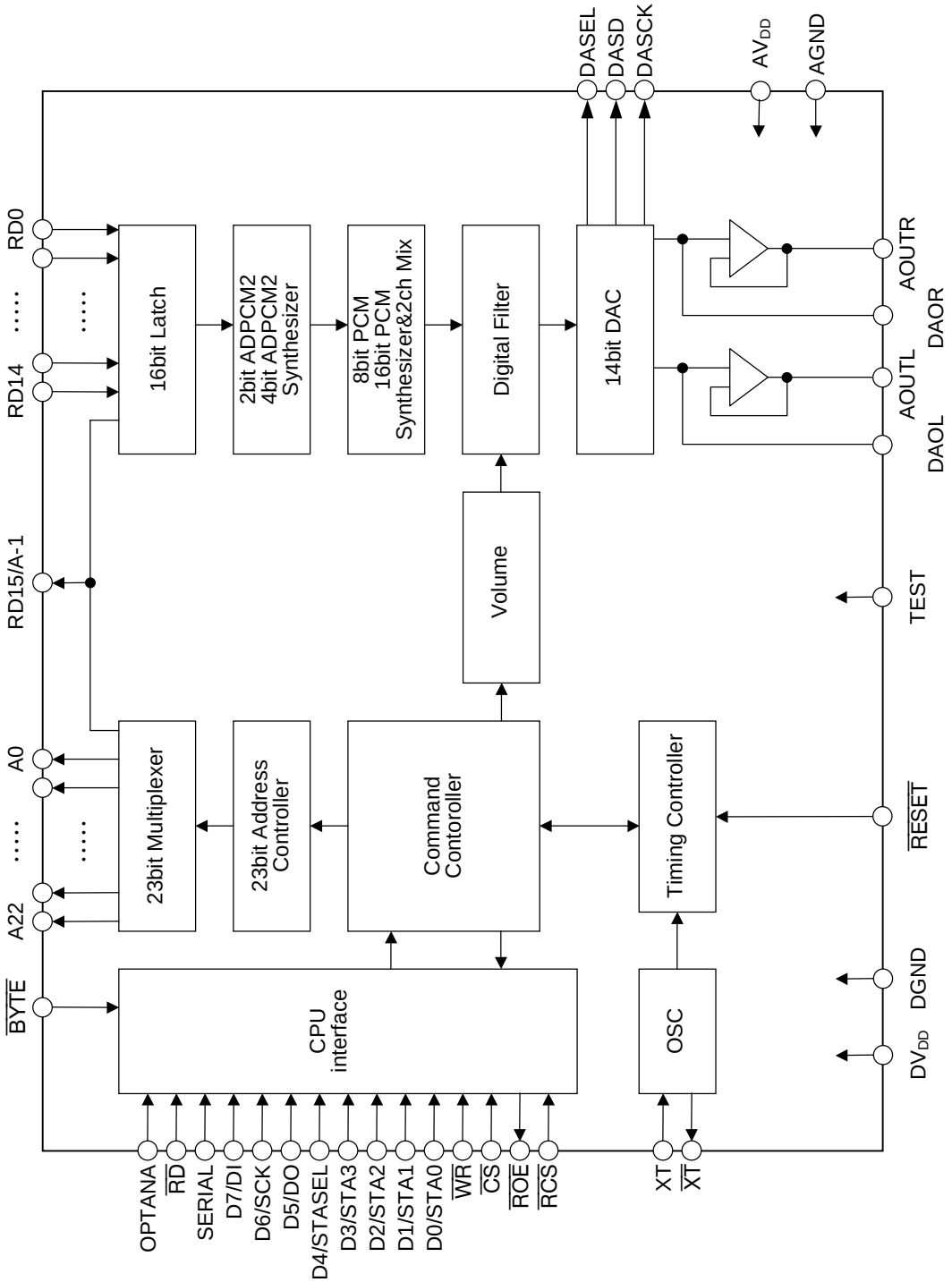
GENERAL DESCRIPTION

The ML2240 is a 4-channel mixing speech synthesis device which connects an external ROM expanded up to 128-Mbit (maximum). This ML2240 allows to select the playback method from the 8-bit PCM, non-linear 8-bit PCM, 16-bit PCM, 2-bit ADPCM2, and 4-bit ADPCM2 algorithms. And the sound volume is adjustable as well. The ML2240 incorporates a 14-bit D/A converter, and low-pass filter.
It is easy to configure a speech synthesizer by externally connecting a power amplifier and a CPU to the ML2240.

FEATURES

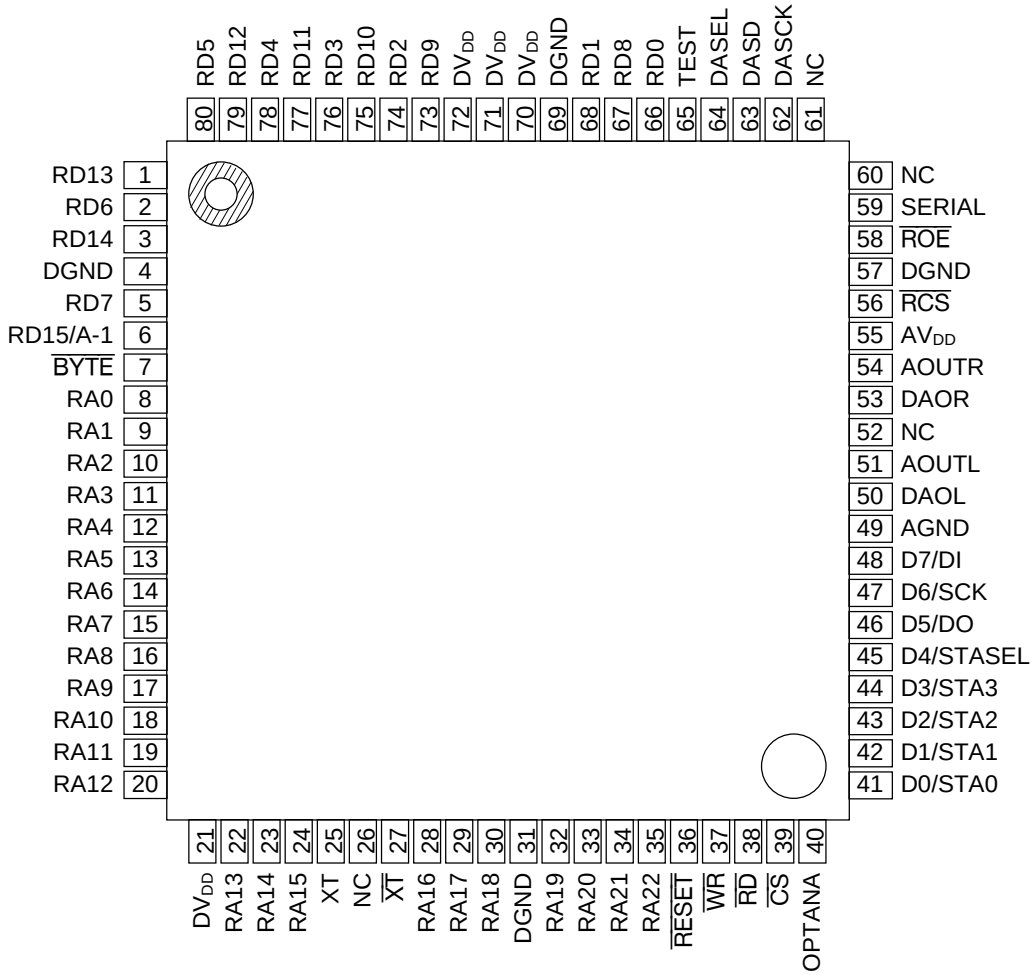
- Non-linear 8-bit PCM, 8-bit PCM, 16-bit PCM, 2-bit ADPCM2, and 4-bit ADPCM2 algorithms
- Serial input/parallel input selectable
- Phrase control table function i.e., user definable phrase control table function
- 4 channels mixing function
- Master clock frequency: 4.096 MHz
- Sampling frequency: 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 21.3 kHz, 25.6 kHz, 32.0 kHz, 42.7 kHz, 48 kHz
- Maximum number of phrases: 256 phrases
- Sound volume adjustment function built in (4 sounds independently adjustable in 29 steps)
- External voice data can be input
- 14-bit D/A converter built in
- Built-in low-pass filter: Digital filter
- Package: 80-pin plastic TQFP (TQFP80-P-1212-0.50-K) (ML2240TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

80-pin plastic TQFP



NC: No Connection

PIN DESCRIPTIONS

80-pin Plastic TQFP

Pin	Symbol	Type	Description
1-3, 5, 66-68, 73-80	RD14-RD0	I	Data pins to connect an external memory. Data is input when the $\overline{ROE}$ pin is at "L" level. Input data from outside is not accepted when the $\overline{ROE}$ pin is at "H" level. The RD14-RD8 pins do not accept input data from outside when the $\overline{BYTE}$ pin is at "L" level.
6	RD15/A-1	I/O	Data pin of the externally connected memory when $\overline{BYTE}$ pin is at "H" level. The data is input when the $\overline{ROE}$ pin output is at "L" level. When the $\overline{ROE}$ pin output is at "H" level, input data from outside is not accepted. This pin becomes an address A-1 output pin when the device is in byte mode. The address is output when the $\overline{RCS}$ pin is at "L" level. When the $\overline{RCS}$ pin is at "H" level, this pin is in a high impedance state.
7	$\overline{BYTE}$	I	Word/byte switching pin of the externally connected memory. When $\overline{BYTE}$ pin = "L" level: Byte mode When $\overline{BYTE}$ pin = "H" level: Word mode
8-20, 22-24, 28-30, 32-35	RA22-RA0	O	Address pins of an externally connected memory. When $\overline{RCS}$ pin = "H": High impedance
25	XT	I	Wired to a crystal or ceramic oscillator. Contains a feedback resistor of around 1 MΩ between this XT pin and $\overline{XT}$ pin (pin 27). When using an external clock, input the clock from this pin.
27	$\overline{XT}$	O	Wired to a crystal or ceramic oscillator. When using an external clock, keep this pin open.
36	$\overline{RESET}$	I	When "L" level is input to this pin, the device is reset to the initial state. The oscillation stops, and AOUT output goes into "GND" level.
37	$\overline{WR}$	I	CPU interface write signal. When $\overline{CS}$ pin is at "H" level, the $\overline{WR}$ signal cannot be input to the device.
38	$\overline{RD}$	I	CPU interface read signal. For parallel input interface, a status signal for each channel is output from the D0-D7 pins when the $\overline{RD}$ pin is at "L" level. For the serial input interface, a status signal for each channel is output from the D5/D0 pin. This pin has a pull-up resistor built-in.
39	$\overline{CS}$	I	CPU interface chip select pin. When $\overline{CS}$ pin is at "H" level, the $\overline{WR}$, and $\overline{RD}$ signals cannot be input to the device.
41-44	D3/STA3 D2/STA2 D1/STA1 D0/STA0	I/O	CPU interface data bus pins in the parallel input interface become data input pins when $\overline{WR}$ is at "L" level. They become channel status output pins in the serial input interface. These pins also become channel status output pins when $\overline{RD}$ is at "L" level.

Pin No.	Pin Symbol	I/O	Description
45	D4/STASEL	I/O	CPU interface data bus pin in the parallel input interface. This pin becomes a data input pin when $\overline{WR}$ is at "L" level. It becomes a channel status output pin when $\overline{RD}$ is at "L" level. It outputs a $\overline{BUSY}$ signal for channel 1. For the serial input interface, it becomes a channel status changeover pin. When D4/STASEL is at "L" level, the D3/STA3-D0/STA0 pins output the NCR (Next Command Request) for each channel. When the D4/STASEL is at "H" level, the D3/STA3-D0/STA0 pins output $\overline{BUSY}$ signals for their corresponding channels.
46	D5/DO	I/O	CPU interface data bus pin in the parallel input interface. This pin becomes a data input pin when $\overline{WR}$ is at "L" level. It becomes a channel status output pin when $\overline{RD}$ is at "L" level. This pin outputs 2 channels of $\overline{BUSY}$ signal. When $\overline{CS}$ and $\overline{RD}$ are at "L" level, this D5/DO pin serially outputs the status of each channel in synchronization with D6/SCK clock.
47	D6/SCK	I/O	CPU interface data bus pin in the parallel input interface. This pin becomes a data input pin when $\overline{WR}$ is at "L" level. It becomes a channel status output pin when $\overline{RD}$ is at "L" level. It outputs a $\overline{BUSY}$ signal for channel 3. This pin becomes a serial clock input pin for the serial input interface. When the SCK pin input is at "L" level on the falling edge of the $\overline{CS}$ pin signal, the DI pin input signal goes into the device on at the rising edge of the SCK clock, and the data is output from the DO pin. When the SCK pin input is at "H" level on the falling edge of the $\overline{CS}$ pin signal, the DI pin input signal goes into the device on the falling edge of the SCK clock, and the data is output from the DO pin.
48	D7/DI	I/O	CPU interface data bus pin in the parallel input interface. When $\overline{WR}$ is at "L" level, it becomes a data input pin. When $\overline{RD}$ is at "L" level, it becomes a channel status output pin. It outputs a $\overline{BUSY}$ signal for channel 4. For the serial input interface, this pin becomes a serial data input pin. Works as serial data input pin in the serial input interface.
50	DAOL	O	Outputs the left 14-bit DAC analog signal.
51	AOUTL	O	Outputs the left 14-bit DAC analog signal via voltage follower.
53	DAOR	O	Outputs the right 14-bit DAC analog signal.
54	AOUTR	O	Outputs the right 14-bit DAC analog signal via voltage follower.
56	$\overline{RCS}$	I	"L" level: RA22-0, A-1, and $\overline{ROE}$ pins output the address data and the output enable signal. "H" level: RA22-0, A-1, and $\overline{ROE}$ pins are in high impedance.
58	$\overline{ROE}$	O	Output enable pin for an externally connected memory. $\overline{RCS}$ pin = "H" level: High impedance
59	SERIAL	I	CPU interface switching pin. "H" level: Serial input interface, "L" level: Parallel input interface

Pin No.	Pin Symbol	I/O	Description
40	OPTANA	I	Device test pin. Fix this pin to “L” level.
62	DASCK	O	Device test pin. Leave this pin open.
63	DASD	O	Device test pin. Leave this pin open.
64	DASEL	O	Device test pin. Leave this pin open.
65	TEST	I	Device test pin. Input “L” level. This pin has a pull-down resistor built in.
55	AV_{DD}	—	Analog power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and AGND pin.
21, 70-72	DV_{DD}	—	Digital power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and DGND pin.
49	AGND	—	Analog ground pin.
4, 31, 57, 69	DGND	—	Digital ground pin.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (3 V)

(GND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	—	2.7 to 3.6			V
Operating temperature	T_{OP}	—	–40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

RECOMMENDED OPERATING CONDITIONS (5 V)

(GND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	—	4.5 to 5.5			V
Operating temperature	T_{OP}	—	–40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

ELECTRICAL CHARACTERISTICS

DC Characteristics (3 V)

DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86 × V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.14 × V_{DD}	V
"H" output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = V_{DD}	—	—	10	µA
"H" input current 2 (Note 1)	I_{IH2}	V_{IH} = V_{DD}	0.3	3.0	15	µA
"H" input current 3 (Note 4)	I_{IH3}	V_{IH} = V_{DD}	8	—	130	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (Note 2)	I_{IL2}	V_{IL} = GND	–120	—	–10	µA
"L" input current 3 (Note 1)	I_{IL3}	V_{IL} = GND	–15	–3.0	–0.3	µA
Output leakage current (Note 3)	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}	–10	—	+10	µA
Operating current consumption 1	I_{DD1}	f_{OSC} = 4 MHz at no load OPTANA = "L"	—	8	20	mA
Operating current consumption 2	I_{DD2}	f_{OSC} = 4 MHz at no load OPTANA = "H"	—	10	30	mA
Standby current consumption	I_{DS}	Ta = –40 to +70°C	—	—	15	µA
		Ta = –40 to +85°C	—	—	50	µA

Notes: 1. Applies to XT pin.
2. Applies to $\overline{RD}$ pin.
3. Applies to RA22 to RA0, D15/A-1, and $\overline{ROE}$ pins.
4. Applies to TEST pin.

DC Characteristics (5 V)

DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8 × V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.2 × V_{DD}	V
"H" output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = V_{DD}	—	—	10	µA
"H" input current 2 (Note 1)	I_{IH2}	V_{IH} = V_{DD}	0.8	5.0	20	µA
"H" input current 3 (Note 4)	I_{IH3}	V_{IH} = V_{DD}	30	—	350	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (Note 2)	I_{IL2}	V_{IL} = GND	–230	—	–60	µA
"L" input current 3 (Note 1)	I_{IL3}	V_{IL} = GND	–20	–5.0	–0.8	µA
Output leakage current (Note 3)	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}	–10	–3.0	+10	µA
Operating current consumption 1	I_{DD1}	f_{OSC} = 4 MHz at no load OPTANA = "L"	—	14	30	mA
Operating current consumption 2	I_{DD2}	f_{OSC} = 4 MHz at no load OPTANA = "H"	—	17	40	mA
Standby current consumption	I_{DS}	Ta = –40 to +70°C	—	—	15	µA
		Ta = –40 to +85°C	—	—	100	µA

Notes: 1. Applies to XT pin.
2. Applies to $\overline{RD}$ pin.
3. Applies to RA22 to RA0, D15/A-1, and $\overline{ROE}$ pins.
4. Applies to TEST pin.

Analog Section Characteristics (3 V)

DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT, AOUTR output load resistance	R_{LAO}	—	50	—	—	kΩ
AOUT, AOUTR output voltage range	V_{AOUT}	No output load	0.5	—	AV_{DD} – 0.5	V
DAOL, DAOR output impedance	R_{DAO}	—	30	43	60	kΩ

Analog Section Characteristics (5 V)

DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT, AOUTR output load resistance	R_{LAO}	—	50	—	—	kΩ
AOUT, AOUTR output voltage range	V_{AOUT}	No output load	0.5	—	AV_{DD} – 0.5	V
DAOL, DAOR output impedance	R_{DAO}	—	30	43	60	kΩ

FUNCTIONAL DESCRIPTION

Micro-computer Interface

The micro-computer interface in the ML2240 has 2 types of interface circuits built in: Parallel interface and serial interface. The interface setting can be changed with the SERIAL pin.

SERIAL pin = "H" level: Serial interface
SERIAL pin = "L" level: Parallel interface

Table below shows the SERIAL pin status in the serial and parallel interfaces.

SERIAL = "L"		SERIAL = "H"	
Parallel interface		Serial interface	
D7 (I/O)	Data input and output pins/ status output pin	DI (I)	Serial data input pin
D6 (I/O)		SCK (I)	Serial clock input pin
D5 (I/O)		DO (O)	Channel status serial output pin
D4 (I/O)		STASEL (I)	Channel status switching pin NCRn output at "L" level $\overline{\text{BUSY}}$n output at "H" level
D3 (I/O)		STA3 (O)	Channel 4 status output pin
D2 (I/O)		STA2 (O)	Channel 3 status output pin
D1 (I/O)		STA1 (O)	Channel 2 status output pin
D0 (I/O)		STA0 (O)	Channel 1 status output pin

1. Parallel Interface

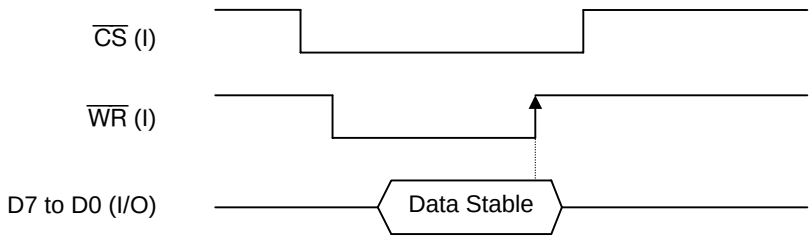
   When selecting the parallel interface, the I/O pins $\overline{\text{CS}}$, $\overline{\text{WR}}$, D7 to D0, and $\overline{\text{RD}}$ are used as input pins to input various commands and data, and as output pins to read out the status of the commands and data input.

   The micro-computer interface becomes effective when the $\overline{\text{CS}}$ pin is set to "L" level.

   When a command or data is input, the input data to D7 through D0 pins is captured inside the device on the rising edge of the $\overline{\text{WR}}$ pin.

   To read the channels status, pins $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are made "L" level. By doing so, the status signals of each channel are output to D7 through D0 pins.

Command and Data Input Timing



Status Read Timing

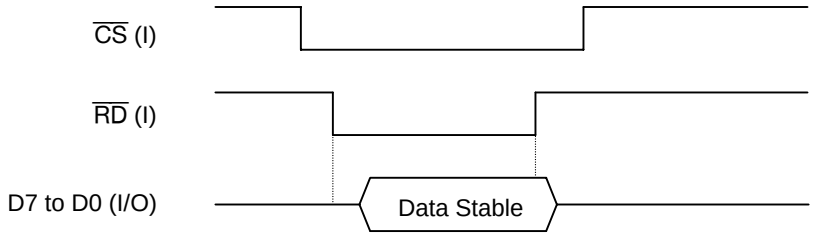


Table below shows the contents of each data output when reading the status of the channels.

Pin	Output status signal
D7	Channel 4 BUSY output (BUSY4)
D6	Channel 3 BUSY output (BUSY3)
D5	Channel 2 BUSY output (BUSY2)
D4	Channel 1 BUSY output (BUSY1)
D3	Channel 4 NCR output (NCR4)
D2	Channel 3 NCR output (NCR3)
D1	Channel 2 NCR output (NCR2)
D0	Channel 1 NCR output (NCR1)

The BUSY signal outputs “L” level when either a command is being processed or the playback of a pertinent channel is going on. In other states, the BUSY signal outputs “H” level.
The NCR signal outputs “L” level when either a command is being processed or a pertinent channel is in standby for playback. In other states, the NCR signal outputs “H” level.

2. Serial Interface

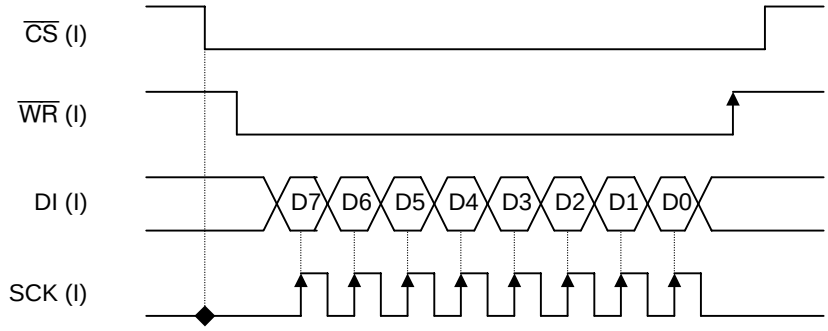
When selecting the serial interface, the I/O pins $\overline{CS}$, $\overline{WR}$, DI. SCK, $\overline{RD}$, and DO are used as input pins to input various commands and data, and as output pins to read out the status of the commands and data.

The micro-computer interface becomes effective when $\overline{CS}$ pin is set to “L” level.

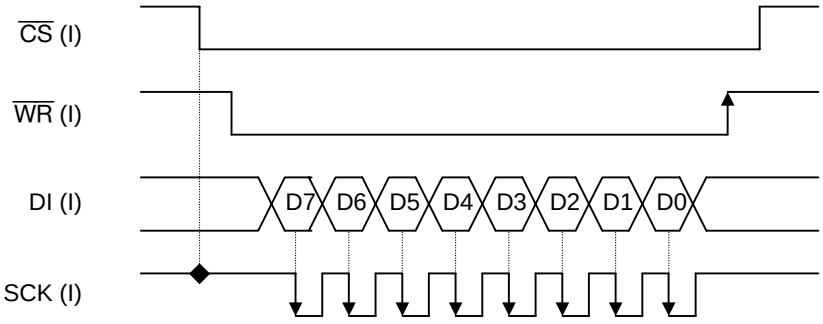
To input the commands and data, “L” level is input to $\overline{CS}$ and $\overline{WR}$ pins followed by, from MSB, to DI pin in synchronization with the input clock signal at SCK pin. Data at DI pin is captured inside the device on the rising or falling edge of the clock at SCK pin. And the command is executed on the rising edge of the $\overline{WR}$ pin. The selection of rising/falling edge of SCK clock is determined by the input level of the SCK pin on the falling edge of the $\overline{CS}$ pin. If the SCK pin on the falling edge of the $\overline{CS}$ pin is at “L” level, the DI pin data is captured inside the device on the rising edge of SCK clock. Conversely, if the SCK pin on the falling edge of the $\overline{CS}$ pin is at “H” level, then the DI pin data is captured on the falling edge of SCK clock.

Command and Data Input Timings

- SCK Rising Edge Operation



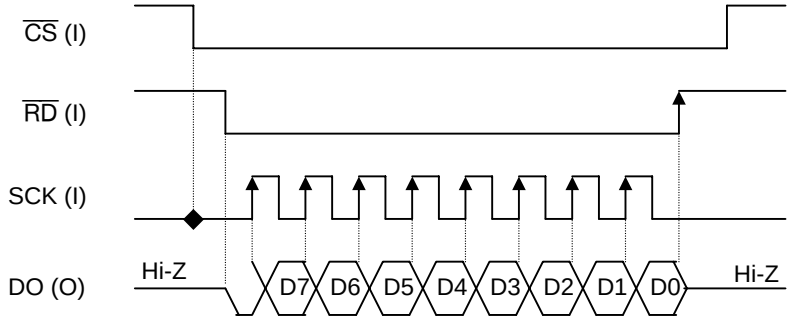
- SCK falling Edge Operation



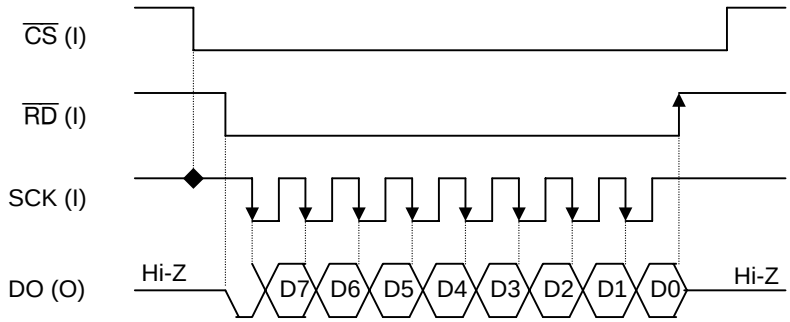
To read the channel status, input “L” level to $\overline{CS}$ and $\overline{RD}$ pins. D0 pin will output the channel status in synchronization with SCK clock.
The selection of rising/falling edge of SCK clock, similar to when inputting the commands and data, is determined by the level at SCK pin at the falling edge of $\overline{CS}$ pin.
The status signals in the parallel interface are output to D7 to D0 pins sequentially from D7.

Status Read Timing

- SCK Rising Edge Operation



- SCK Falling Edge Operation



Commands List

Each command is 1-byte (8 bits) input. PLAY, MUON, and FLASH I/F only are 2 bytes input.

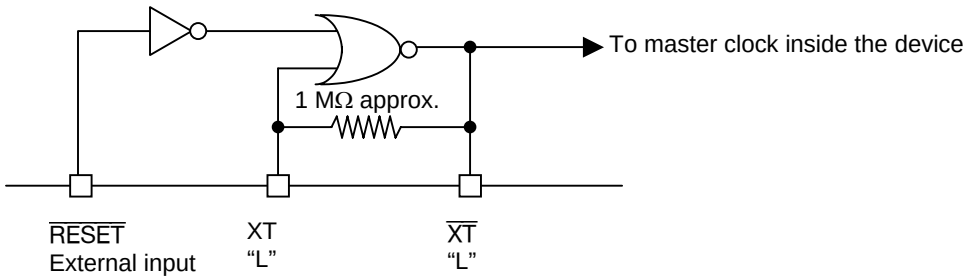
Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP1	0	0	0	0	—	—	—	—	Instantly shifts the power down device to the command standby state.
PUP2	0	0	0	1	—	—	—	—	Suppresses pop noise and shifts the power down device to the command standby state.
PDWN1	0	0	1	0	—	—	—	—	Instantly shifts the device from the command standby state to the power down state.
PDWN2	0	0	1	1	—	—	—	—	Suppresses pop noise and shifts the device from the command standby state to power down state.
PLAY	0	1	0	0	C3	C2	C1	C0	Inputs the phrase after the playback channel is specified, and then starts the playback.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	C3	C2	C1	C0	Playback start command with phrase specification. Inputs the phrase after the playback channel is specified, and then starts the playback. Playback start command without phrase specification. Inputs the phrase with the FADR command and starts the playback on multiple channels at the same time.
FADR	0	1	1	0	C3	C2	C1	C0	Phrase specification command. With this command, specifies the playback phrase for each channel.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	1	C3	C2	C1	C0	Playback stop command.
MUON	1	0	0	0	C3	C2	C1	C0	Specifies the channel for inserting silence, inputs the silence duration, and then inserts silence.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	1	C3	C2	C1	C0	Repeats the playback mode setting command. Effective only for the channel being used for playback.
CLOOP	1	0	1	0	C3	C2	C1	C0	Repeat playback mode releasing command. Inputting the STOP command releases repeat playback mode automatically.
VOL	1	0	1	1	C3	C2	C1	C0	Specifies the channel for which the sound volume is to be set, and then sets the volume for that channel.
	—	—	—	V4	V3	V2	V1	V0	
PAN	1	1	0	0	C3	C2	C1	C0	Sets the volume for the Left/Right of each channel.
	—	—	—	L4	L3	L2	L1	L0	
	—	—	—	R4	R3	R2	R1	R0	

C3, C2, C1, C0 : Channel specification (C3 = "1": Channel 4; C2 = "1": Channel 3; C1 = "1": Channel 2, C0 = "1": Channel 1)
F7 to F0 : Phrase address
M7 to M0 : Silence time length
V4 to V0 : Sound volume
L4 to L0 : Left sound volume
R4 to R0 : Right sound volume

Power Down Function

In power down state, the power down function in the device stops the internal operation and oscillation, sets AOUT to GND, and minimizes the static Idd.

Figure below shows the equivalent circuit of $\overline{XT}$ and XT pins.



Channel Status

Channel status is of 2 types: NCRn and $\overline{BUSYn}$.

Channel	Channel status	
CH1	NCR1	$\overline{BUSY1}$
CH2	NCR2	$\overline{BUSY2}$
CH3	NCR3	$\overline{BUSY3}$
CH4	NCR4	$\overline{BUSY4}$

NCRn = "H" indicates that it is possible to input the PLAY, START, and MUON commands for the phrase to be played back next for channel n.

$\overline{BUSYn}$ = "H" indicates a state in which channel n has not performed voice processing. $\overline{BUSYn}$ = "L" indicates a state in which channel n is performing voice processing.
Meanwhile, after a command is input, the NCR and $\overline{BUSY}$ signals of all channels are at "L" level during the processing of the command.
For Status output methods, see the Micro-computer Interface section.

Voice Synthesis Algorithm

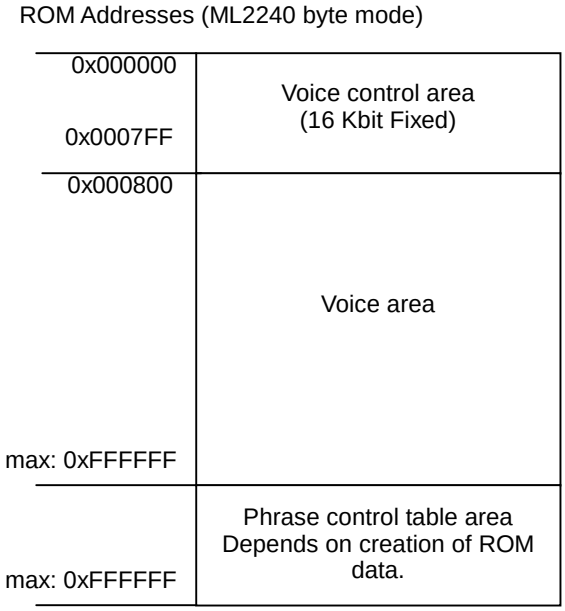
The ML2240 contains 5 algorithm types to match the characteristic of playback voice: 2-bit ADPCM 2 algorithm, 4-bit ADPCM 2 algorithm, 8-bit PCM algorithm, 8-bit non-linear PCM algorithm, and 16-bit PCM algorithm. Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Applied waveform	Feature
Oki 2-bit ADPCM2	Normal voice waveform	Oki's specific speech synthesis algorithm of low bit rate with improved 2-bit ADPCM.
Oki 4-bit ADPCM2	Normal voice waveform	Oki's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
Oki 8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM	High-frequency components inclusive sound effect etc.	Normal 8-bit PCM algorithm
16-bit PCM	High-frequency components inclusive sound effect etc.	Normal 16-bit PCM algorithm

Memory Allocation and Creating Voice Data

The ROM is partitioned into 3 data areas: voice (i.e., phrase) control area, voice area, and phrase control table area. The voice control area manages the ROM's voice data. It controls the start/end addresses of voice data, usage/not usage of the phrase control table function and so on. The voice control area stores voice control data for 256 phrases.
The voice area stores the actual waveform data.
The phrase control table area stores data for effective use of voice data. As for the details, please refer to the Phrase control table Function.
There is no phrase control table area if the phrase control table is not used.

The ROM data is created using a development tool.



Playback Time and Memory Capacity

The playback time depends upon the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.

$$\text{Playback time [sec]} = \frac{1.024 \times (\text{Memory capacity} - 16)\ (\text{Kbit})}{\text{Sampling frequency (kHz)} \times \text{Bit length}}$$

(Bit length is ADPCM, ADPCM 2 = 4 bits; PCM = 8 bits.)

Example: Let the sampling frequency be 16 kHz and 4-bit ADPCM algorithm. If one 8 Mbits ROM is used, then the playback time is obtained as follows:

$$\text{Playback time} = \frac{1.024 \times (8192 - 16)\ (\text{Kbit})}{16\ (\text{kHz}) \times 4\ (\text{bit})} \cong 131\ (\text{sec})$$

The above equation gives the playback time when the phrase control table function is not used.

Mixing Function

The ML2240 can perform simultaneous mixing of 4 channels. It is possible to specify PLAY and STOP for each channel separately.

- Precautions for Waveform Clamp at the Time of Channels Mixing
  When mixing of channels is done, the clamp occurrence possibility increases from the mixing calculation point of view. If it is known beforehand that the clamp will occur, then adjust the sound volume by VOL command.

- Mixing of Different Sampling Frequency
  It is not possible to perform analog mixing by a different sampling frequency.
  When performing analog mixing, the sampling frequency group of the first playback channel is selected. Therefore, please note that if analog mixing is performed by a sampling frequency group other than the selected sampling frequency group, then the playback will not be of constant speed: some times faster and at other times slower.
  The available sampling groups for analog mixing by a different sampling frequency are listed below.
  4.0 kHz, 8.0 kHz, 16.0 kHz, 32.0 kHz ··· (Group 1)
  5.3 kHz, 10.6 kHz, 21.3 kHz, 42.7 kHz ··· (Group 2)
  6.4 kHz, 12.8 kHz, 25.6 kHz ··· (Group 3)

Figures below show a case when a sampling frequency group played back a different sampling frequency group.

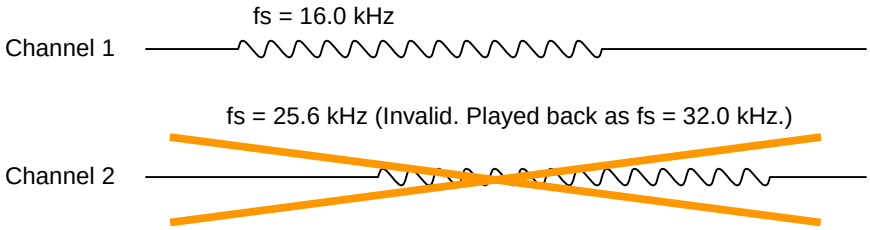


Figure 1 In Case a Different Sampling Frequency Played Back during Playback of the Other Channel Playback

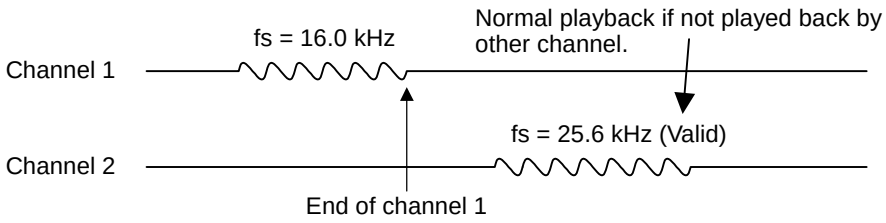


Figure 2 In Case a Different Sampling Frequency Played Back after the End of the Other Channel

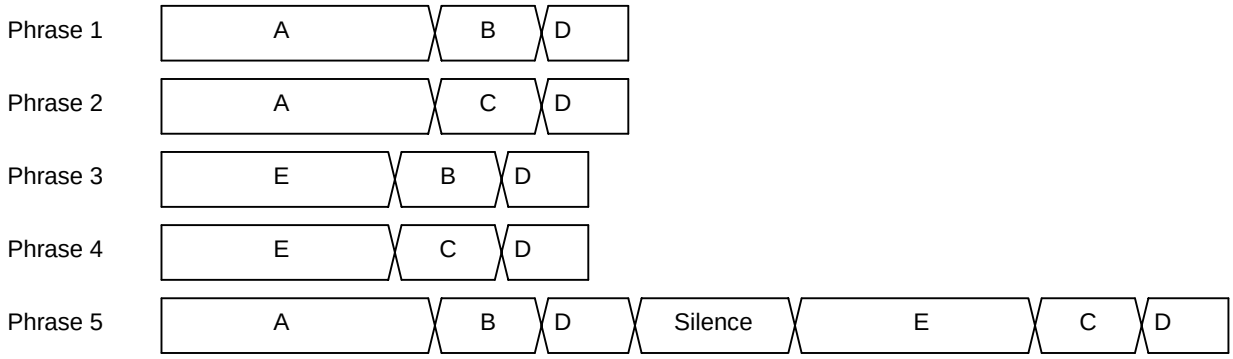
Phrase Control Table Function

The phrase control table function makes it possible to play back multiple phrases in succession. The following functions are set using the phrase control table function:

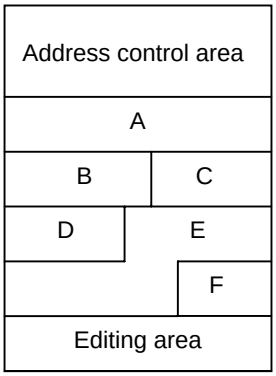
- Continuous playback: There is no limit to the number of times a continuous playback can be specified. It depends on the memory capacity only.
- Silence insertion function: 4 to 1024 ms

Using the phrase control table function enables to effectively use the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the phrase control table function.

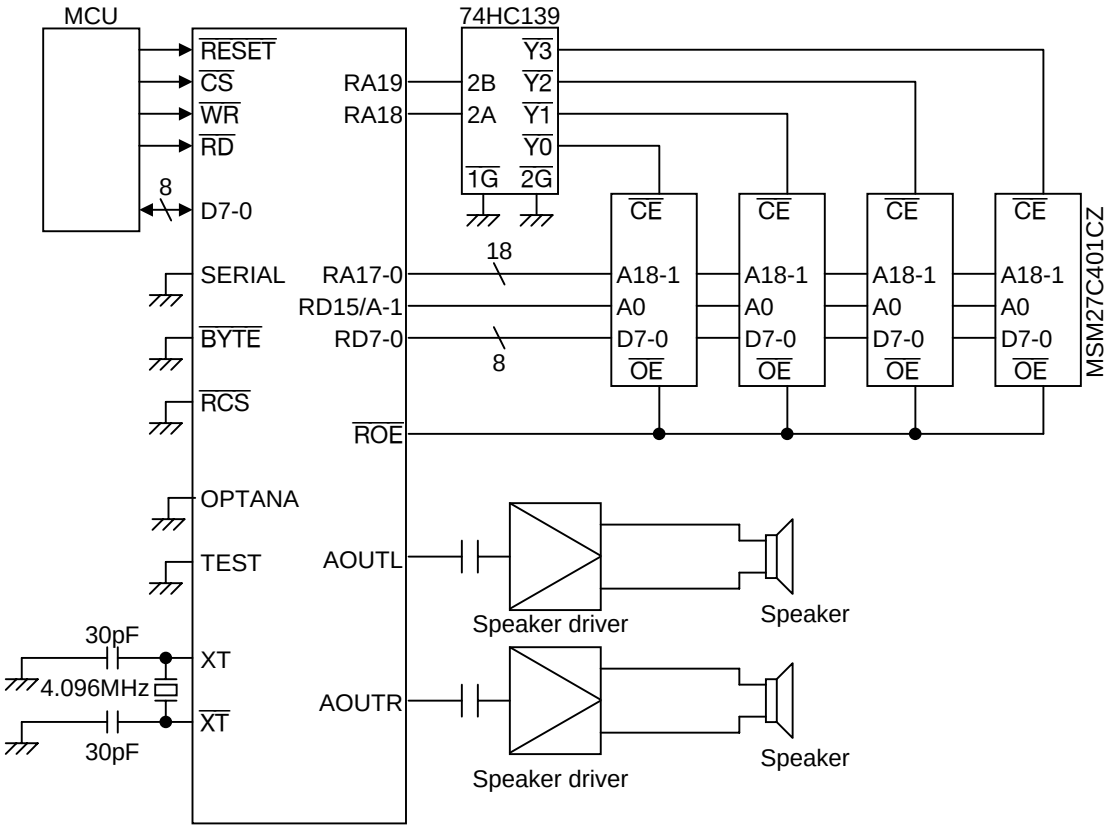
Example 1: Phrases Using the Phrase Control Table Function



Example 2: Example of ROM Data in case Example 1 Converted to ROM



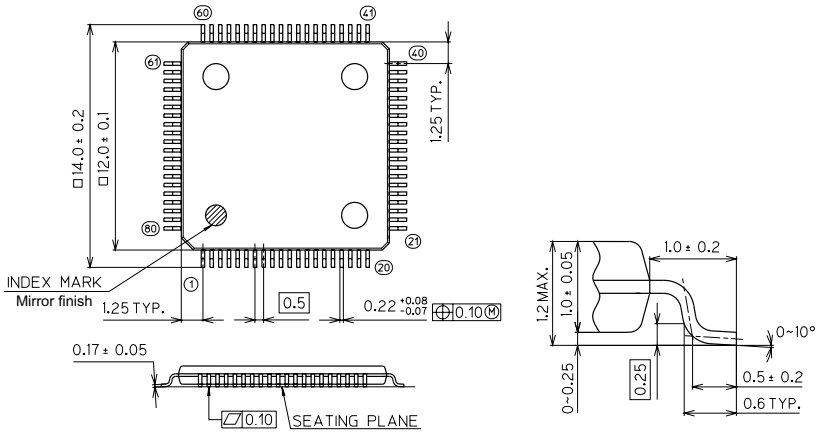
APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

(Unit: mm)

TQFP80-P-1212-0.50-K



Oki Electric Industry Co., Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.40 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL2240DIGEST-01	Oct. 17, 2003	—	—	Final edition 1
FEDL2240DIGEST-02	Jul. 12, 2004	15	15	Corrected first byte of Play command.

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