10-Bit 20 MSPS Monolithic A/D Converter

AD773A

1.1 Scope.

This specification covers the detail requirements for a complete monolithic 10-bit, 20 Msps A/D converter with an on-chip, high performance track-and-hold amplifier (THA).

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD773ASD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin Side Brazed Ceramic DIP

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

AV_{DD} to AGND . . . . . −0.5 V to +6.5 V
AV_{SS} to AGND . . . . . −6.5 V to +0.5 V
DV_{DD}, DRV_{DD} to DGND . . . . . −0.5 V to +6.5 V
AGND to DGND . . . . . −1 V to +1 V
AV_{DD} to DV_{DD} . . . . . −6.5 V to +6.5 V
Clock Input to DGND . . . . . −0.5 V to DV_{DD} + 0.5 V
Digital Outputs to DGND . . . . . −0.5 V to DV_{DD} + 0.3 V
REF IN to AV_{DD} . . . . . AV_{SS} to 0 V
REF IN to AV_{SS} . . . . . 0 V to AV_{DD}
V_{INA}, V_{INB}, REF IN to AGND . . . . . −6.5 V to +6.5 V
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

1.5 Thermal Characteristics.

Thermal Resistance: θ_{JC} = 25°C/W
θ_{JA} = 60°C/W

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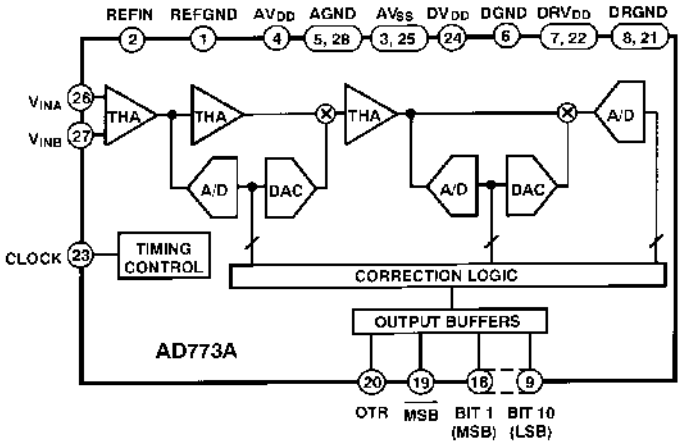
Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition	Units
Resolution	RES	−1	10	10	10		Bits
Zero Error	B_{POE}	−1	0.5	0.5			±% FSR max
Gain Error	A_E	1	0.5	0.5			±% FSR max
Zero Error Drift	TCB_{POE}	1			3.5	External 2.5 V Reference	±% FSR max
Gain Error Drift	TCA_{EXT}	−1			2	External 2.5 V Reference	±% FSR max
Power Supply Rejection	PSR	−1	18	18	18	See Note 1	±mV/V max
Analog Input Range	V_{IN}	−1	1	1	1		V p-p
Input Resistance	R_{IN}	−1	200				kΩ
Input Capacitance	C_{IN}	−1	10				pF
Power Dissipation	PD	−1	1.2	1.2	1.2		Watts max
Power Supply Current	I_{AVDD}	−1	80	80	80		mA max
	I_{AVSS}		140	140	140		
	I_{DVDD}		20	20	20		
	I_{DRVDD}		15	15	15		
Signal-to-Noise Distortion Ratio	S/(N+D)	−1	51	51	51	f_{IN} = 1 MHz; f_S = 20 MHz	dB min
Total Harmonic Distortion	THD	−1	−56	−56	−56	f_{IN} = 1 MHz; f_S = 20 MHz	dB max
Logic Input High Voltage	V_{IH}	−1	3.5	3.5	3.5		V min
Logic Input Low Voltage	V_{IL}	−1	0.5	0.5	0.5		V max
Logic Input High Current (CLK)	I_{IH}	−1	10	10	10		+μA max
Logic Input Low Current (CLK)	I_{IL}	−1	10	10	10		±μA max
Logic Output High Voltage	V_{OH}	−1	2.4	2.4	2.4	I_{SOURCE} − 500 μA	V min
Logic Output Low Voltage	V_{OL}	−1	0.4	0.4	0.4	I_{SINK} = 1.6 mA	V min
Clock Period	t_C	1	50	50	50		ns min
Output Delay	t_{OD}	−1	20				ns min
Pipeline Delay	t_{PD}	−1	4				Clock Cycles max
Clock Pulse Width High	t_{CH}	−1	25				ns min
Clock Pulse Width Low	t_{CL}	−1	25				ns min

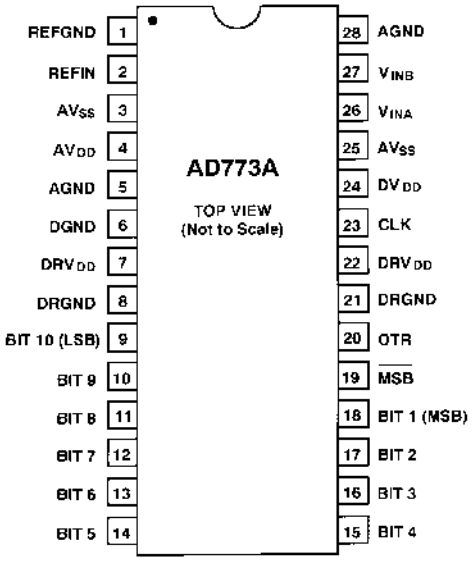
NOTES

[1]Test conditions for PSR: 4.75 V ≤ AV_{DD} ≤ 5.25 V, 4.75 V ≤ D_{DVDD} ≤ 5.25 V, −4.75 V ≤ AV_{SS} ≤ −5.25 V, 4.75 V ≤ DRV_{DD} ≤ 5.25 V.

3.2.1 Functional Block Diagram and Terminal Assignments.



D Package



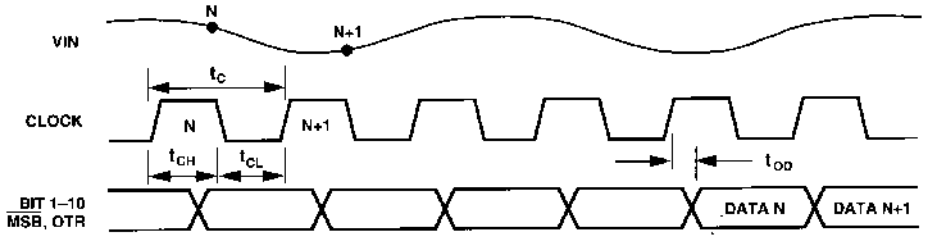


Figure 1. Timing Diagram

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (93).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).