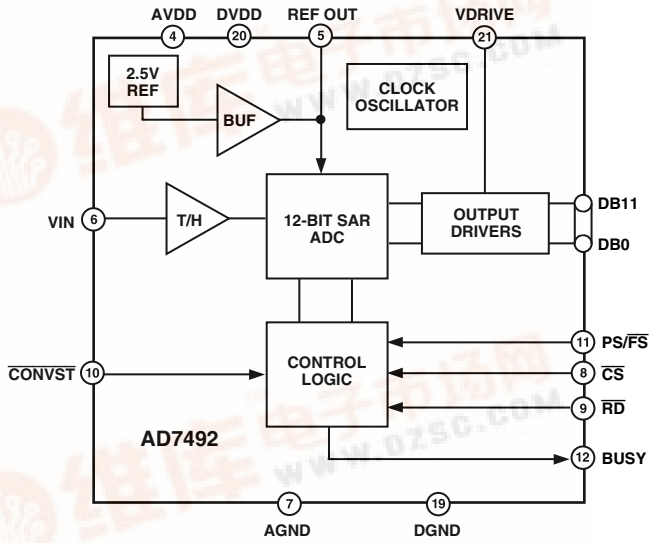
1.25 MSPS, 16 mW Internal REF and CLK, 12-Bit Parallel ADC

AD7492

FEATURES

Specified for V_{DD} of 2.7 V to 5.25 V
Throughput Rate of 1 MSPS—AD7492
Throughput Rate of 1.25 MSPS—AD7492-5
Low Power
4 mW Typ at 1 MSPS with 3 V Supplies
11 mW Typ at 1 MSPS with 5 V Supplies
Wide Input Bandwidth
70 dB Typ SNR at 100 kHz Input Frequency
2.5 V Internal Reference
On-Chip CLK Oscillator
Flexible Power/Throughput Rate Management
No Pipeline Delays
High-Speed Parallel Interface
Sleep Mode: 50 nA Typ
24-Lead SOIC and TSSOP Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7492 and AD7492-5 are 12-bit high-speed, low power, successive-approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.25 MSPS. They contain a low-noise, wide bandwidth track/hold amplifier that can handle bandwidths up to 10 MHz.

The conversion process and data acquisition are controlled using standard control inputs allowing easy interface to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$ and conversion is also initiated at this point. The BUSY goes high at the start of conversion and goes low 880 ns (AD7492) or 680 ns (AD7492-5) later to indicate that the conversion is complete. There are no pipeline delays associated with the part. The conversion result is accessed via standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals over a high-speed parallel interface.

The AD7492 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With 5 V supplies and 1.25 MSPS, the average current consumption AD7492-5 is typically 2.75 mA. The part also offers flexible power/throughput rate management.

It is also possible to operate the part in a full sleep mode and a partial sleep mode, where the part wakes up to do a conversion and automatically enters a sleep mode at the end of conversion. The type of sleep mode is hardware selected by the PS/$\overline{\text{FS}}$ pin. Using these sleep modes allows very low power dissipation numbers at lower throughput rates.

The analog input range for the part is 0 to REF IN. The 2.5 V reference is supplied internally and is available for external referencing. The conversion rate is determined by the internal clock.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption
   The AD7492-5 offers 1.25 MSPS throughput with 16 mW power consumption.
2. Flexible Power/Throughput Rate Management
   The conversion time is determined by an internal clock. The part also features two sleep modes, partial and full, to maximize power efficiency at lower throughput rates.
3. No Pipeline Delay
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{\text{CONVST}}$ input and once-off conversion control.
4. Flexible Digital Interface
   The V_{DRIVE} feature controls the voltage levels on the I/O digital pins.
5. Fewer Peripheral Components
   The AD7492 optimizes PCB space by using an internal Reference and internal CLK.

REV. 0

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AD7492-5—SPECIFICATIONS[1] (V_{DD} = 4.75 V to 5.25 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_S = 1.25 MSPS
Signal to Noise + Distortion (SINAD)	69	69	dB typ	f_{IN} = 500 kHz Sine Wave
	68	68	dB min	f_{IN} = 100 kHz Sine Wave
Signal-to-Noise Ratio (SNR)	70	70	dB typ	f_{IN} = 500 kHz Sine Wave
	68	68	dB min	f_{IN} = 100 kHz Sine Wave
Total Harmonic Distortion (THD)	–83	–83	dB typ	f_{IN} = 500 kHz Sine Wave
	–87	–87	dB typ	f_{IN} = 100 kHz Sine Wave
	–75	–75	dB max	f_{IN} = 100 kHz Sine Wave
Peak Harmonic or Spurious Noise (SFDR)	–83	–83	dB typ	f_{IN} = 500 kHz Sine Wave
	–90	–90	dB typ	f_{IN} = 100 kHz Sine Wave
	–76	–76	dB max	f_{IN} = 100 kHz Sine Wave
Intermodulation Distortion (IMD)				
Second Order Terms	–82	–82	dB typ	f_{IN} = 500 kHz Sine Wave
	–90	–90	dB typ	f_{IN} = 100 kHz Sine Wave
Third Order Terms	–71	–71	dB typ	f_{IN} = 500 kHz Sine Wave
	–88	–88	dB typ	f_{IN} = 100 kHz Sine Wave
Aperture Delay	5	5	ns typ	
Aperture Jitter	15	15	ps typ	
Full Power Bandwidth	10	10	MHz typ	
DC ACCURACY				f_S = 1.25 MSPS
Resolution	12	12	Bits	
Integral Nonlinearity	±1.5	±1.25	LSB max	
Differential Nonlinearity	+1.5/–0.9	+1.5/–0.9	LSB max	Guaranteed No Missed Codes to 12 Bits (A and B Version)
Offset Error	±9	±9	LSB max	
Gain Error	±2.5	±2.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to 2.5	0 to 2.5	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	33	33	pF typ	
REFERENCE OUTPUT				
REF OUT Output Voltage Range	2.5	2.5	V	±1.5% for Specified Performance
LOGIC INPUTS				
Input High Voltage, V_{INH}[2]	V_{DRIVE} × 0.7	V_{DRIVE} × 0.7	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}[2]	V_{DRIVE} × 0.3	V_{DRIVE} × 0.3	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V_{DRIVE} – 0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance	10	10	pF max	
Output Coding	Straight (Natural) Binary	Straight (Natural) Binary		
CONVERSION RATE				
Conversion Time	680	680	ns max	
Track/Hold Acquisition Time	120	120	ns min	
Throughput Rate	1.25	1.25	MSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS				
V_{DD}	4.75/5.25	4.75/5.25	V min/max	
I_{DD}				Digital I/Ps = 0 V or DV_{DD}.
Normal Mode	3.3	3.3	mA max	f_S = 1.25 MSPS, Typ 2.75 mA
Quiescent Current	1.8	1.8	mA max	
Partial Sleep Mode	250	250	µA max	Static. Typ 190 µA
Full Sleep Mode	1	1	µA max	Static. Typ 200 nA
Power Dissipation[4]				Digital I/Ps = 0 V or DV_{DD}
Normal Mode	16.5	16.5	mW max	
Partial Sleep Mode	1.25	1.25	mW max	
Full Sleep Mode	5	5	µW max	

NOTES
[1]Temperature ranges as follows: A and B Versions: –40°C to +85°C.
[2]V_{INH} and V_{INL} trigger levels are set by the V_{DRIVE} voltage. The logic interface circuitry is powered by V_{DRIVE}.
[3]Sample tested @ 25°C to ensure compliance.
[4]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7492–SPECIFICATIONS[1] (V_{DD} = 2.7 V to 5.25 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_S = 1 MSPS
Signal to Noise + Distortion (SINAD)	69	69	dB typ	f_{IN} = 500 kHz Sine Wave
	68	68	dB min	f_{IN} = 100 kHz Sine Wave
Signal-to-Noise Ratio (SNR)	70	70	dB typ	f_{IN} = 500 kHz Sine Wave
	68	68	dB min	f_{IN} = 100 kHz Sine Wave
Total Harmonic Distortion (THD)	–85	–85	dB typ	f_{IN} = 500 kHz Sine Wave
	–87	–87	dB typ	f_{IN} = 100 kHz Sine Wave
	–75	–75	dB max	f_{IN} = 100 kHz Sine Wave
Peak Harmonic or Spurious Noise (SFDR)	–86	–86	dB typ	f_{IN} = 500 kHz Sine Wave
	–90	–90	dB typ	f_{IN} = 100 kHz Sine Wave
	–76	–76	dB max	f_{IN} = 100 kHz Sine Wave
Intermodulation Distortion (IMD)				
Second Order Terms	–77	–77	dB typ	f_{IN} = 500 kHz Sine Wave
	–90	–90	dB typ	f_{IN} = 100 kHz Sine Wave
Third Order Terms	–69	–69	dB typ	f_{IN} = 500 kHz Sine Wave
	–88	–88	dB typ	f_{IN} = 100 kHz Sine Wave
Aperture Delay	5	5	ns typ	
Aperture Jitter	15	15	ps typ	
Full Power Bandwidth	10	10	MHz typ	
DC ACCURACY				f_S = 1 MSPS
Resolution	12	12	Bits	
Integral Nonlinearity	±1.5		LSB max	
		±0.6	LSB typ	V_{DD} = 5 V
		±1	LSB max	V_{DD} = 3 V
Differential Nonlinearity	+1.5/–0.9	+1.5/–0.9	LSB max	Guaranteed No Missed Codes to 12 Bits (A and B Version)
Offset Error	±9	±9	LSB max	
Gain Error	±2.5	±2.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to 2.5	0 to 2.5	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	33	33	pF typ	
REFERENCE OUTPUT				
REF OUT Output Voltage Range	2.5	2.5	V	±1.5% for Specified Performance
LOGIC INPUTS				
Input High Voltage, V_{INH}[2]	V_{DRIVE} × 0.7	V_{DRIVE} × 0.7	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}[2]	V_{DRIVE} × 0.3	V_{DRIVE} × 0.3	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V_{DRIVE} – 0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance	10	10	pF max	
Output Coding	Straight (Natural) Binary	Straight (Natural) Binary		
CONVERSION RATE				
Conversion Time	880	880	ns max	
Track/Hold Acquisition Time	120	120	ns min	
Throughput Rate	1	1	MSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS				
V_{DD}	2.7/5.25	2.7/5.25	V min/max	
I_{DD}				Digital I/Ps = 0 V or DV_{DD}.
Normal Mode	3	3	mA max	f_S = 1 MSPS, Typ 2.2 mA
Quiescent Current	1.8	1.8	mA max	
Partial Sleep Mode	250	250	µA max	Static. Typ 190 µA
Full Sleep Mode	1	1	µA max	Static. Typ 200 nA
Power Dissipation[4]				Digital I/Ps = 0 V or DV_{DD}
Normal Mode	15	15	mW max	V_{DD} = 5 V
Partial Sleep Mode	1.25	1.25	mW max	V_{DD} = 5 V
Full Sleep Mode	5	5	µW max	V_{DD} = 5 V

NOTES

[1]Temperature ranges as follows: A and B Versions: –40°C to +85°C.

[2]V_{INH} and V_{INL} trigger levels are set by the V_{DRIVE} voltage. The logic interface circuitry is powered by V_{DRIVE}.

[3]Sample tested @ 25°C to ensure compliance.

[4]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = 2.7 V to 5.25 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7492	AD7492-5[2]	Unit	Description
$t_{CONVERT}$	880	680	ns max	
t_{WAKEUP}	20[3]	20[3]	µs max	Partial Sleep Wake-Up Time
	500	500	µs max	Full Sleep Wake-Up Time
t_1	10	10	ns min	$\overline{CONVST}$ Pulsewidth
t_2	10	10	ns max	$\overline{CONVST}$ to BUSY Delay, V_{DD} = 5 V
	40	N/A	ns max	$\overline{CONVST}$ to BUSY Delay, V_{DD} = 3 V
t_3	0	0	ns max	BUSY to $\overline{CS}$ Setup Time
t_4[4]	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	20	20	ns min	$\overline{RD}$ Pulsewidth
t_6[4]	15	15	ns min	Data Access Time after Falling Edge of $\overline{RD}$
t_7[5]	8	8	ns max	Bus Relinquish Time after Rising Edge of $\overline{RD}$
t_8	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9	120	120	ns min	Acquisition Time
t_{10}	100	100	ns min	Quiet Time

NOTES

[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. See Figure 1.

[2]The AD7492-5 is specified with V_{DD} = 4.75 V to 5.25 V.

[3]This is the time needed for the part to settle within 0.5 LSB of its stable value. Conversion can be initiated earlier than 20 µs, but we cannot guarantee that the part will sample within 0.5 LSB of the true analog input value. Therefore we recommend that the user does not start conversion until after the specified time.

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[5]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

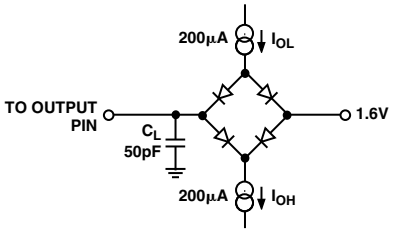


Figure 1. Load Circuit for Digital Output Timing Specifications

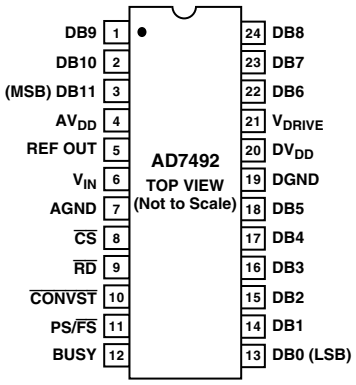
ABSOLUTE MAXIMUM RATINGS [1]

(T_A = 25°C unless otherwise noted)

AV_{DD} to AGND/DGND . . . . . –0.3 V to +7 V
DV_{DD} to AGND/DGND . . . . . –0.3 V to +7 V
V_{DRIVE} to AGND/DGND . . . . . –0.3 V to +7 V
AV_{DD} to DV_{DD} . . . . . –0.3 V to +0.3 V
V_{DRIVE} to DV_{DD} . . . . . –0.3 V to DVDD + 0.3 V
AGND TO DGND . . . . . –0.3 V to +0.3 V
Analog Input Voltage to AGND . . . –0.3 V to AVDD + 0.3 V
Digital Input Voltage to DGND . . . –0.3 V to DVDD + 0.3 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
  Commercial (A and B Versions) . . . . . –40°C to +85°C
  Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
SOIC, TSSOP Package Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 75°C/W (SOIC)
  . . . . . 115°C/W (TSSOP)
  θ_{JC} Thermal Impedance . . . . . 25°C/W (SOIC)
  . . . . . 35°C/W (TSSOP)
Lead Temperature, Soldering
  Vapor Phase (60 secs) . . . . . 215°C
  Infrared (15 secs) . . . . . 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7492 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Resolution (Bits)	Throughput Rate (MSPS)	Package Description	Package Option[1]
AD7492AR	–40°C to +85°C	12	1	SOIC	R-24
AD7492ARU	–40°C to +85°C	12	1	TSSOP	RU-24
AD7492BR	–40°C to +85°C	12	1	SOIC	R-24
AD7492BRU	–40°C to +85°C	12	1	TSSOP	RU-24
AD7492AR-5	–40°C to +85°C	12	1.25	SOIC	R-24
AD7492ARU-5	–40°C to +85°C	12	1.25	TSSOP	RU-24
AD7492BR-5	–40°C to +85°C	12	1.25	SOIC	R-24
AD7492BRU-5	–40°C to +85°C	12	1.25	TSSOP	RU-24
EVAL-AD7492CB[2]					Evaluation Board
EVAL-CONTROL BRD2[3]					Controller Board

NOTES
[1]R = SOIC; RU = TSSOP.
[2]This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1–3, 13–18, 22–24	DB9–DB11, DB0–DB5, DB6–DB8	Data Bit 0 to DB11. Parallel digital outputs that provide the conversion result for the part. These are three-state outputs that are controlled by $\overline{CS}$ and $\overline{RD}$. The output high voltage level for these outputs is determined by the V_{DRIVE} input.
4	AV_{DD}	Analog Supply Voltage, 2.7 V to 5.25 V. This is the only supply voltage for all analog circuitry on the AD7492. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. This supply should be decoupled to AGND.
5	REF OUT	Reference Out. The output voltage from this pin is 2.5 V ±1%.
6	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to REFIN. The analog input presents a high dc input impedance.
7	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7492. All analog input signals should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
8	$\overline{CS}$	Chip Select. Active low logic input used in conjunction with $\overline{RD}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to the same AND gate on the input so the signals are interchangeable. $\overline{CS}$ can be hardwired permanently low.
9	$\overline{RD}$	Read Input. Logic input used in conjunction with $\overline{CS}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to the same AND gate on the input so the signals are interchangeable. $\overline{CS}$ and $\overline{RD}$ can be hardwired permanently low, in which case the data bus is always active and the result of the new conversion is clocked out slightly before to the BUSY line going low.
10	$\overline{CONVST}$	Conversion Start Input. Logic input used to initiate conversion. The input track/hold amplifier goes from track mode to hold mode on the falling edge of $\overline{CONVST}$ and the conversion process is initiated at this point. The conversion input can be as narrow as 10 ns. If the $\overline{CONVST}$ input is kept low for the duration of conversion and is still low at the end of conversion, the part will automatically enter a sleep mode. The type of sleep mode is determined by the PS/$\overline{FS}$ pin. If the part enters a sleep mode, the next rising edge of $\overline{CONVST}$ wakes up the part. Wake-up time depends on the type of sleep mode.
11	PS/$\overline{FS}$	Partial Sleep/Full Sleep Mode. This pin determines the type of sleep mode the part will enter if the $\overline{CONVST}$ pin is kept low for the duration of the conversion and is still low at the end of conversion. In partial sleep mode the internal reference circuit and oscillator circuit is not powered down and draws 250 μA maximum. In full sleep mode all of the analog circuitry is powered down and the current drawn is negligible. This pin is hardwired either high (DV_{DD}) or low (GND).
12	BUSY	BUSY Output. Logic output indicating the status of the conversion process. The BUSY signal goes high after the falling edge of $\overline{CONVST}$ and stays high for the duration of conversion. Once conversion is complete and the conversion result is in the output register, the BUSY line returns low. The track/hold returns to track mode just prior to the falling edge of BUSY and the acquisition time for the part begins when BUSY goes low. If the $\overline{CONVST}$ input is still low when BUSY goes low, the part automatically enters its sleep mode on the falling edge of BUSY.
19	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7492. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
20	DV_{DD}	Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD7492 apart from the output drivers and input circuitry. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND.
21	V_{DRIVE}	Supply Voltage for the Output Drivers and Digital Input circuitry, 2.7 V to 5.25 V. This voltage determines the output high voltage for the data output pins and the trigger levels for the digital inputs. It allows the AV_{DD} and DV_{DD} to operate at 5 V (and maximize the dynamic performance of the ADC) while the digital input and output pins can interface to 3 V logic.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Gain Error
The last transition should occur at the analog value 1 1/2 LSB below the nominal full scale. The first transition is a 1/2 LSB above the low end of the scale (zero in the case of AD7492). The gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions with offset errors removed.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode after the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter is 62 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7492 it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

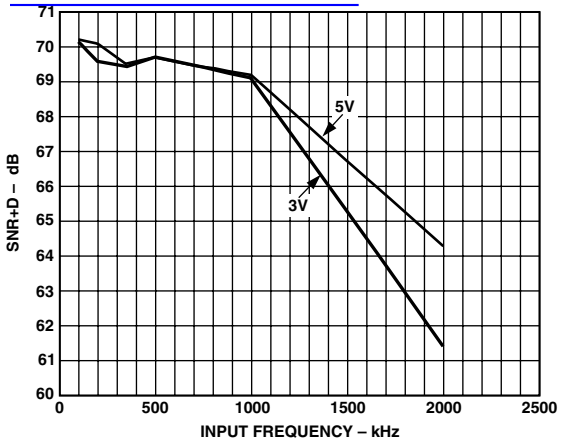
Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7492 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

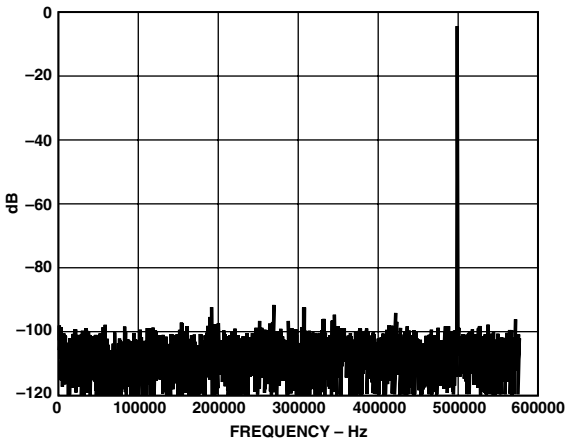
Aperture Delay
In a sample/hold, the time required after the hold command for the switch to open fully is the aperture delay. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

Aperture Jitter
Aperture jitter is the range of variation in the aperture delay. In other words, it is the uncertainty about when the sample is taken. Jitter is the result of noise which modulates the phase of the hold command. This specification establishes the ultimate timing error, hence the maximum sampling frequency for a given resolution. This error will increase as the input dV/dt increases.

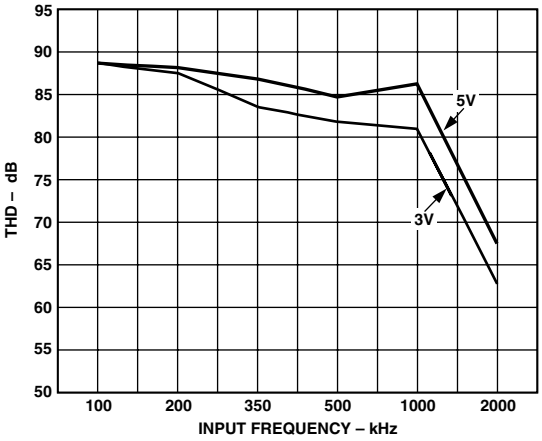
AD7492–Typical Performance Characteristics



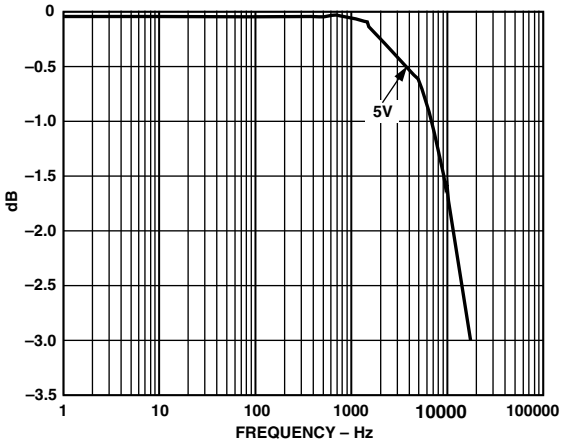
TPC 1. Typical SNR+D vs. Input Tone



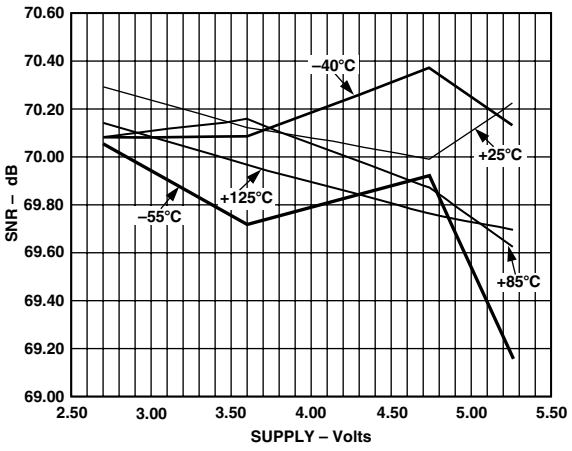
TPC 4. Typical SNR @ 500 kHz Input Tone



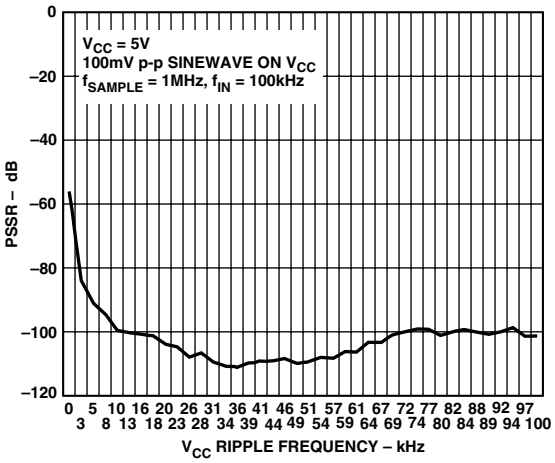
TPC 2. Typical THD vs. Input Tone



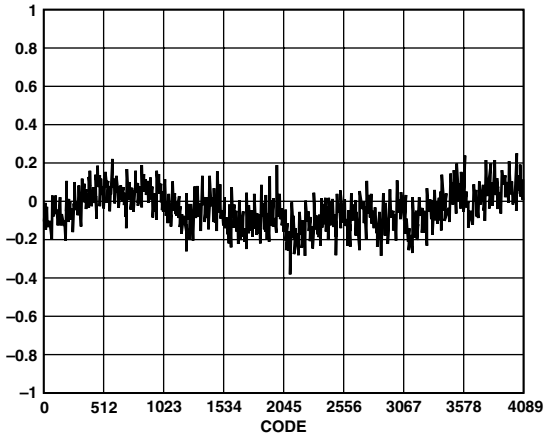
TPC 5. Typical Bandwidth



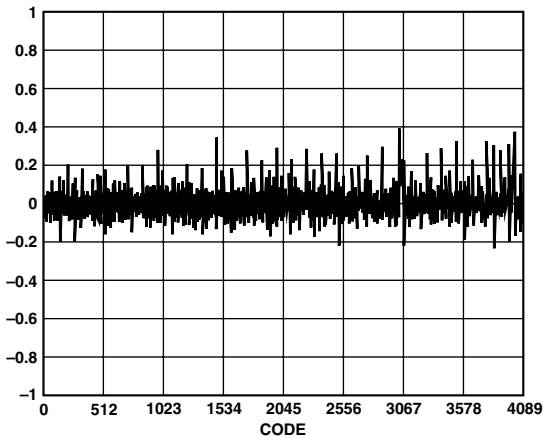
TPC 3. Typical SNR vs. Supply



TPC 6. Typical Power Supply Rejection Ratio (PSRR)



TPC 7. Typical INL for 2.75 V @ 25°C



TPC 8. Typical DNL for 2.75 V @ 25°C

CIRCUIT DESCRIPTION

CONVERTER OPERATION

The AD7492 is a 12-bit successive approximation analog-to-digital converter based around a capacitive DAC. The AD7492 can convert analog input signals in the range 0 V to V_{REF}. Figure 2 shows a very simplified schematic of the ADC. The Control Logic, SAR, and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition.

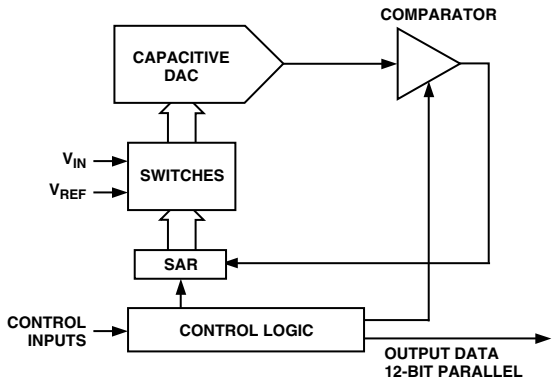


Figure 2. Simplified Block Diagram of AD7492

Figure 3 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

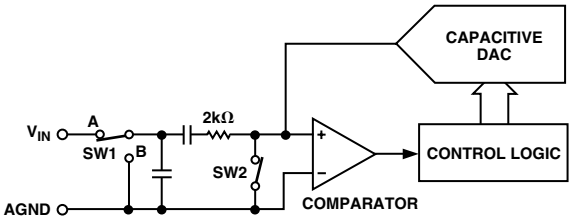


Figure 3. ADC Acquisition Phase

Figure 4 shows the ADC during conversion. When conversion starts, SW2 will open and SW1 will move to Position B, causing the comparator to become unbalanced. The ADC then runs through its successive approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced, the conversion result is available in the SAR register.

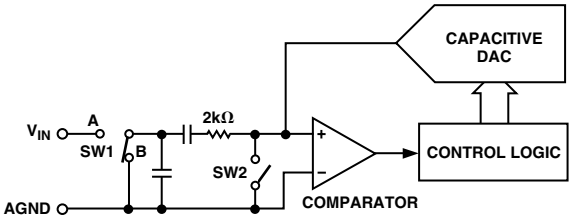


Figure 4. ADC Conversion Phase

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7492. Conversion is initiated by a falling edge on $\overline{\text{CONVST}}$. Once $\overline{\text{CONVST}}$ goes low the BUSY signal goes high, and at the end of conversion the falling edge of BUSY is used to activate an Interrupt Service Routine. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ lines are then activated in parallel to read the 12 data bits. The internal bandgap reference voltage is 2.5 V, providing an analog input range of 0 V to 2.5 V, making the AD7492 a unipolar A/D. A capacitor with a minimum capacitance of 100 nF is needed at the output of the REF OUT pin as it stabilizes the internal reference value. It is recommended to perform a dummy conversion after power-up as the first conversion result could be incorrect. This also ensures that the part is in the correct mode of operation. The $\overline{\text{CONVST}}$ pin should not be floating when power is applied as a rising edge on $\overline{\text{CONVST}}$ might not wake up the part.

In Figure 5 the V_{DRIVE} pin is tied to DV_{DD}, which results in logic output voltage values being either 0 V or DV_{DD}. The voltage applied to V_{DRIVE} controls the voltage value of the output logic signals and the input logic signals. For example, if DV_{DD} is supplied by a 5 V supply and V_{DRIVE} by a 3 V supply, the logic output voltage levels would be either 0 V or 3 V. This feature allows the AD7492 to interface to 3 V parts while still enabling the A/D to process signals at 5 V supply.

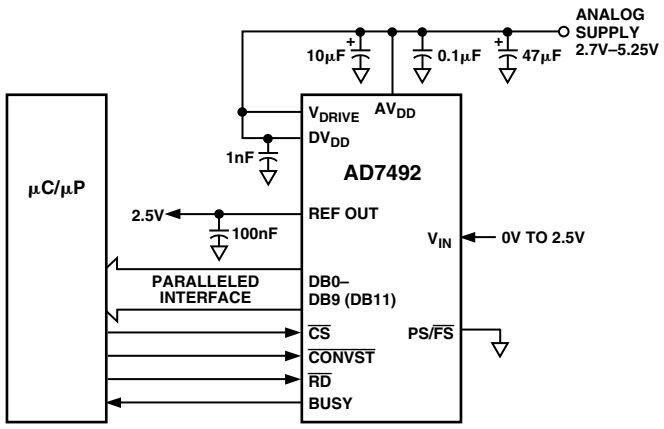


Figure 5. Typical Connection Diagram

ADC TRANSFER FUNCTION

The output coding of the AD7492 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSB, etc.). The LSB size is = 2.5/4096 for the AD7492. The ideal transfer characteristic for the AD7492 is shown in Figure 6.

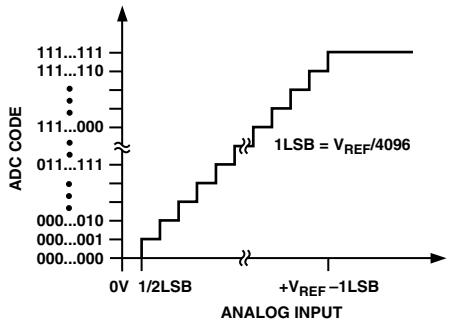


Figure 6. Transfer Characteristic for 12 Bits

AC ACQUISITION TIME

In ac applications it is recommended to always buffer analog input signals. The source impedance of the drive circuitry must be kept as low as possible to minimize the acquisition time of the ADC. Large values of impedance at the V_{IN} pin of the ADC will cause the THD to degrade at high input frequencies.

Table I. Dynamic Performance Specifications

Input Buffers	SNR 500 kHz	THD 500 kHz	Typical Amplifier Current Consumption
AD9631	69.5	80	17 mA
AD797	69.6	81.6	8.2 mA

DC Acquisition Time

The ADC starts a new acquisition phase at the end of a conversion and ends it on the falling edge of the $\overline{CONVST}$ signal. At the end of conversion there is a settling time associated with the sampling circuit. This settling time lasts 120 ns. The analog signal on V_{IN} is also being acquired during this settling time; therefore, the minimum acquisition time needed is 120 ns.

Figure 7 shows the equivalent charging circuit for the sampling capacitor when the ADC is in its acquisition phase. R3 represents the source impedance of a buffer amplifier or resistive network, R1 is an internal switch resistance, R2 is for bandwidth control, and C1 is the sampling capacitor. C2 is back-plate capacitance and switch parasitic capacitance.

During the acquisition phase the sampling capacitor must be charged to within 0.5 LSB of its final value.

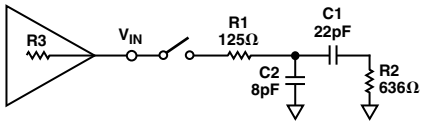


Figure 7. Equivalent Analog Input Circuit

ANALOG INPUT

Figure 8 shows the equivalent circuit of the analog input structure of the AD7492. The two diodes, D1 and D2, provide ESD protection for the analog inputs. The capacitor C3 is typically about 4 pF and can be primarily attributed to pin capacitance. The resistor R1 is an internal switch resistance. This resistor is typically about 125 Ω. The capacitor C1 is the sampling capacitor while R2 is used for bandwidth control.

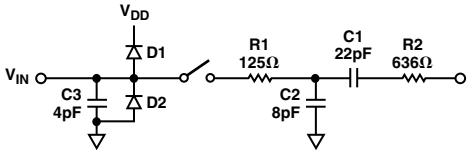


Figure 8. Equivalent Analog Input Circuit

PARALLEL INTERFACE

The parallel interface of the AD7492 is 12 bits wide. The output data buffers are activated when both $\overline{CS}$ and $\overline{RD}$ are logic low. At this point the contents of the data register are placed onto the data bus. Figure 9 shows the timing diagram for the parallel port.

Figure 10 shows the timing diagram for the parallel port when $\overline{CS}$ and $\overline{RD}$ are tied permanently low. In this setup, once the BUSY line goes from high to low, the conversion process is completed. The data is available on the output bus slightly before the falling edge of BUSY.

It is important to point out that the data bus cannot change state while the A/D is doing a conversion as this would have a detrimental effect on the conversion in progress. The data out lines will go three-state again when either the $\overline{RD}$ or $\overline{CS}$ line goes high. Thus the $\overline{CS}$ can be tied low permanently, leaving the $\overline{RD}$ line to control conversion result access. Please reference the V_{DRIVE} section for output voltage levels.

OPERATING MODES

The AD7492 has two possible modes of operation depending on the state of the $\overline{CONVST}$ pulse at the end of a conversion, Mode 1 and Mode 2.

Mode 1 (High-Speed Sampling)

In this mode of operation the $\overline{CONVST}$ pulse is brought high before the end of conversion, i.e., before the BUSY goes low (see Figure 10). If the $\overline{CONVST}$ pin is brought from high to low while BUSY is high, the conversion is restarted. When operating in

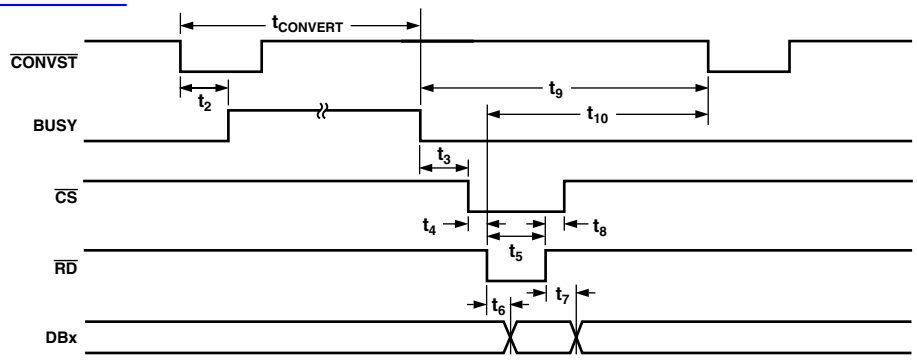


Figure 9. Parallel Port Timing

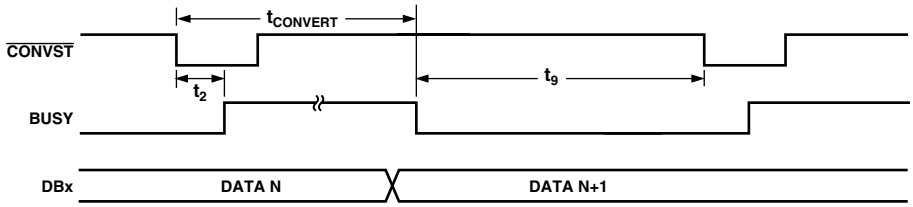


Figure 10. Parallel Port Timing with $\overline{CS}$ and $\overline{RD}$ Tied Low

this mode a new conversion should not be initiated until 140 ns after BUSY goes low. This acquisition time allows the track/hold circuit to accurately acquire the input signal. As mentioned earlier, a read should not be done during a conversion. This mode facilitates the fastest throughput times for the AD7492.

Mode 2 (Partial or Full Sleep Mode)

Figure 11 shows AD7492 in Mode 2 operation where the ADC goes into either partial or full sleep mode after conversion. The $\overline{CONVST}$ line is brought low to initiate a conversion and remains low until after the end of conversion. If $\overline{CONVST}$ goes high and low again while BUSY is high, the conversion is restarted. Once the BUSY line goes from a high to a low, the $\overline{CONVST}$ line has its status checked and, if low, the part enters a sleep mode. The type of sleep mode the AD7492 enters depends on what ever way the PS/$\overline{FS}$ pin is hardwired. If the PS/$\overline{FS}$ pin is tied high, the AD7492 will enter partial sleep mode. If the PS/$\overline{FS}$ pin is tied low, the AD7492 will enter full sleep mode.

The device wakes up again on the rising edge of the $\overline{CONVST}$ signal. From partial sleep the AD7492 is capable of starting conversions typically 1 µs after the rising edge of $\overline{CONVST}$. The $\overline{CONVST}$ line can go from a high to a low during the wake-up time, but the conversion will still not be initiated until after 1 µs. We recommend that conversion should not be initiated until at least 20 µs of the wake-up time has elapsed. This will ensure that the AD7492 has stabilized to within 0.5 LSB of the analog input value. After 1 µs, the AD7492 will have only stabilized to within approximately 3 LSB of the input value. From full sleep this wake-up time is typically 500 µs. In all cases the BUSY line will only go high once $\overline{CONVST}$ goes low. Superior power performance can be achieved in these modes of operation by waking up the AD7492 only to carry out a conversion. The optimum power performance is obtained when using full sleep mode as the ADC comparator, Reference buffer and Reference circuit is powered down. While in partial sleep mode, only the ADC comparator is powered down and the reference buffer is put into a low power mode. The 100 nF capacitor on the REF OUT pin is kept charged up by the reference buffer in partial sleep mode while in full sleep mode this capacitor slowly discharges. This explains why the wake-up time is shorter in partial sleep mode. In both sleep modes the clock oscillator circuit is powered down.

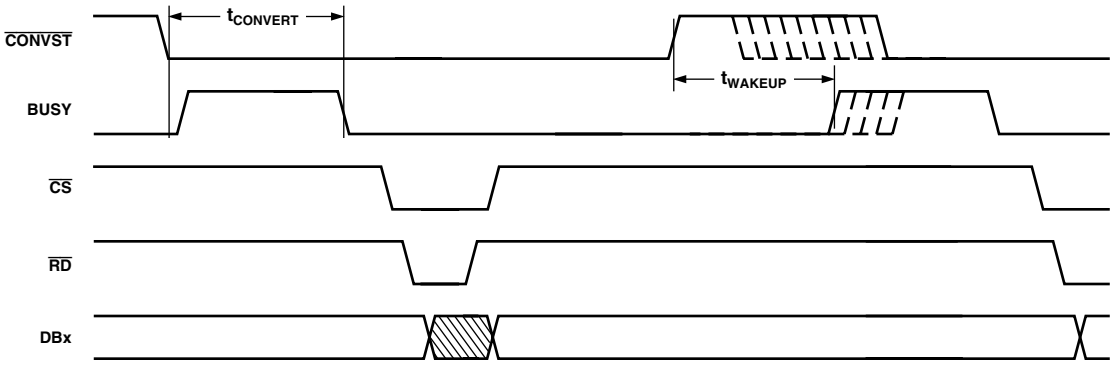


Figure 11. Mode 2 Operation

V_{DRIVE}

The V_{DRIVE} pin is used as the voltage supply to the digital output drivers and the digital input circuitry. It is a separate supply from AV_{DD} and DV_{DD}. The purpose of using a separate supply for the digital input/output interface is that the user can vary the output high voltage, V_{OH}, and the logic input levels, V_{INH} and V_{INL}, from the V_{DD} supply to the AD7492. For example, if AV_{DD} and DV_{DD} are using a 5 V supply, the V_{DRIVE} pin can be powered from a 3 V supply. The ADC has better dynamic performance at 5 V than at 3 V, so operating the part at 5 V, while still being able to interface to 3 V parts, pushes the AD7492 to the top bracket of high performance 12-bit A/Ds. Of course, the ADC can have its V_{DRIVE} and DV_{DD} pins connected together and be powered from a 3 V or 5 V supply. The trigger levels are $V_{DRIVE} \times 0.7$ and $V_{DRIVE} \times 0.3$ for the digital inputs.

The pins that are powered from V_{DRIVE} are DB0–DB11, $\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$, and BUSY.

PS/$\overline{FS}$ PIN

As previously mentioned, the PS/$\overline{FS}$ pin is used to control the type of power-down mode that the AD7492 can enter into if operated in Mode 2. This pin can be hardwired either high or low, or even controlled by another device. It is important to note that toggling the PS/$\overline{FS}$ pin while in power-down mode will not switch the part between partial sleep and full sleep modes. To switch from one sleep mode to another, the AD7492 will have to be powered up and the polarity of the PS/$\overline{FS}$ pin changed. It can then be powered down to the required sleep mode.

POWER-UP

It is recommended that the user performs a dummy conversion after power-up, as the first conversion result could be incorrect. This also ensures that the parts is in the correct mode of operation. The recommended power-up sequence is as follows:

1 > GND
2 > V_{DD}
3 > V_{DRIVE}
4 > Digital Inputs
5 > V_{IN}

Power vs. Throughput

The two modes of operation for the AD7492 will produce different power versus throughput performances, Mode 1 and Mode 2; see Operating Modes section of the data sheet for more detailed descriptions of these modes. Mode 2 is the Sleep Mode (Partial/Full) of the part and it achieves the optimum power performance.

Mode 1

Figure 12 shows the AD7492 conversion sequence in Mode 1 using a throughput rate of 500 kSPS. At 5 V supply the current consumption for the part when converting is 3 mA and the quiescent current is 1.8 mA. The conversion time of 880 ns contributes 6.6 mW to the overall power dissipation in the following way:

$$(880\ ns/2\ \mu s) \times (5 \times 3\ mA) = 6.6\ mW$$

The contribution to the total power dissipated by the remaining 1.12 µs of the cycle is 5.04 mW.

$$(1.12\ \mu s/2\ \mu s) \times (5 \times 1.8\ mA) = 5.04\ mW$$

Thus the power dissipated during each cycle is:

$$6.6\ mW + 5.04\ mW = 11.64\ mW$$

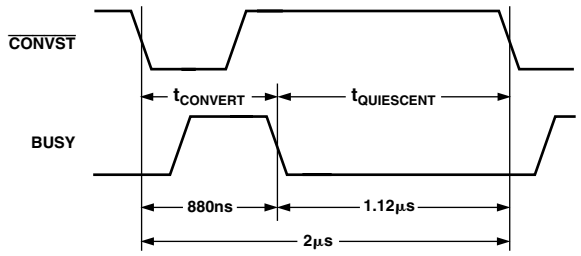


Figure 12. Mode 1 Power Dissipation

Mode 2 (Full Sleep Mode)

Figure 13 shows the AD7492 conversion sequence in Mode 2, Full Sleep mode, using a throughput rate of approximately 100 SPS. At 5 V supply the current consumption for the part when converting is 3 mA, while the full sleep current is 1 µA max. The power dissipated during this power-down is negligible and thus not worth considering in the total power figure. During the wake-up phase, the AD7492 will draw typically 1.8 mA. Overall power dissipated is:

$$(880\ ns/10\ ms) \times (5 \times 3\ mA) + (500\ \mu s/10\ ms) \times (5 \times 1.8\ mA) = 451.32\ \mu W$$

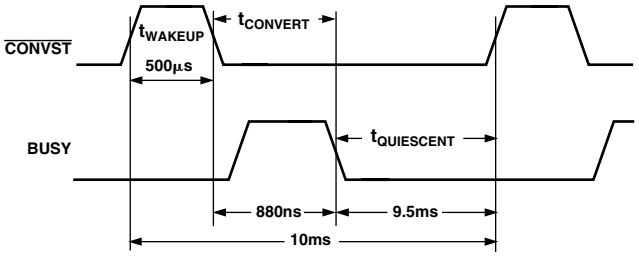


Figure 13. Full Sleep Power Dissipation

Mode 2 (Partial Sleep Mode)

Figure 14 shows the AD7492 conversion sequence in Mode 2, Partial Sleep mode, using a throughput rate of 1 kSPS. At 5 V supply the current consumption for the part when converting is 3 mA, while the partial sleep current is 250 µA max. During the wake-up phase, the AD7492 will draw typically 1.8 mA. Power dissipated during wake-up and conversion is :

$$(880\ ns/1\ ms) \times (5 \times 3\ mA) + (20\ \mu s/1\ ms) \times (5 \times 1.8\ mA) = 193.2\ \mu W$$

Power dissipated during power-down is:

$$(979\ \mu s/1\ ms) \times (5 \times 250\ \mu A) = 1.22\ mW$$

Overall power dissipated is:

$$193.2\ \mu W + 1.22\ mW = 1.41\ mW$$

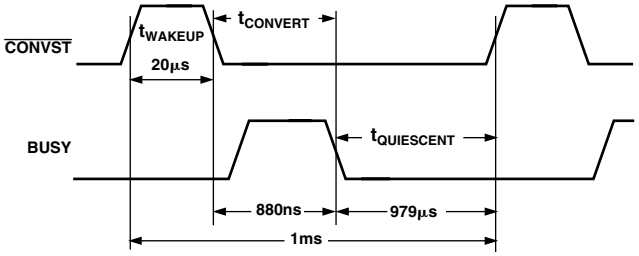


Figure 14. Partial Sleep Power Dissipation

Figure 15 to Figure 17 show a typical graphical representation of Power versus Throughput for the AD7492 when in (a) Mode 1 @ 5 V and 3 V, (b) Mode 2 in full sleep mode @ 5 V and 3 V and (c) Mode 2 in partial sleep mode @ 5 V and 3 V.

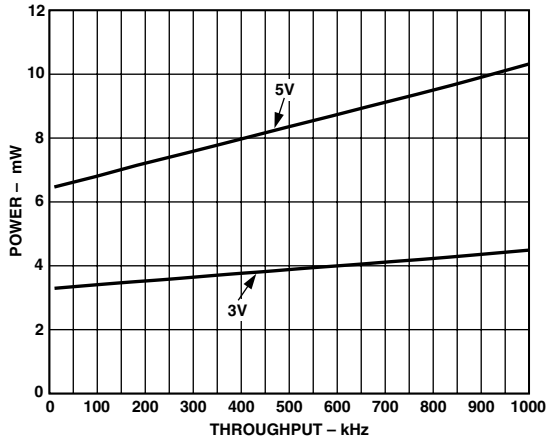


Figure 15. Power vs. Throughput (Mode 1 @ 5 V and 3 V)

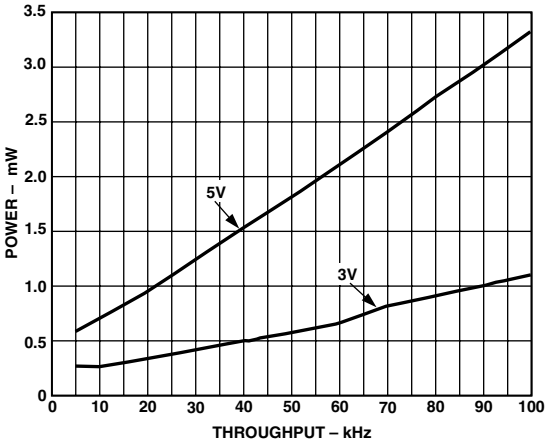


Figure 16. Power vs. Throughput (Mode 2 in Full Sleep Mode @ 5 V and 3 V)

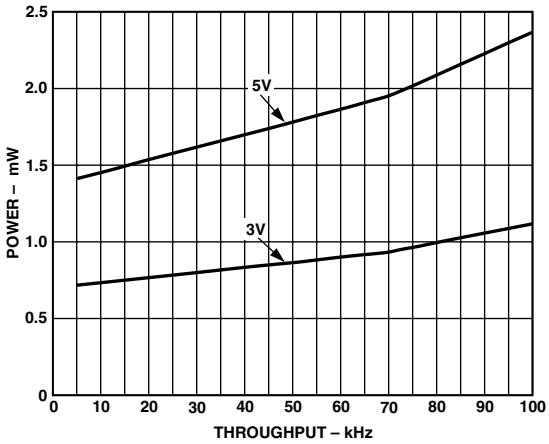


Figure 17. Power vs. Throughput (Mode 2 in Partial Sleep Mode @ 5 V and 3 V)

GROUNDING AND LAYOUT

The analog and digital power supplies are independent and separately pinned out to minimize coupling between analog and digital sections within the device. To complement the excellent noise performance of the AD7492 it is imperative that care be given to the PCB layout. Figure 18 shows a recommended connection diagram for the AD7492.

All of the AD7492 ground pins should be soldered directly to a ground plane to minimize series inductance. The AV_{DD}, DV_{DD}, and V_{DRIVE} pins should be decoupled to both the analog and digital ground planes. The REF OUT pin should be decoupled to the analog ground plane with a minimum capacitor value of 100 nF. This capacitor helps to stabilize the internal reference circuit. The large value capacitors will decouple low frequency noise to analog ground, the small value capacitors will decouple high frequency noise to digital ground. All digital circuitry power pins should be decoupled to the digital ground plane. The use of ground planes can physically separate sensitive analog components from the noisy digital system. The two ground planes should be joined in *only* one place and should not overlap so as to minimize capacitive coupling between them. If the AD7492 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point, that should be established as close as possible to the AD7492.

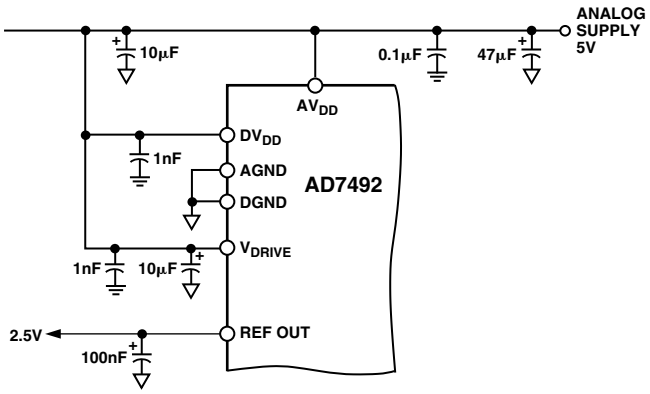


Figure 18. Typical Decoupling Circuit

Noise can be minimized by applying some simple rules to the PCB layout: analog signals should be kept away from digital signals; fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs; avoid running digital lines under the device as these will couple noise onto the die; the power supply lines to the AD7492 should use as large a trace as possible to provide a low impedance path and reduce the effects of glitches on the power supply line; avoid crossover of digital and analog signals and place traces that are on opposite sides of the board at right angles to each other.

Noise to the analog power line can be further reduced by use of multiple decoupling capacitors as shown in Figure 18. Decoupling capacitors should be placed directly at the power inlet to the PCB and also as close as possible to the power pins of the AD7492. The same decoupling method should be used on other ICs on the PCB, with the capacitor leads as short as possible to minimize lead inductance.

POWER SUPPLIES

Separate power supplies for AV_{DD} and DV_{DD} are desirable, but if necessary, DV_{DD} may share its power connection to AV_{DD}. The digital supply (DV_{DD}) must not exceed the analog supply (AV_{DD}) by more than 0.3 V in normal operation.

MICROPROCESSOR INTERFACING

AD7492 to ADSP-2185 Interface

Figure 19 shows a typical interface between the AD7492 and the ADSP-2185. The ADSP-2185 processor can be used in one of two memory modes, Full Memory Mode and Host Mode. The Mode C pin determines in which mode the processor works. The interface in Figure 19 is set up to have the processor working in Full Memory Mode, which allows full external addressing capabilities.

When the AD7492 has finished converting, the BUSY line requests an interrupt through the $\overline{IRQ2}$ pin. The $\overline{IRQ2}$ interrupt has to be set up in the interrupt control register as edge-sensitive. The DMS (Data Memory Select) pin latches in the address of the A/D into the address decoder. The read operation is thus started.

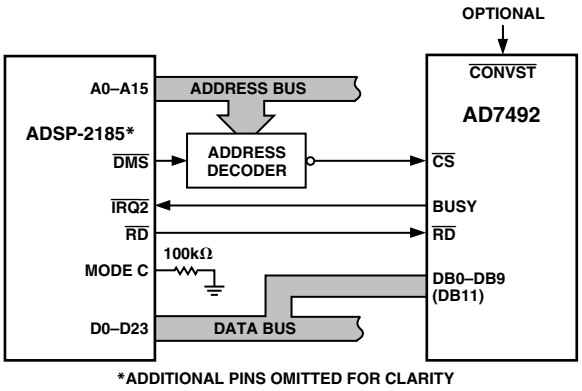


Figure 19. Interfacing to the ADSP-2185

AD7492 to ADSP-21065L Interface

Figure 20 shows a typical interface between the AD7492 and the ADSP-21065L SHARC® processor. This interface is an example of one of three DMA handshake modes. The $\overline{MS_X}$ control line is actually three memory select lines. Internal $ADDR_{25-24}$ are decoded into $\overline{MS_{3-0}}$, these lines are then asserted as chip selects. The $\overline{DMAR_1}$ (DMA Request 1) is used in this setup as the interrupt to signal end of conversion. The rest of the interface is standard handshaking operation.

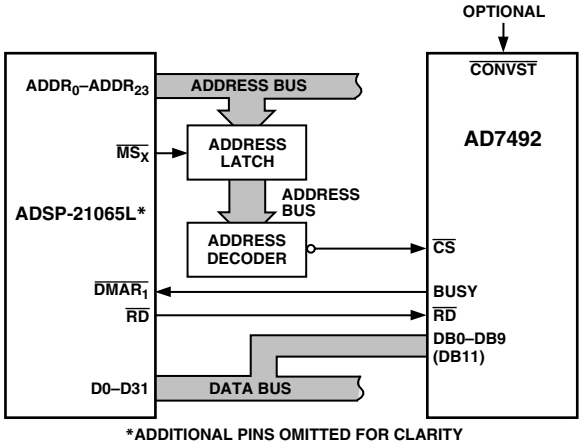


Figure 20. Interfacing to ADSP-21065L

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AD7492 to TMS320C25 Interface

Figure 21 shows an interface between the AD7492 and the TMS320C25. The $\overline{CONVST}$ signal can be applied from the TMS320C25 or from an external source. The BUSY line interrupts the digital signal processor when conversion is completed. The TMS320C25 does not have a separate $\overline{RD}$ output to drive the AD7492 $\overline{RD}$ input directly. This has to be generated from the processor $\overline{STRB}$ and R/$\overline{W}$ outputs with the addition of some glue logic. The $\overline{RD}$ signal is OR-gated with the $\overline{MSC}$ signal to provide the WAIT state required in the read cycle for correct interface timing. The following instruction is used to read the conversion from the AD7492:

IN D,ADC

where *D* is Data Memory address and the *ADC* is the AD7492 address. The read operation must not be attempted during conversion.

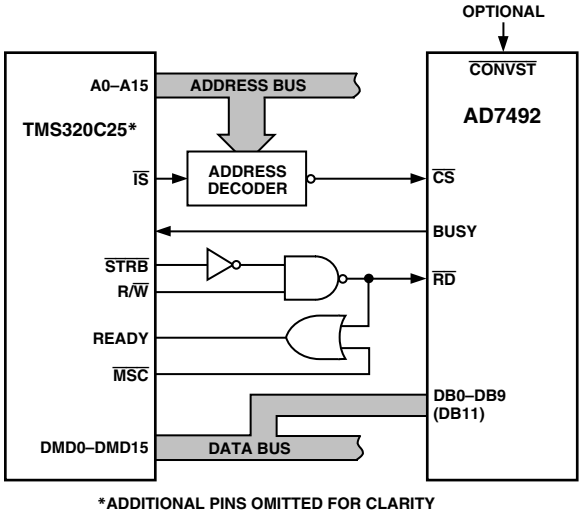


Figure 21. Interfacing to the TMS320C25

AD7492 to PIC17C4x Interface

Figure 22 shows a typical parallel interface between the AD7492 and PIC17C42/43/44. The microcontroller sees the A/D as another memory device with its own specific memory address on the memory map. The $\overline{CONVST}$ signal can either be controlled by the microcontroller or an external source. The BUSY signal provides an interrupt request to the microcontroller when a conversion ends. The INT pin on the PIC17C42/43/44 must be configured to be active on the negative edge. PORTC and PORTD of the microcontroller are bidirectional and used to address the AD7492 and also to read in the 12-bit data. The $\overline{OE}$ pin on the PIC can be used to enable the output buffers on the AD7492 and preform a read operation.

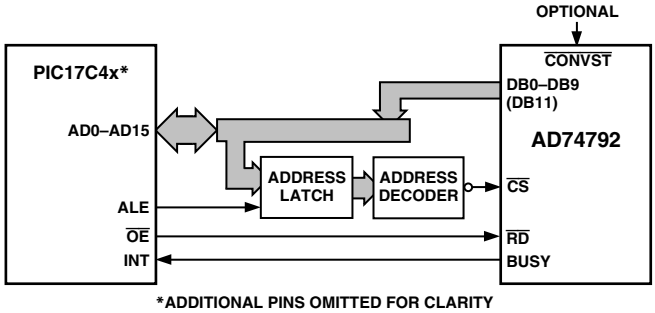


Figure 22. Interfacing to the PIC17C4x

AD7492 to 80C186 Interface

Figure 23 shows the AD7492 interfaced to the 80C186 microprocessor. The 80C186 DMA controller provides two independent high-speed DMA channels where data transfer can occur between memory and I/O spaces. (The AD7492 occupies one of these I/O spaces.) Each data transfer consumes two bus cycles, one cycle to fetch data and the other to store data.

After the AD7492 has finished conversion, the BUSY line generates a DMA request to Channel 1 (DRQ1). As a result of the interrupt, the processor performs a DMA READ operation which also resets the interrupt latch. Sufficient priority must be assigned to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80C186 processors.

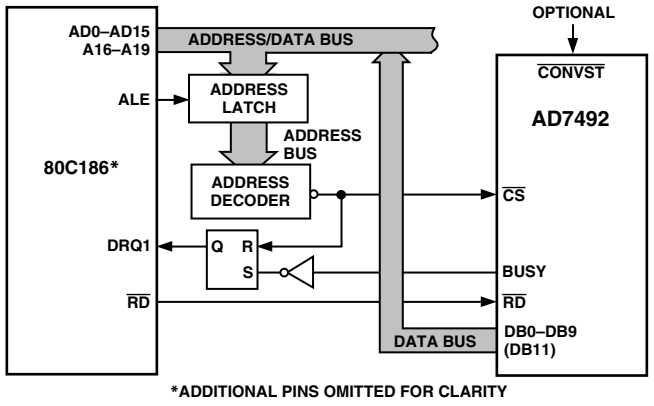
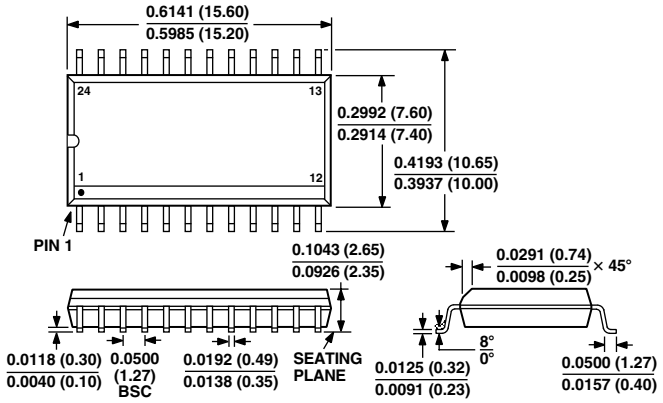


Figure 23. Interfacing to 80C186

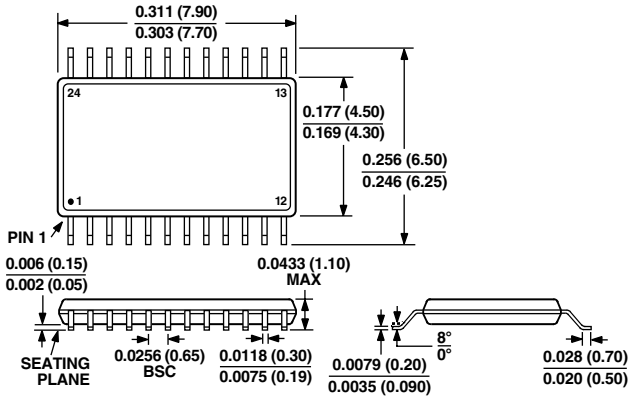
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead SOIC
(R-24)



24-Lead TSSOP
(RU-24)



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