

(Dual MC1741)
Internally Compensated, High
Performance Operational Amplifiers

The MC1747 and MC1747C were designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally and electrically equivalent to the μ A747 and μ A747C respectively.

- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability

Figure 1. High-Impedance, High-Gain Inverting Amplifier

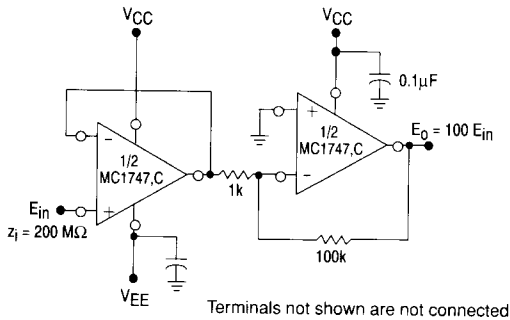
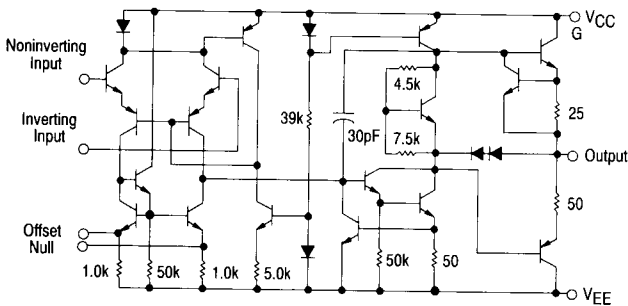


Figure 2. Circuit Schematic



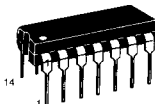
MC1747
MC1747C

(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

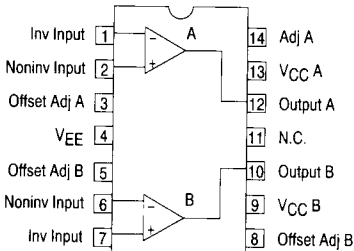


P2 SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1747L	-55° to +125°C	Ceramic DIP
MC1747CD		SO-14
MC1747CL	0° to +70°C	Ceramic DIP
MC1747CP2		Plastic DIP

MC1747, MC1747C

MAXIMUM RATINGS (TA = +25°C, unless otherwise noted.)

Rating	Symbol	MC1747	MC1747C	Unit
Power Supply Voltages	V _{CC} V _{EE}	+22 -22	+18 -18	V _{dc}
Differential Input Signal Voltages (Note 1)	V _{ID}	±30		V
Common Mode Input Swing Voltage (Note 2)	V _{ICR}	±15		V
Output Short Circuit Duration	t _{SC}	Continuous		
Voltage (Measurement between Offset Null and V _{EE})		±0.5		V
Operating Ambient Temperature Range	T _A	-55 to +125	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T _J	175 150		°C

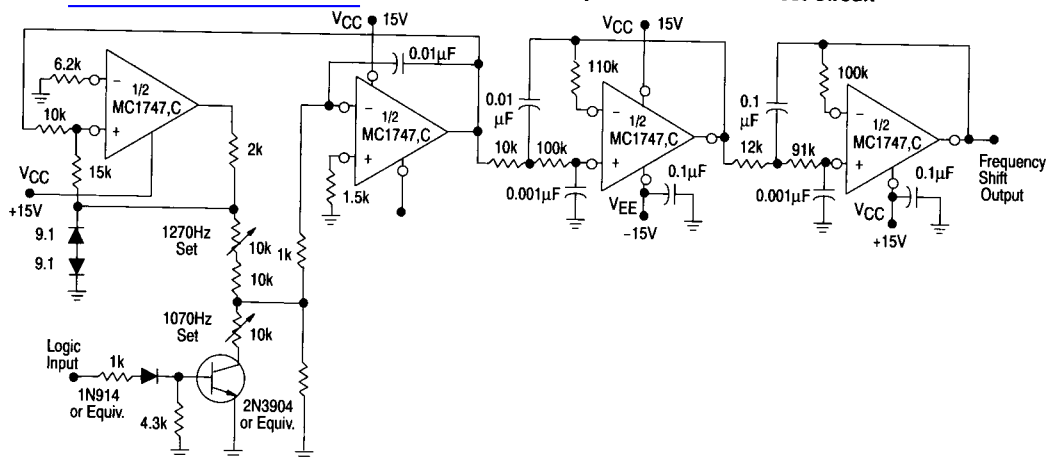
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	MC1747			MC1747C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current T _A = +25°C T _A = T _{high} (Note 3) T _A = T _{low} (Note 3)	I _{IB}	—	80 30 300	500 500 1500	—	80 30 30	500 800 800	nAdc
Input Offset Current T _A = +25°C T _A = T _{high} T _A = T _{low}	I _{IO}	—	20 7.0 85	200 200 500	—	20 7.0 7.0	200 300 300	nAdc
Input Offset Current T _A = +25°C T _A = T _{low} to T _A = T _{high}	V _{IO}	—	1.0 1.0	5.0 6.0	—	1.0 1.0	6.0 7.5	mVdc
Offset Voltage Adjustment Range		—	±15	—	—	±15	—	mV
Differential Input Impedance (Open-loop, f = 20 Hz)	r _i	0.3	2.0	—	0.3	2.0	—	MΩ
Parallel Input Resistance	C _i	—	1.4	—	—	1.4	—	pF
Common Mode Input Voltage Swing T _{low} ≤ T _A ≤ T _{high}	V _{ICR}	±12	±13	—	±12	±13	—	V
Common Mode Rejection (R _S = 10 kΩ) T _{low} ≤ T _A ≤ T _{high}	CMR	70	90	—	70	90	—	dB
Open-Loop Voltage Gain T _A = +25°C T _A = T _{low} to T _A = T _{high} (V _O = ±10 V, R _L = 2.0 kΩ)	A _{VOL}	50,000 25,000	200,000 —	— —	25,000 15,000	200,000 —	— —	V
Transient Response (Unity Gain) (V _{in} = 20 mV, R _L = 2.0 kΩ, C _L ≤ 100 pF) Rise Time Overshoot Percentage	t _{PLH}	—	0.3 5.0	— —	—	0.3 5.0	— —	μs %
Slew Rate (Unity Gain)	SR	—	0.5	—	—	0.5	—	V/μs
Output Impedance	z _o	—	75	—	—	75	—	Ω
Short Circuit Output Current	I _{SC}	—	25	—	—	25	—	mAdc
Channel Separation		—	120	—	—	120	—	dB
Output Voltage Swing (T _{low} ≤ T _A ≤ T _{high}) R _L = 10 kΩ R _L = 2.0 kΩ	V _{OR}	±12 ±10	±14 ±13	— —	±12 ±10	±14 ±13	— —	V _{pk}
Power Supply Rejection (T _{low} to T _{high}) V _{EE} = Constant, R _S ≤ 10 kΩ V _{CC} = Constant, R _S ≤ 10 kΩ	PSR+ PSR-	75 75	— —	— —	75 75	— —	— —	dB
Power Supply Current (each amplifier) T _A = +25°C T _A = T _{low} T _A = T _{high}	I _{CC,IEE}	— — —	1.7 2.0 1.5	2.8 3.3 2.5	— — —	1.7 2.0 2.0	2.8 3.3 3.3	mAdc
DC Power Consumption (each amplifier) T _A = +25°C T _A = T _{low} T _A = T _{high}	P _C	— — —	50 60 45	85 100 75	— — —	50 60 60	85 100 100	mW

- NOTES:**
- For supply voltages of less than ±15 V, the maximum differential input voltage is equal to ±(V_{CC} + |V_{EE}|).
 - For supply voltages of less than ±15 V, the maximum input voltage is equal to the supply voltage (+V_{CC}, -|V_{EE}|).
 - T_{low} = 0°C for MC1747CL T_{high} = +70°C for MC1747CL
-55°C for MC1747L +125°C for MC1747L

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Figure 8. Typical Frequency Shift Keyer Tone Generator Test Circuit



**Figure 4. Typical Frequency Shift Keyer
Tone Generator**

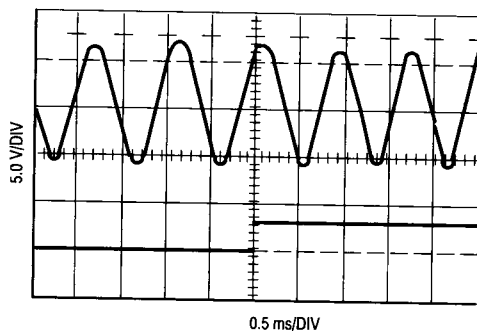


Figure 5. Open-Loop Voltage Gain versus Power-Supply Voltage

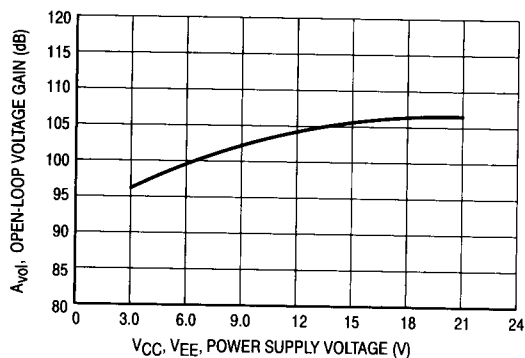
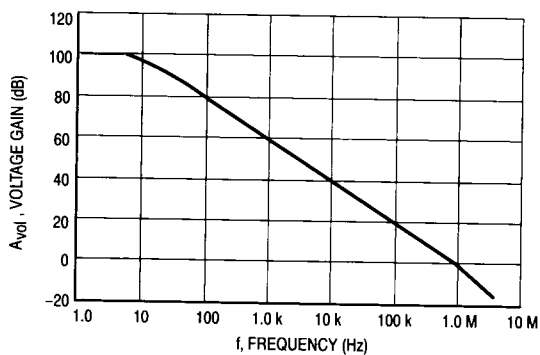


Figure 6. Open-Loop Frequency Response



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Figure 7. Power Bandwidth
(Large Signal Swing versus Frequency)

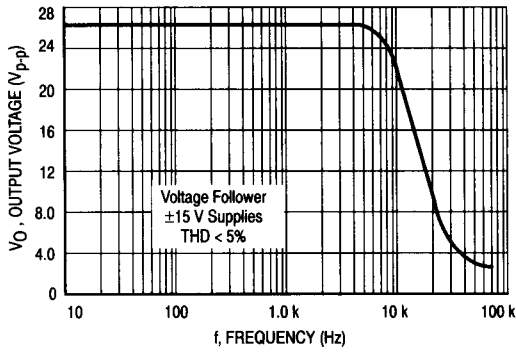


Figure 8. Power Consumption
versus Power Supply Voltage

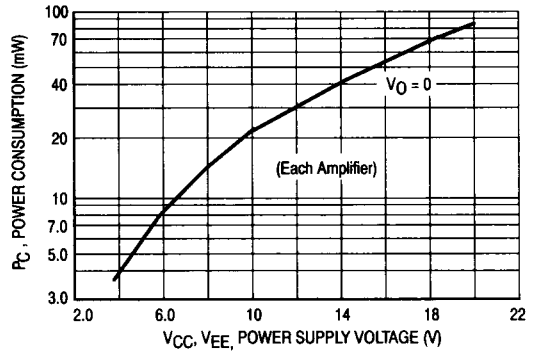


Figure 9. Output Voltage Swing
versus Load Resistance

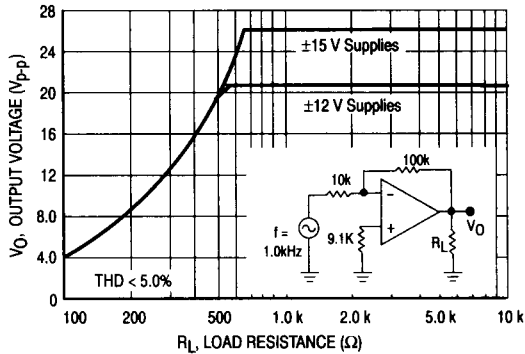


Figure 10. Output Noise versus Source Resistance

