

FEATURES
IQ Modulator with Integrated Fractional-N PLL
Output frequency range: 400 MHz to 1300 MHz
Internal LO Frequency Range: 750 MHz to 1160 MHz
Output P1dB: +14 dBm
Output IP3: +29 dBm
Noise Floor: -158 dBm/Hz
Baseband Modulation bandwidth: 500 MHz (3 dB)
SPI Serial Interface for PLL Programming
Power Supply: +5 V / 210 mA
40 Pin 6mm X 6mm LFCSP
GENERAL DESCRIPTION

The ADRF6701 is an IQ modulator with integrated PLL and VCO. The PLL/Synthesizer uses a Fractional-N PLL to generate a $2 \cdot F_{LO}$ input to the I-Q modulator. The PLL reference input is supported from 12MHz to 160MHz. The phase detector output controls a charge pump whose output is integrated in an off-chip loop-filter. The loop filter output is then applied to an integrated VCO. The VCO output at $2 \cdot F_{LO}$ is then applied to a quadrature divider as well as to a programmable divider. The programmable divider is controlled by a sigma-delta modulator (SDM). The I-Q modulator has analog I + Q inputs which can be at baseband or optionally at a complex IF up to 200 MHz

Table 1. Device Frequency Ranges

Part #	Internal LO Range	+/-3dB RF Out Balun Range	+/-1dB RF Out Balun Range
ADRF6701	750 MHz	400 MHz	550 MHz
	1160 MHz	1300 MHz	1000 MHz
ADRF6702	1550 MHz	1200 MHz	1550 MHz
	2150 MHz	2400 MHz	2200 MHz
ADRF6703	2100 MHz	1600 MHz	1900 MHz
	2600 MHz	2600 MHz	2400 MHz
ADRF6704	2500 MHz	2200MHz	2400 MHz
	2900 MHz	3000MHz	2800 MHz

The modulator mixes the I-Q inputs from the analog inputs with the quadrature LO from the quadrature divider. The differential output is converted to a single-ended output intended to drive a 50-Ohm load with good output return-loss characteristics.

The device is fabricated using an advanced silicon-germanium BiCMOS. It is available in a 40-lead, exposed-paddle, Pb-free, 6mm x 6mm LFCSP package. Performance is specified over a -40°C to $+85^{\circ}\text{C}$ temperature range.

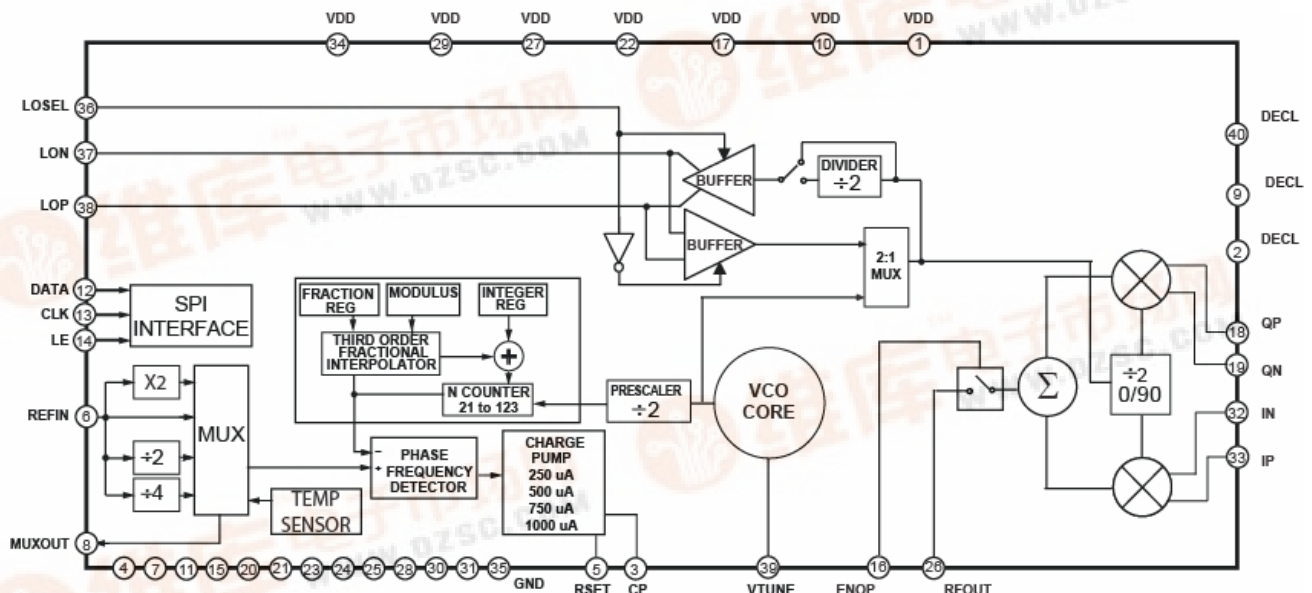


Figure 1. Block Diagram

Rev. PrE

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SPECIFICATIONS

VDD = 5 V; Ambient Temperature (T_A) = 25°C; I/Q inputs = 1 V p-p differential sine waves in quadrature on a 500 mV dc bias; FREF = 76.8 MHz, Modulator Baseband Frequency = 1 MHz, Output Frequency = 900 MHz, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
RF OUTPUT	Pin RFOUT				
Frequency Range		400		1300	MHz
Nominal Output Power	Baseband VIQ= 1 Vpp differential		+4		dBm
Output Harmonics	2 nd Harmonic		-80		dBc
	3 rd Harmonic		-55		dBc
Gain Flatness					
vs. Frequency	Pout=-7dBm, +/-5MHz		0.2		dB
	Pout=-7dBm, +/-40MHz		1.0		dB
vs. Temperature	-40C to +85C		1.0		dB
OP1dB			14		dBm
OIP3	F1 _{BB} = 3.5 MHz, F2 _{BB} = 4.5 MHz, P _{OUT} = -5 dBm per tone		29		dBm
OIP2	F1 _{BB} = 3.5 MHz, F2 _{BB} = 4.5 MHz, P _{OUT} = -5 dBm per tone		80		dBm
Carrier Feedthrough	at LO Frequency/2		-45		dBm
Sideband Suppression			-40		dBc
Noise Floor	All inputs tied to 0.5 V		-158		dBm/Hz
LO INPUT/OUTPUT	LOP, LON				
Output Frequency Range		750		1160	MHz
LO Output Level	2*LO or 1*LO Mode, Into a 50 Ω Load, LO Buffer Enabled		3		dBm
LO Input Level	Externally Applied 2XLO, PLL Disabled		0		dBm
LO Input Impedance	Externally Applied 2XLO, PLL Disabled		50		Ω
BASEBAND INPUTS	Pins IBBP, IBBN, QBBP, QBBN				
I and Q Input Bias Level			500		mV
Bandwidth	Combined bandwidth of baseband input an RF output				
3 dB			500		MHz
1dB			250		MHz
Input Impedance			1 1		k Ω pF
SYNTHESIZER SPECIFICATIONS	Synthesizer Specifications Referenced to the Modulator Output.				
Internal LO Range		750		1160	MHz
SPURS					
Channel Spurs	Offset from integer boundary. 100 KHz spur is at the half channel boundary and can exist in some cases				
	100kHz		-59		dBc
	200kHz		-64		dBc
	400kHz		-68		dBc
	800kHz		-72		dBc
Reference Spurs	Fref/2		-98		dBc
	Fref		-100		dBc
	>Fref		-100		dBc
LO HARMONICS					
	2 nd Harmonic		-26		dBc
	3 rd Harmonic		-16		dBc

Parameter	Conditions	Min	Typ	Max	Unit
PHASE NOISE	Frequency = 750 to 1160 MHz, PFD Frequency= 30.72 MHz or 38.4 MHz				
	@ 1 kHz to 10 kHz offset		-93		dBc/Hz
	@ 100 kHz offset		-109		dBc/Hz
	@ 500 kHz offset		-127		dBc/Hz
	@ 1 MHz offset		-135		dBc/Hz
	@ 5 MHz offset		-149		dBc/Hz
	@ 10 MHz offset		-156		dBc/Hz
	@ 20 MHz offset		-162		dBc/Hz
Normalized In-Band Phase Noise Floor			TBD		dBc/Hz
Integrated Phase Noise	1 KHz to 10 MHz integration bandwidth		0.5	1	°rms
Frequency Settling			1	2	ms
Phase Detector Frequency		20		40	MHz
REFERENCE CHARACTERISTICS	REFIN, REFOUT				
REFIN Input Frequency		12		160	MHz
REFIN Input Capacitance				4	pF
REFIN Input Current				±100	µA
REFOUT Output Swing	Load ≤ 5 pF (REFIN = 76.8 MHz), Load ≤ 10 pF (REFIN = 38.4 MHz)	0.25		2.7	V
REFOUT Duty Cycle		45		55	%
CHARGE PUMP					
Pump Current	Programmable to 250uA, 500uA, 750uA, 1000uA		500		uA
Output Compliance Range		1		2.8	Volts
LOGIC INPUTS	CLK, DATA, LE				
V _{INH} , Input High Voltage		1.4		3.3	V
V _{INL} , Input Low Voltage		0		0.7	V
I _{INH} /I _{INL} , Input Current			±TBD		µA
C _{IN} , Input Capacitance			TBD		pF
POWER SUPPLIES	Pins VDD				
Voltage Range		4.75	5	5.25	V
Supply Current	PLL only		80		mA
	Normal Tx Mode		210		mA
	Tx Mode with LO Buffer Enabled		260		mA
	Power Down Mode		100		uA

TIMING CHARACTERISTICS

Table 3.

Parameter	Limit	Unit	Test Conditions/Comments
t ₁	20	ns min	LE to CLK Setup Time
t ₂	10	ns min	DATA to CLOCK Setup Time
t ₃	10	ns min	DATA to CLOCK Hold Time
t ₄	25	ns min	CLOCK High Duration
t ₅	25	ns min	CLOCK Low Duration
t ₆	10	ns min	CLOCK to LE Setup Time
t ₇	20	ns min	LE Pulse Width

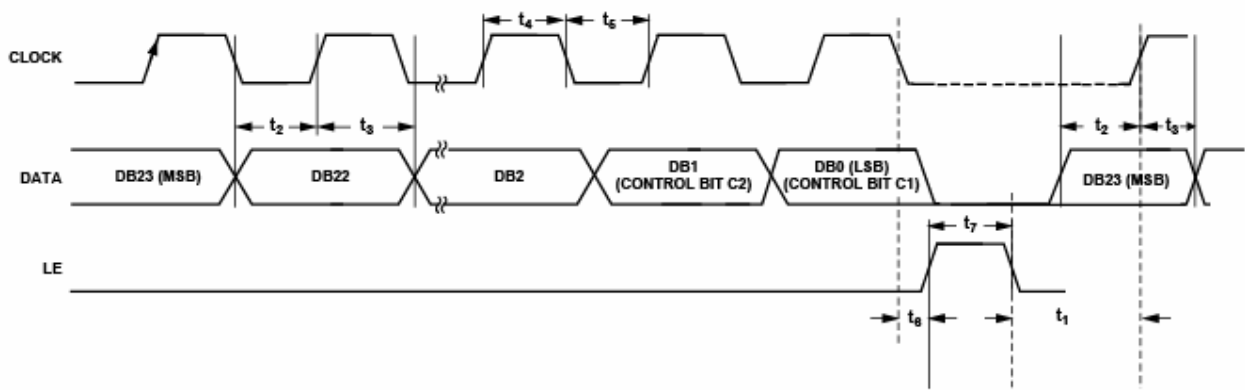


Figure2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage VCC, VCCbb, VCCrf	-0.5 to 6 V
Digital I/O CLK, DATA, LE	-0.3 to 3.3 V
IBBP, IBBN, QBBP, QBBN	TBD V
θ_{JA} (Exposed Paddle Soldered Down)	TBD °C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

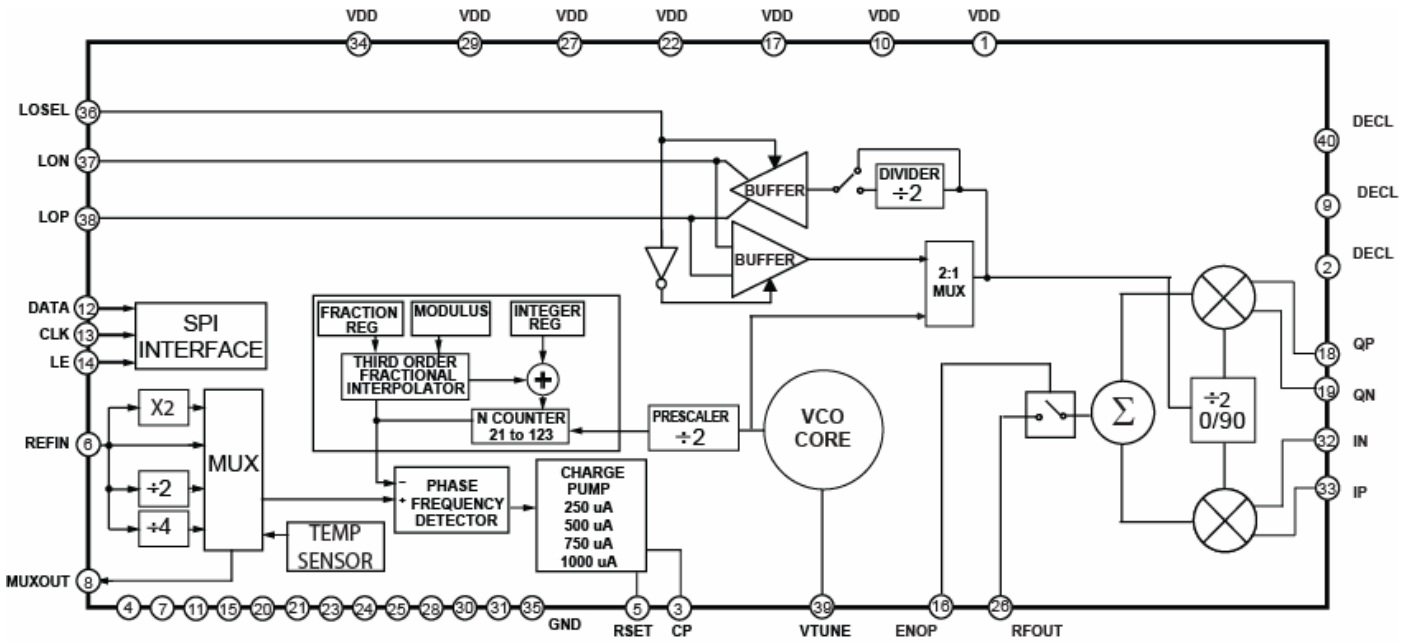


Figure 3. Block Diagram

Table 5. Pin Function Descriptions

Pin Nr.	Mnemonic	Description																														
1,10,17,22, 27,29,34	VDD	Power Supply: Power supply voltage range is 4.75 V to 5.25 V. Each pin should be decoupled with a 100 pf and 0.1uF capacitors located close to the pin.																														
2,9, 40	DECL	Internal Decoupling Nodes: Connect a 100 pF and a 0.1uF capacitor between each of these pins and ground.																														
3	CP	Charge Pump: Chargepump Output Pin. Connect to V _{TUNE} through loop filter																														
4, 7,11,15,20, 21,23,24,25,2 8,30,31,35	GND	Ground: Connect these pins to a low impedance ground planeGND																														
5	R _{SET}	<p>Charge Pump Current: The nominal charge pump current can be set to either 250 uA, 500 uA, 750 uA or 1 mA using DB10 and DB11 of Register 4 and by setting DB18 to 0 (Internal Reference Current). In this mode, no external R_{SET} is required. If DB18 is set to 1, the four nominal charge pump currents (I_{NOMINAL}) can be externally tweaked according to the equation.</p> $R_{SET} [\Omega] = \left[\frac{217.4 \times I_{CP, BASE}}{250} \right] - 37.8$ <p>Where I_{CP, BASE} is the base charge pump current in uA. For further details on the charge pump current, see Register 4 - Charge Pump, PFD and Reference Path Control.</p>																														
6	REFIN	Refence Input: Nominal input level is 1Vpp. Input range is 10 MHz to 160 MHz.																														
8	MUXOUT	Multiplexer Output: This output can be programmed to provide the Reference Output signal or the Lock Detect signal. The output is selected by programming the appropriate register.																														
12	DATA	Serial Data Input: The serial data input is loaded MSB first with the three LSBs being the control bits.																														
13	CLK	Serial Clock Input: This serial clock input is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. Maximum clock frequency is 20 MHz.																														
14	LE	Load Enable: When the LE input pin goes high, the data stored in the shift registers is loaded into one of the six registers, the relevant latch being selected by the first three control bits of the 24-bit word.																														
16	ENOP	<p>Modulator Output Enable/Disable</p> <table border="1"> <thead> <tr> <th>ENOP</th> <th>R5:DB6</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>0</td> <td>DISABLED</td> </tr> <tr> <td>0</td> <td>X</td> <td>DISABLED</td> </tr> <tr> <td>1</td> <td>1</td> <td>ENABLED</td> </tr> </tbody> </table>	ENOP	R5:DB6	Output	X	0	DISABLED	0	X	DISABLED	1	1	ENABLED																		
ENOP	R5:DB6	Output																														
X	0	DISABLED																														
0	X	DISABLED																														
1	1	ENABLED																														
18,19, 32,33	QP, QN, IN, IP	Modulator Baseband Inputs: Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs should be dc-biased to 0.5 V.																														
26	RFOUT	RF Output: Single-ended, 50 Ω internally biased RF output. RFOUT must be ac-coupled to its load.																														
36	LOSEL	<p>LO Select: This digital input pin determines whether the LOP and LON pins operate as inputs or outputs. LOP and LON become inputs if the LOSEL pin is set low AND the LDRV bit of Register 5 is set low. External LO drive must be a 2XLO. In addition to setting LOSEL and LDRV low and providing an external LO to the IQ Modulator. LON and LOP become outputs when LOSEL is high OR if the LDRV bit of Register 5 (DB3) is set high. A 1X or 2X LO output can be selected by setting the LDIV bit of Register 5 (DB5) to 1 or 0 respectively.</p> <table border="1"> <thead> <tr> <th>LON/LOP Function</th> <th>LOSEL</th> <th>R5:DB3 (LDRV)</th> <th>R5:DB5(LDIV)</th> <th>R5:DB4(LXL)</th> </tr> </thead> <tbody> <tr> <td>Input (2XLO)</td> <td>0</td> <td>0</td> <td>X</td> <td>1</td> </tr> <tr> <td>Output (1XLO)</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> </tr> <tr> <td>Output (1XLO)</td> <td>1</td> <td>X</td> <td>0</td> <td>X</td> </tr> <tr> <td>Output (2XLO)</td> <td>X</td> <td>1</td> <td>1</td> <td>X</td> </tr> <tr> <td>Output (2XLO)</td> <td>1</td> <td>X</td> <td>1</td> <td>X</td> </tr> </tbody> </table> <p>X = Don't Care LOSEL should not be left floating.</p>	LON/LOP Function	LOSEL	R5:DB3 (LDRV)	R5:DB5(LDIV)	R5:DB4(LXL)	Input (2XLO)	0	0	X	1	Output (1XLO)	X	1	0	X	Output (1XLO)	1	X	0	X	Output (2XLO)	X	1	1	X	Output (2XLO)	1	X	1	X
LON/LOP Function	LOSEL	R5:DB3 (LDRV)	R5:DB5(LDIV)	R5:DB4(LXL)																												
Input (2XLO)	0	0	X	1																												
Output (1XLO)	X	1	0	X																												
Output (1XLO)	1	X	0	X																												
Output (2XLO)	X	1	1	X																												
Output (2XLO)	1	X	1	X																												
37,38	LON, LOP	Local Oscillator Input/Output: The internally generated 1XLO or 2XLO is available on these pins. When internal LO generation is disabled, an external 1XLO or 2XLO can be applied to these pins.																														
39	VTUNE	VCO Control Voltage Input: This pin is driven by the output of the loop filter. Nominal input voltage range on this pin is 1.5 V to 2.5 V																														
	EP	Exposed Paddle: The exposed paddle should be soldered to a low impedance ground plane.																														

THEORY OF OPERATION

The ADRF6701 integrates a high performance IQ modulator with a state of the art fractional-N PLL. The PLL also integrates a low noise VCO. The programmable SPI port allows the user to control the fractional-N PLL functions and the modulator optimization functions as well as allowing for an externally applied LO or VCO.

The quadrature modulator core within the ADRF670X family is the next generation of industry leading family of modulators from Analog Devices. The baseband inputs are converted to currents and then mixed to RF using high-performance NPN transistors. The mixer output currents are transformed to a single-ended RF output using an integrated RF transformer balun. The high performance active mixer core, coupled with the low-loss RF transformer balun results in an exceptional OIP3 and OP1dB, with a very low output noise floor for excellent dynamic range. The use of a passive transformer balun rather than an active output stage leads to an improvement in OIP3 with no sacrifice in noise floor. Over the specified frequency range the four devices in the ADRF670X typically provide RF output P1dB of 15dBm, OIP3 of 30dBm, and RF output noise floor of -158dBm/Hz. Typical image rejection under these conditions is 40dB with no additional I and Q gain compensation.

The fractional divide function of the PLL allows the frequency multiplication value from REFIN to LO Out to be a fractional value rather than restricted to an integer as in traditional PLLs. In operation, this multiplication value is $INT + (FRAC/MOD)$ where INT is the integer value, FRAC is the fractional value and MOD is the modulus value, all programmable via the SPI port. In previous frac-N PLL designs, the fractional multiplication was achieved by periodically changing the fractional value in a deterministic way. The down side of this was often spurious components close to the fundamental signal. In the ADRF670x family, a sigma-delta modulator is used to distribute the fractional value randomly, thus significantly reducing the spurious content due to the fractional function.

BASIC CONNECTIONS FOR OPERATION

The device's seven power supply pins should be individually decoupled using 1000 pF and 0.1 μF capacitors located as close as possible to the device. In addition, internal decoupling nodes (labeled DECL) should be decoupled with the capacitor values shown.

The four IQ inputs should be driven with a bias level of 500 mV. A peak-to-peak differential swing on the I and Q inputs of 1 V (0.353 Vrms for a sinewave input) results in a single sideband output power of +4 dBm. The I and Q inputs are high impedance and should normally be terminated with resistors to provide an appropriate match to the baseband filter which immediately precedes the IQ modulator in the signal chain.

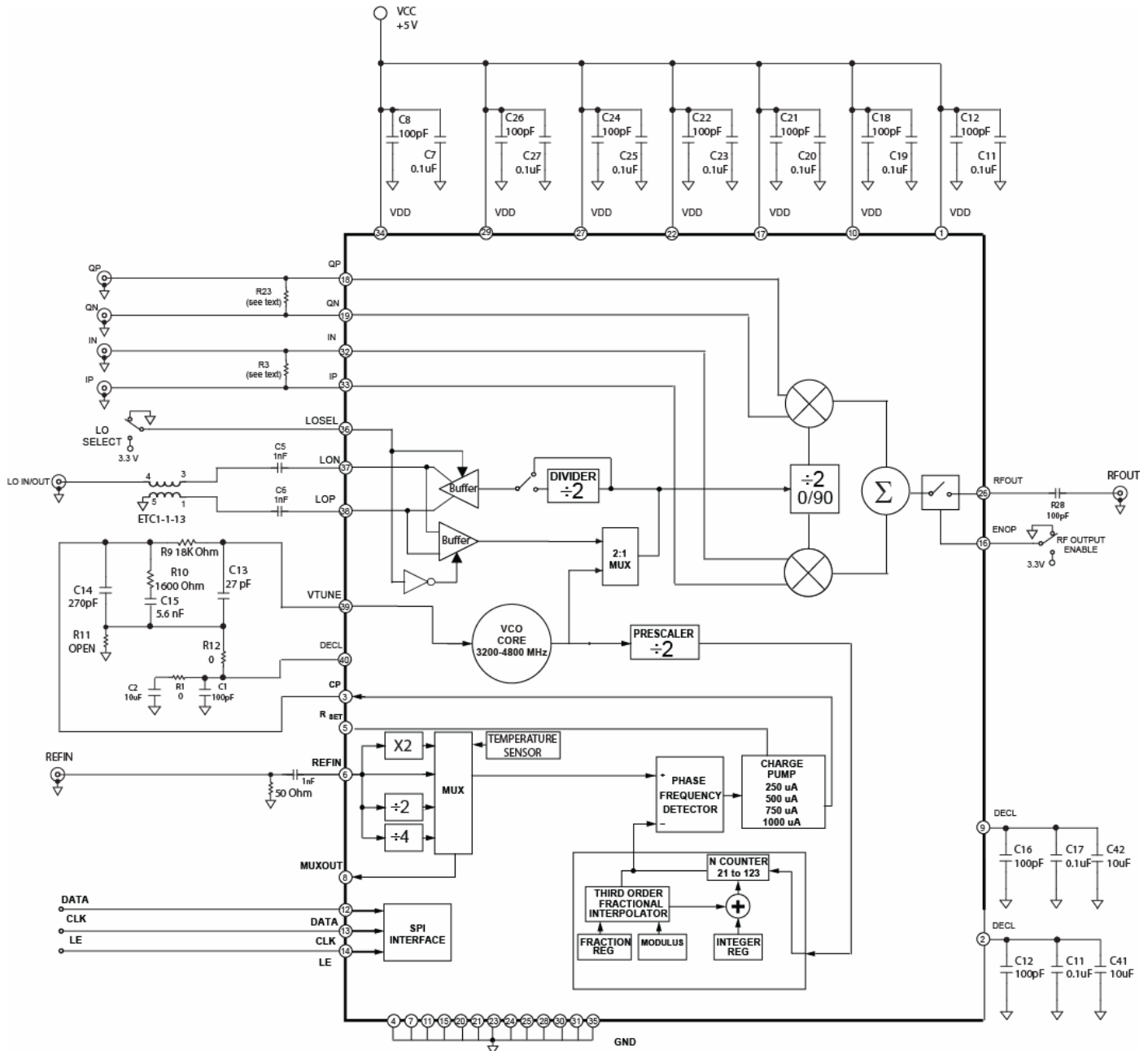


Figure 4. Basic Connections for Operation

DEVICE PROGRAMMING

Device programming is effected using a three pin SPI port. The description of timing requirements for the SPI port is given in Figure 2. There are eight programmable registers, each with 24 bits, controlling the operation of the device. The register functions can be broken down as follows;

Register 0 – Integer control for the PLL.

Register 1 – Modulus control for PLL.

Register 2 – Fractional control for PLL.

Register 3 – Sigma Delta Function

Register 4 – PLL Charge pump, PFD, reference path control

Register 5 – LO path and modulator control

Register 6 – VCO controls and VCO enable functions

Register 7 – Modulator bias enable, external VCO enable

Note - The PLL has internal calibration that must be run when the device is programmed with a given frequency. This calibration is automatically run whenever registers 0, 1, or 2 are programmed. Because the other registers affect PLL performance, the lower three registers should always be programmed last, preferably in the order 0, 1, 2.

Software is available on the Analog Devices website (www.analog.com) that allows easy programming from a PC running Windows XP™.

REGISTER 0 INTEGER DIVIDE CONTROL

With R0[2:0] set to 000, the on-chip integer divide control register is programmed as shown in figure 39.

INTEGER DIVIDE RATIO

The integer divide ratio is used to set the INT value in Equation 1. The INT, FRAC, and MOD values make it possible to generate output frequencies that are spaced by fractions of the PFD frequency. The VCO frequency (F_{VCO}) equation is:

$$F_{VCO} = 2 \times f_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

Where:

F_{VCO} is the output frequency of the internal VCO.

INT is the preset integer divide ratio value (24 to 119 in fractional mode).

MOD is the preset fractional modulus (1 to 2047).

FRAC is the preset fractional divider ratio value (0 to MOD-1).

DIVIDE MODE

Divide mode determines whether fractional mode or integer mode is used. In integer mode, the RF VCO output frequency (F_{VCO}) is calculated using the following equation:

$$F_{VCO} = 2 \times f_{PFD} \times (INT) \quad (2)$$

where INT is the integer divide ratio value (21 to 123 in integer mode).

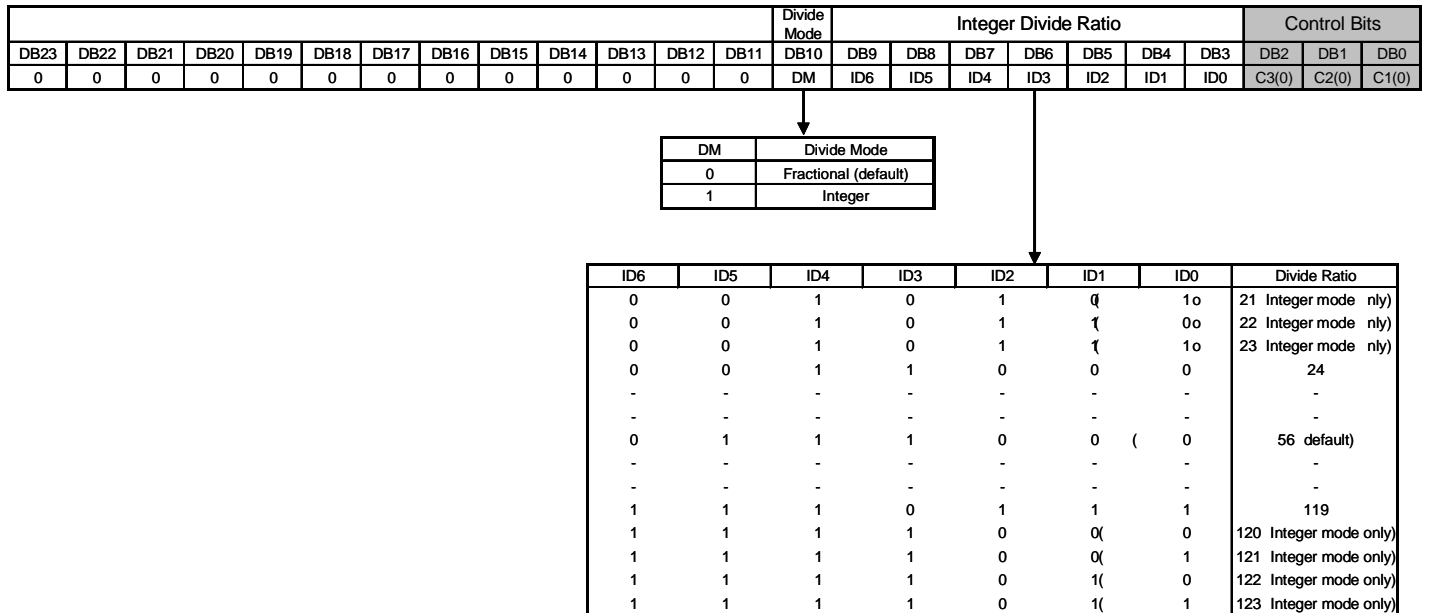


Figure 5. Integer Divide Control Register (R0)

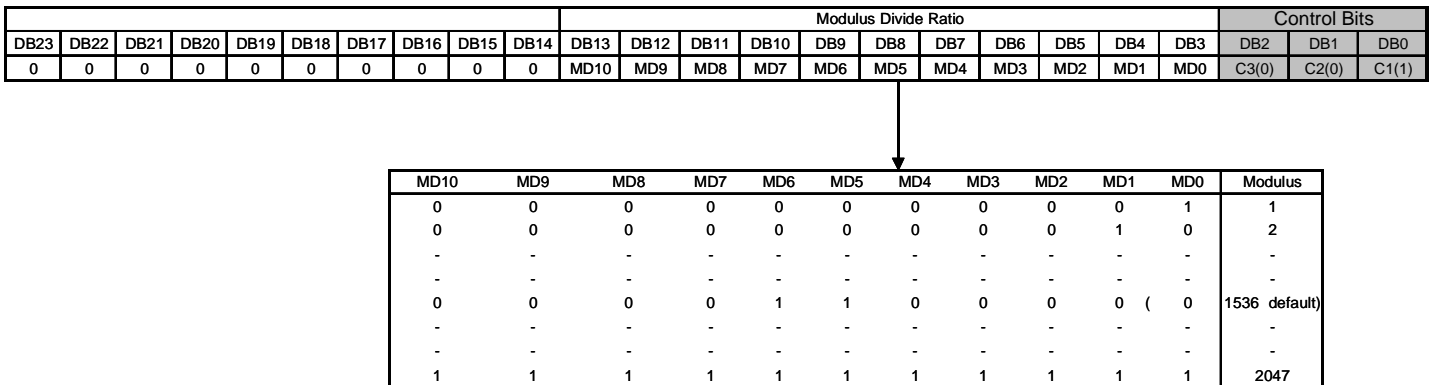


Figure 6. Modulus Divide Control Register (R1)

REGISTER 1—MODULUS DIVIDE CONTROL

With R1[2:0] set to 001, the on-chip modulus divide control register is programmed as shown in figure 40.

The MOD value is the preset fractional modulus ranging from 1 to 2047.

										Fractional Divide Ratio										Control Bits			
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	C3(0)	C2(1)	C1(0)

FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	Fractional Value
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-
0	1	1	0	0	0	0	0	0	0	0	768 (default)
-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-
Fractional Value must be less than Modulus											<MDR

Figure 7. Fractional Divide Control Register (R2)

REGISTER 2—FRACTIONAL DIVIDE CONTROL

With R2[2:0] set to 010, the on-chip fractional divide control register is programmed as shown in figure 41.

The FRAC value is the preset fractional modulus ranging from 0 to MOD-1.

Dither Magnitude		Dither Enable	Dither Restart Value																	Control Bits			
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	DITH1	DITH0	DEN	DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	C3(0)	C2(1)	C1(1)

DEN	Dither Enable
0	Disable (recommended)
1	Enable (default)

DITH1	DITH0	Dither Magnitude
0	0	15 (default)
0	1	7
1	0	3
1	1	1 (recommended)

DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	Dither Restart Value
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0x00001 (default)
.
.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0x1FFFF

Figure 8. Sigma Delta Modulator Dither Control Register (R3)

REGISTER 3—SIGMA DELTA MODULATOR DITHER CONTROL

With R3[2:0] set to 011, the on-chip sigma delta modulator dither control register is programmed as shown in figure 42.

The dither restart value can be programmed from 0 to 2¹⁷-1, though a value of 1 is typically recommended.

REGISTER 4—CHARGE PUMP, PFD AND REFERENCE PATH CONTROL

With R4[2:0] set to 100, the on-chip Charge Pump, PFD and Reference Path Control register is programmed as shown in figure 43.

The charge pump current is controlled by the base charge pump current ($I_{CP,BASE}$), and the value of the charge pump current multiplier ($I_{CP,MULT}$).

The base charge pump current can be set using an internal or external resistor (according to DB18 of Register 4). When using an external resistor, the value of $I_{CP,BASE}$ can be varied according to the following table.

$$R_{SET} [\Omega] = \left[\frac{217.4 \times I_{CP,BASE}}{250} \right] - 37.8$$

The actual charge pump current can be programmed to be a multiple (1, 2, 3, 4) of the charge pump base current. The multiplying value ($I_{CP,MULT}$) is equal to 1 plus the value of bits DB11 and DB10 in register 4.

The PFD phase offset multiplier ($\theta_{PFD,OFFS}$), which is set by bits DB16-DB12 of Register 4, will cause the PLL to lock with a nominally fixed phase offset between the PFD reference signal and the divided-down VCO signal. This phase offset is used to linearize the PFD-CP transfer function and can improve fractional spurs. The magnitude of the phase offset is determined by the following equation:

$$|\Delta\Phi| [\text{deg}] = 22.5 \frac{\theta_{PFD,OFFS}}{I_{CP,MULT}}$$

Finally, the phase offset can be either positive or negative depending on the value of DB17 in register 4.

The reference frequency applied to the PFD can be manipulated using the internal reference path source. The external reference frequency applied can be internally scaled in frequency by 2X, 1X, 0.5X, or 0.25X. This allows a broader range of reference frequency selections while keeping the reference frequency applied to the PFD within an acceptable range.

The ADRF6701 also provides a MUXOUT pin that can be programmed to output a selection of several internal signals. The default mode is to provide a lock-detect output to allow the user to verify when the PLL has locked to the target frequency. In addition, several other internal signals may be passed to the MUXOUT pin as described in figure 43.

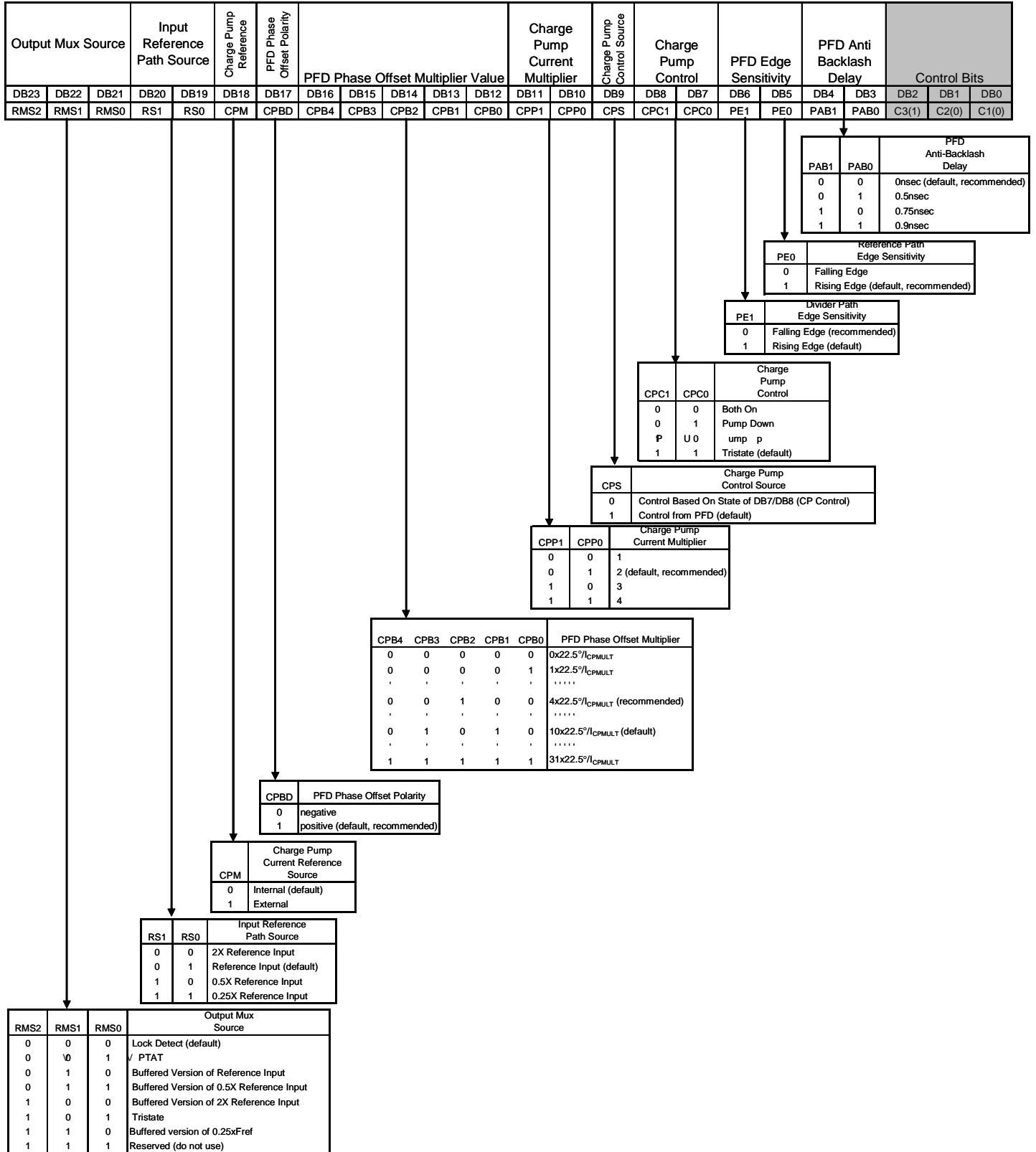


Figure 9. Charge Pump, PFD, and Reference Path Control Register (R4)

REGISTER 5 LO PATH AND MODULATOR CONTROL

The modulator output or the complete modulator can be disabled using the modulator bias enable and modulator output enable addresses of register 5.

The LO port (pins LOP and LON) can be used to apply an external 2X LO (i.e. bypass internal PLL) to the IQ Modulator. A differential LO drive of 0 dBm is recommended for best LO suppression at the RF output. When using an external frequency stable local oscillator signal to commutate the mixer core it is possible to shut down the PLL circuitry through the PLL enable address of register 5.

The LO port can also be used as an output where a 2X or 1X LO can be brought out and used to drive another mixer. The nominal output power provided at the LO port is +3 dBm.

The LO port's mode of operation is determined by the status of the LOSEL pin (3.3 V logic) along with the settings in a number of internal registers.

Table 6. LO Port Configuration

LON/LOP Function	LOSEL	R5:DB3 (LDRV)	R5:DB5 (LDIV)	R5:DB4(LXL)
Input (2XLO)	0	0	X	1
Output (1XLO)	X	1	0	X
Output (1XLO)	1	X	0	X
Output (2XLO)	X	1	1	X
Output (2XLO)	1	X	1	X

X = Don't Care

The device's internal VCO can also be bypassed. In this case, the charge pump output drives an external VCO through the loop filter. The loop is completed by routing the VCO in to the device through the LO Port.

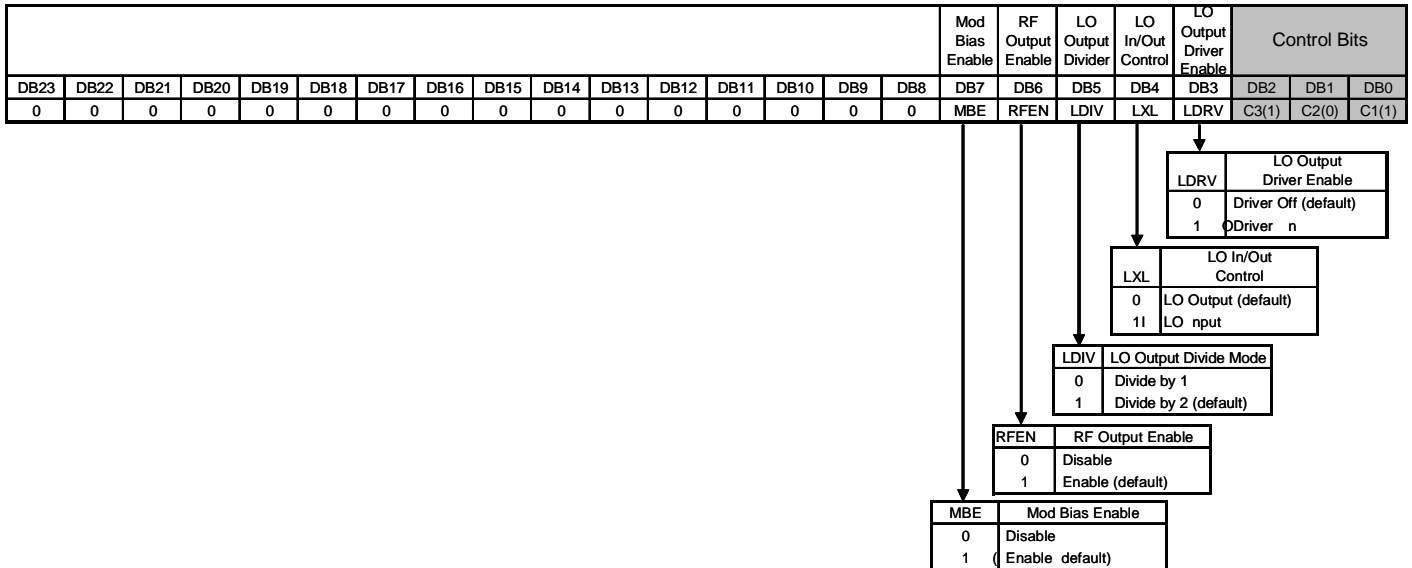


Figure 10. LO Path and Modulator Control (R5)

REGISTER 6 VCO CONTROL AND ENABLES

With R6[2:0] set to 110, the VCO Control and Enables register is programmed as shown in figure 16.

VCO band selection is normally selected based on BANDCAL calibration, though the user can directly select the VCO band using register 6. The VCO BS SRC determines whether the BANDCAL calibration will determine the optimum VCO tuning band, or if the external SPI interface will be used to select the VCO tuning band based on the value of the VCO Band Select.

The VCO amplitude can be controlled through register 6. The VCO amplitude setting can be controlled between 0 and 31 decimal, with a default value of 31.

The internal VCO can be disabled using register 6. The internal VCO LDO can be disabled if an external clean 2.5V supply is available to be applied to pins 9 and 16. Additionally the 3.3V on-board LDO can be disabled through register 6 and an external 3.3V supply can be applied to pin 2.

The internal charge pump can be disabled through register 6. Normally the charge pump will be enabled.

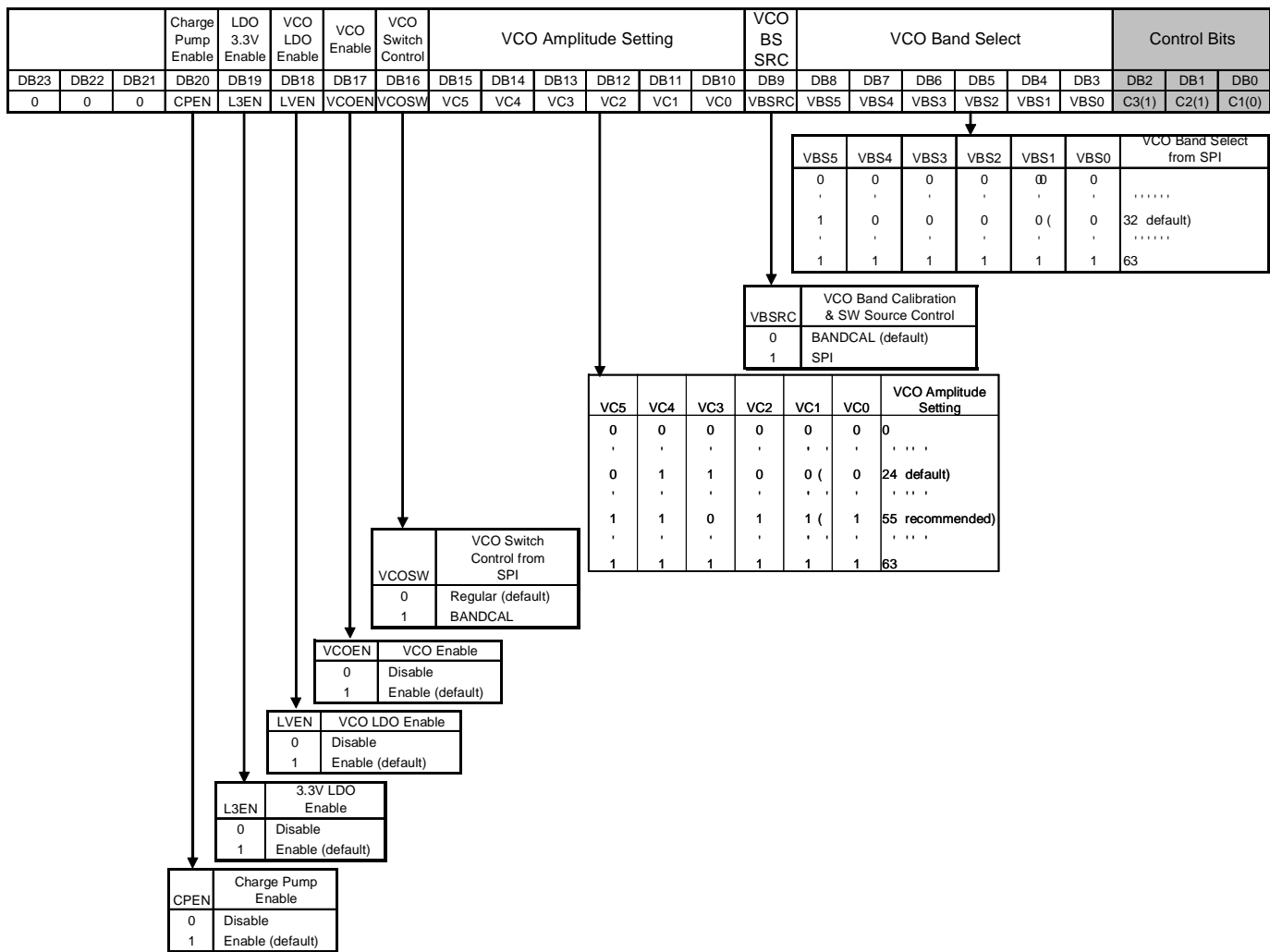


Figure 11. VCO Control and Enable(R6)

REGISTER 7 EXTERNAL VCO ENABLE

With R6[2:0] set to 111, the External VCO Control register is programmed as shown in figure 9.

The External VCO Enable bit allows the use of an external VCO in the PLL instead of the internal VCO. This can be advantageous in cases where the internal VCO is not capable of providing the desired frequency or where the internal VCO's

phase noise is higher than desired. By setting this bit (DB22) to 1, and setting Register 6, bits DB15-DB10 to 0, the internal VCO is disabled, and the output of an external VCO can be fed into the part differentially on pins 38,37 (LOP,LON). Since the loop filter is already external, the output of the loop filter simply needs to be connected to the external VCO's tuning voltage pin.

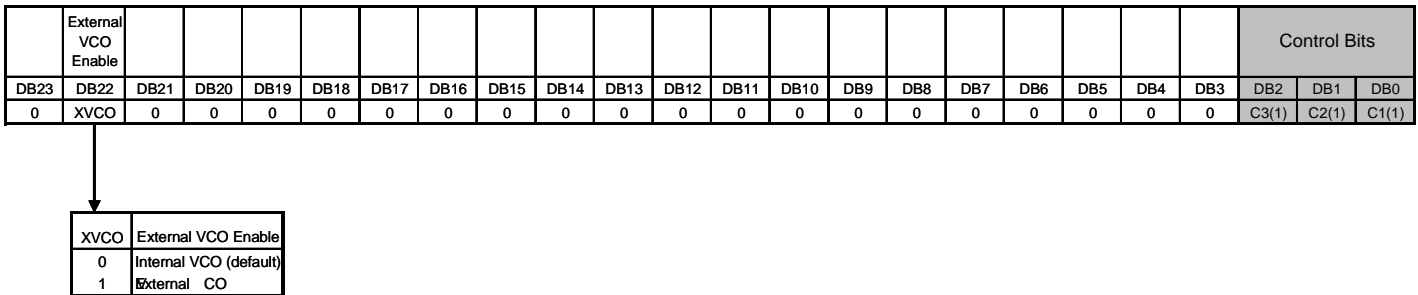
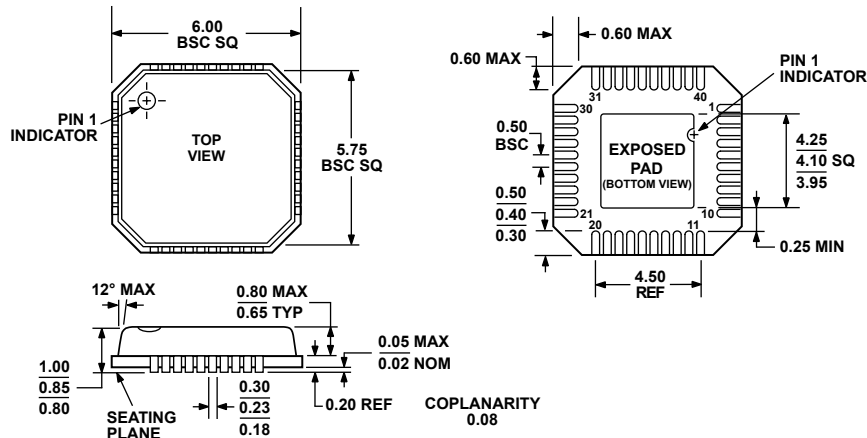


Figure 12. VCO Control and Enable (R7)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-2

072108-A

Figure 13. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
 6 x 6 mm Body, Very Thin Quad
 (CP-40-1)
 Dimensions shown in millimeters

Table 7. Ordering Guide

Model	Temperature Range (°C)	Package Description	Package Option
ADRF6701ACPZ ¹	-40 to +85	40-Lead Lead Frame Chip Scale Package	CP-40-1

¹ Z = RoHS Compliant Part