

For Serial/Voltage Output Type MOS Linear Image Sensors

The C4074 is a driver/amplifier circuit designed specifically for use with the serial/voltage output type MOS linear image sensors (S3921, S3924, S3922, S3923 series). The C4074 driver/amplifier circuit is simply constructed because the video-line integration in the MOS linear image sensors provides output signal with boxcar waveform. The C4074 includes a generator for a start pulse and two-phase clock pulses used to drive a MOS linear image sensor and an amplifier used to read out the video signal. The signal inputs required for the C4074 are only a master start pulse, master clock pulse, +5V and $\pm 15V$.

In addition, the C4091 pulse generator is available, which supplies the C4074 with a master start pulse and a master clock pulse.

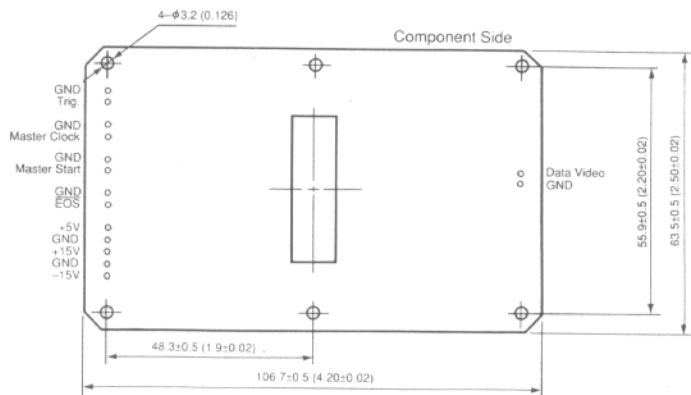
FEATURES

- Structure allows easy cooling and optical alignment of MOS image sensor.
- Simple operation: only a master start pulse, a master clock pulse, +5V and $\pm 15V$ required
- Low cost
- Wide dynamic range
- Simple adjustment

DESCRIPTIONS OF TERMINALS

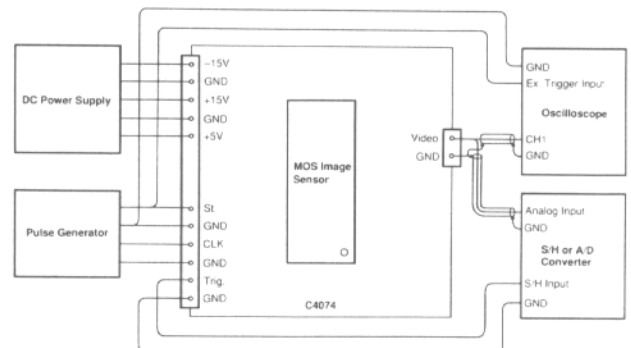
Terminals		Symbols	Descriptions
Input	Supply Voltage	$V_d (+5)$ $V_a (+15)$ (-15)	+5 Vdc, 70 mA +15 Vdc, 20 mA -15 Vdc, 20 mA
	Master Start ϕ_{ms}	St.	CMOS logic compatible. Positive logic. For initializing the circuit and the MOS shift register.
	Master Clock ϕ_{mc}	CLK	CMOS logic compatible. The maximum frequency is 3 MHz. For synchronizing the circuit and the MOS shift register.
Output	Data Video	Video	Positive polarity output. This is the amplified video output of the MOS image sensor, with the polarity inverted and the DC offset cancelled.
	Sample-and-hold	Trig.	CMOS logic compatible. Positive logic. This output can be used as the trigger signal for the sample-and-hold or A/D conversion.
	End of Scan	EOS	CMOS logic compatible. Negative logic. This is the end-of-scan signal of the MOS shift register and it is obtained synchronized with ϕ_2 right after the last element is scanned.

Figure 1: Dimensional Outline and Terminals



Dimensions in mm (inches)

Figure 2: Wiring Example



The diagram illustrates the MOS image sensor system. The MOS IMAGE SENSOR block includes inputs for ϕ_{st} (START), ϕ_1 (CLOCK 1), ϕ_2 (CLOCK 2), RESET ϕ (RESET ϕ), RESET V (V_{scd}) connected to +15V, EOS connected to 5V, ACTIVE VIDEO, and V_{scd} connected to +15V. The sensor's output is connected to an OP AMP. The OP AMP has a feedback resistor R_f (62k Ω) and a feedback capacitor C_f . The input resistor R_s (10k Ω) is connected to the ACTIVE VIDEO input. The OP AMP output is connected to the DATA VIDEO output. The OP AMP is also connected to a variable resistor VR, which is connected to +15V. A CONTROLLER block receives inputs from the sensor and provides outputs: MASTER START, MASTER CLOCK, TRIG., and EOS. The system is powered by +5V, GND, +15V, GND, and -15V.

The timing diagram illustrates the relationship between several signals and their timing parameters:

- MASTER CLOCK ϕ_{mc}** : A periodic square wave. Parameters shown are $t_{pw\phi_{mc}}$ (pulse width) and $f\phi_{mc}$ (frequency).
- MASTER START ϕ_{ms}** : A pulse. Parameters shown are $t_{pw\phi_{ms}}$ (pulse width).
- START ϕ_{st}** : A pulse. Parameter shown is $t_{pw\phi_{st}}$ (pulse width).
- CLOCK ϕ_1** : A square wave. Parameter shown is $t_{pw\phi_1}$ (pulse width).
- CLOCK ϕ_2** : A square wave. Parameter shown is $t_{pw\phi_2}$ (pulse width).
- RESET ϕ** : A square wave. Parameter shown is $t_{pw\phi_r}$ (pulse width).
- TRIG.**: A square wave. Parameters shown are $t_{tr\phi_{mc}}$ (rise time) and $t_{f\phi_{mc}}$ (fall time).
- VIDEO OUT**: A square wave.
- $\overline{EOS}$** : A square wave.

The diagram also includes a detailed view of the timing parameters for the TRIG. signal, showing $t_{tr\phi_{mc}}$, $t_{f\phi_{mc}}$, $t_{tr\phi_{ms}}$, and $t_{f\phi_{ms}}$.