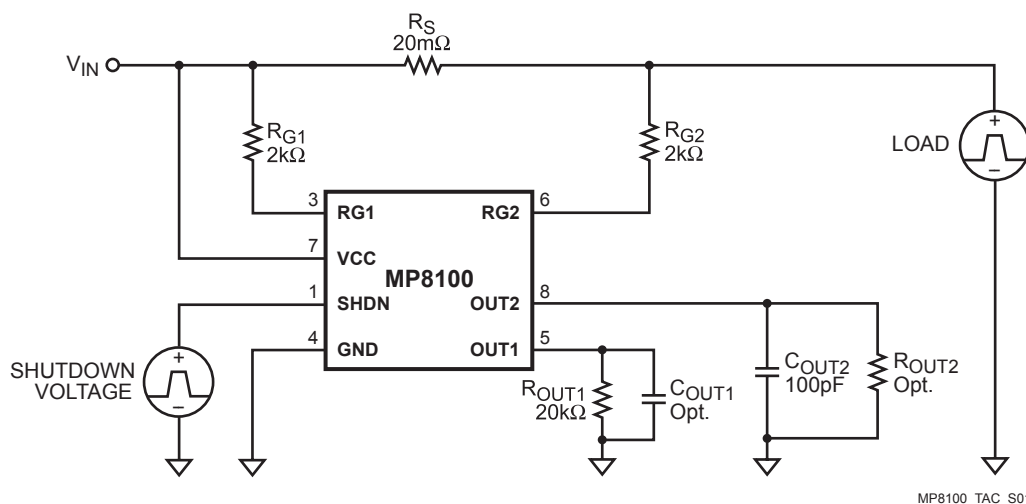




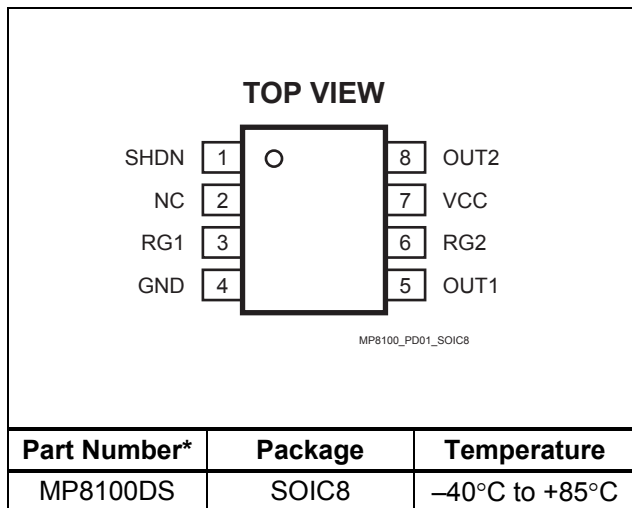
INITIAL RELEASE – SPECIFICATIONS SUBJECT TO CHANGE

Precision High-Side Current-Sense Amplifier



MP8100 TAC S01

PACKAGE REFERENCE



* For Tape & Reel, add suffix –Z (eg. MP8100DS–Z)
For Lead Free, add suffix –LF (eg. MP8100DS–LF–Z)

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

V_{CC}, RG1, RG2 to GND –0.3V to +20V
Maximum Differential Input Voltage, RG1 to RG2 5V
Storage Temperature –65°C to +150°C

Recommended Operating Conditions ⁽²⁾

V_{CC}, RG1, RG2 to GND 2.5V to 18V
Operating Temperature –40°C to +85°C

Thermal Resistance ⁽³⁾

θ_{JA} θ_{JC}
SOIC8 90 42... °C/W
Continuous Power Dissipation
(T_A=70°C) 800mW

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The device is not guaranteed to function outside of its operating conditions.
- 3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V, V_{SHDN} = 0V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V _{CC}		2.5		18	V
Supply Current	I _{CC}	I _{LOAD} = 0A; V _{CC} = 18V		17	30	μA
OUT1 Input Offset Voltage	V _{OS1}			0.25	1.20	mV
OUT2 Input Offset Voltage	V _{OS2}			0.25	1.20	mV
Input Bias Current	I _{RG1} , I _{RG2}			4		nA
OUT1 Current Accuracy	I _{RG1} /I _{OUT1}	V _{SENSE} = 100mV		±1		%
No-Load OUT1 Error		V _{SENSE} = 0V		1		μA
Low-Level OUT1 Error		V _{SENSE} = 5mV		2		μA
No-Load OUT2 Error		V _{SENSE} = 0V		1		μA
Low-Level OUT2 Error		V _{SENSE} = 5mV		2		μA
Power Supply Rejection Ratio	PSRR	2.5V < V _{CC} < 18V, V _{SENSE} = 100mV		0.05		%/V
Shutdown Supply Current	I _{CC(SHDN)}	V _{SHDN} = Float; V _{CC} = 18V		1	5	μA
SHDN Threshold Voltage	V _{TH_SHUTDOWN}		0.7	1.0	1.8	V
SHDN Input Low Current	I _{IL}			–300		nA
SHDN Input High Current	I _{IH}	V _{SHDN} = 3V		+500		nA
OUT1 Output Voltage Range	V _{OUT1}			V _{CC} – 0.15		V
OUT2 Output Voltage Range	V _{OUT2}			V _{CC} – 1		V

ELECTRICAL CHARACTERISTICS *(continued)* $V_{CC} = 10V$, $V_{SHDN} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUT1 Rise, Fall Time ⁽⁴⁾	t_R, t_F	$V_{SENSE} = 10mV$ to $150mV$, $R_{OUT1} = 10k\Omega$, $R_{G1} = R_{G2} = 2k\Omega$, $C_{OUT1} = 50pF$, 10% to 90%		TBD		μs
OUT2 Rise, Fall Time ⁽⁴⁾	t_R, t_F	$V_{SENSE} = 10mV$ to $150mV$, $R_{OUT2} = 100k\Omega$, $R_{G1} = R_{G2} = 2k\Omega$, $C_{OUT2} = 100pF$, 10% to 90%		TBD		μs
Maximum OUT1 Current ⁽⁴⁾	I_{OUT1}			500		μA
Maximum OUT2 Current ⁽⁴⁾	I_{OUT2}			5		mA

Notes:

4) Guaranteed by design.

5) Input common mode range cannot exceed the supply voltage.

PIN FUNCTIONS

Pin #	Name	Description
1	SHDN	Shutdown. Connect to ground for normal operation. When high, supply current is less than $5\mu A$.
2	NC	Not Connected.
3	RG1	Gain Resistor. Connect to battery side of current-sense resistor through the gain resistor.
4	GND	Ground or Battery Negative Terminal.
5	OUT1	Output For Driving Resistive Loads.
6	RG2	Gain Resistor. Connect to load side of current-sense resistor through the gain resistor.
7	VCC	Power Input. Connect to Battery Input.
8	OUT2	Output For Driving Capacitive Loads.

OPERATION

The MP8100 is a current-sense amplifier with a wide operating input voltage range of 2.5V to 18V.

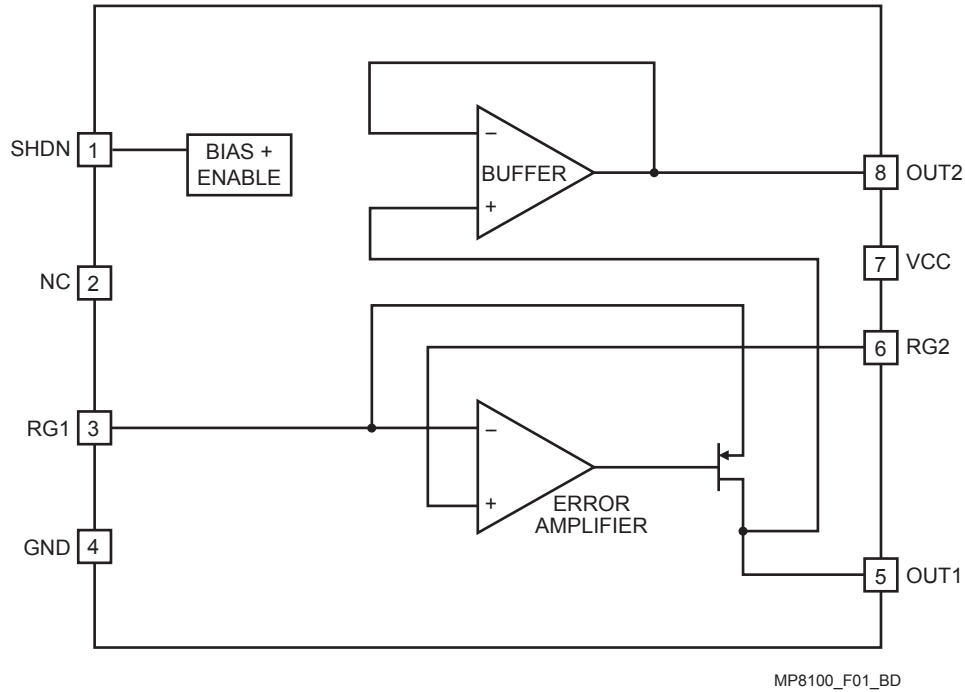


Figure 1—Functional Block Diagram

APPLICATION INFORMATION

COMPONENT SELECTION

Table 1—Suggested Component Values

Full-Scale Load Current, I_{SENSE} (A)	Current Sense Resistor (mΩ)	Gain Setting Resistor (kΩ) ($R_{G1} = R_{G2}$)	R_{OUT1} (kΩ)	Gain
0.1	500	2	20	10
1	50	2	20	10
5	10	2	20	10
10	5	2	20	10

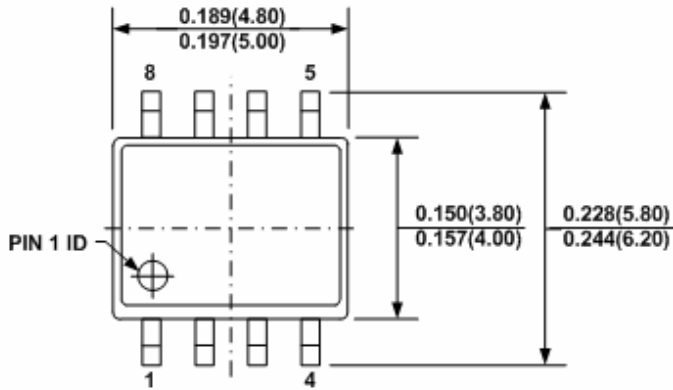
The value of V_{OUT1} can be obtained with the equation:

$$V_{OUT} = \frac{I_L \times R_S \times R_{OUT1}}{R_{G1}} = I_L \times R_S \times \text{Gain}$$

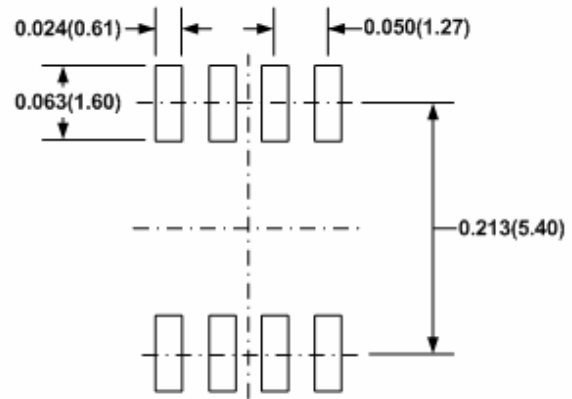
Where R_{G1} is the sense resistor and I_L is the load current.

PACKAGE INFORMATION

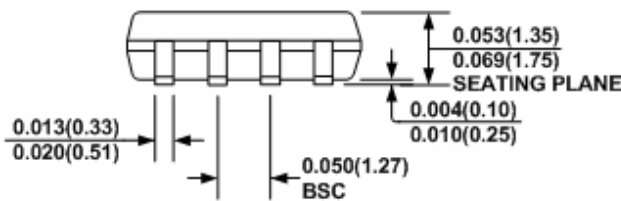
SOIC8



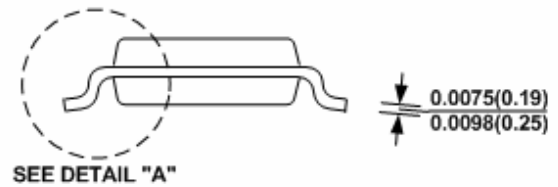
TOP VIEW



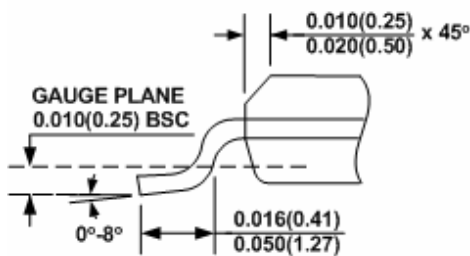
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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