



CMOS 12-Bit Monolithic Multiplying DAC

AD7541

T-51-09-12

1.1 Scope.

This specification covers the detail requirements for a 12-bit monolithic CMOS multiplying digital-to-analog converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7541S(X)/883B
-2	AD7541T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D18	18-Pin Side-Brazed Ceramic
Q	Q18	18-Pin Cerdip
E	E20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} to GND		+17V
V_{REF} to GND		$\pm 25\text{V}$
Digital Input Voltage Range		V_{DD} to GND
Output Voltage (Pin 1, Pin 2)		-0.3V to V_{DD}
Power Dissipation		
Up to $+50^\circ\text{C}$		1000mW
Derates above $+50^\circ\text{C}$		10mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{jc} = 35^\circ\text{C/W}$ for D18, Q18 and E20A
 $\theta_{ja} = 120^\circ\text{C/W}$ for D18, Q18 and E20A

AD7541 — SPECIFICATIONS

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Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2	12					Bits
Relative Accuracy	RA	-1	1	1	1			± LSB max
		-2	1/2	1	1/2	1/2		
Gain Error ²	AE	-1, 2	16.7	12.5	16.7			± LSB max
Gain Tempco	TC _{AE}	-1, 2	13					± ppm/°C max
Power Supply Rejection	PSRR	-1, 2	0.02	0.01	0.02		$V_{DD} = 14.5V$ to $15.5V$	± % per % max
Output Leakage Current Pin 1	I _{OUT1}	-1, 2	200	50	200		Digital Inputs = V_{IL} $V_{REF} = +10V$	± nA max
Pin 2	I _{OUT2}	-1, 2	200	50	200		Digital Inputs = V_{IH} $V_{REF} = +10V$	± nA max
Output Current Settling Time		-1, 2	1				$T_O \pm 1/2LSB$, $R_{OUT1} = 100\Omega$, $C_{OUT1} = 13pF$ Digital Inputs = V_{IH} to V_{IL} or V_{IL} to V_{IH}	µs max
Feedthrough Error ³	FT	-1, 2	1				$V_{REF} = 20V$ p-p at 10kHz	mV p-p max
Reference Input Resistance	R _{IN}	-1, 2	5	5	5			kΩ min
		-1, 2	20	20	20			kΩ max
Digital Input High Voltage	V _{IH}	-1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	-1, 2	1	1	1		$V_{IN} = 0V$ or $15V$	± µA max
Digital Input Capacitance	C _{IN}	-1, 2	8					pF max
Output Capacitance	C _{OUT1}	-1, 2	200				Digital Inputs = V_{IH}	pF max
		-1, 2	60				Digital Inputs = V_{IH}	pF max
	C _{OUT2}	-1, 2	60				Digital Inputs = V_{IL}	pF max
		-1, 2	200				Digital Inputs = V_{IL}	pF max
Supply current from V_{DD}	I _{DD}	-1, 2	2	2	2		Digital Inputs = V_{IH} or V_{IL}	mA max

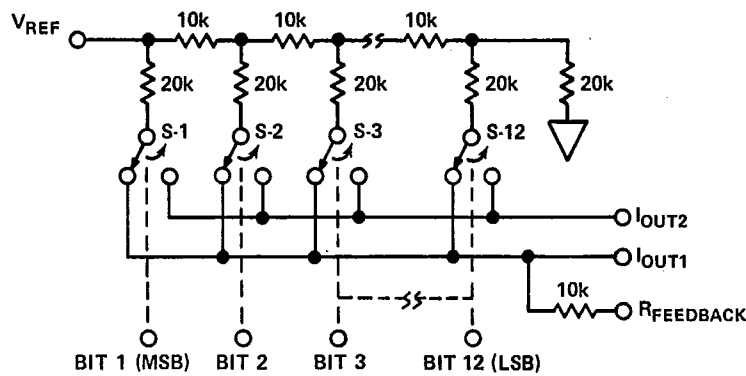
NOTES

¹ $V_{DD} = +15V$; $V_{OUT1} = V_{OUT2} = 0V$; $V_{REF} = +10V$ unless otherwise stated.

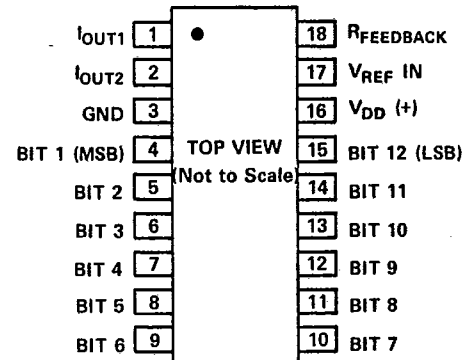
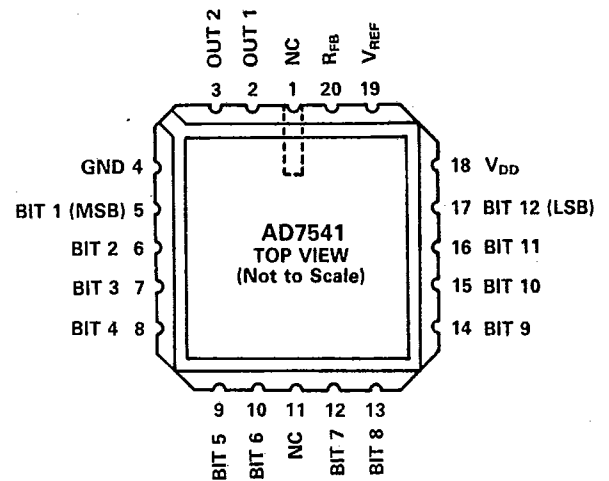
²Measured using internal feedback resistor and includes effect of leakage current and gain TC.

³Feedthrough error can be reduced by connecting the lid of the ceramic package to ground.

Table 1.

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AD7541**3.2.1 Functional Block Diagram and Terminal Assignments.**

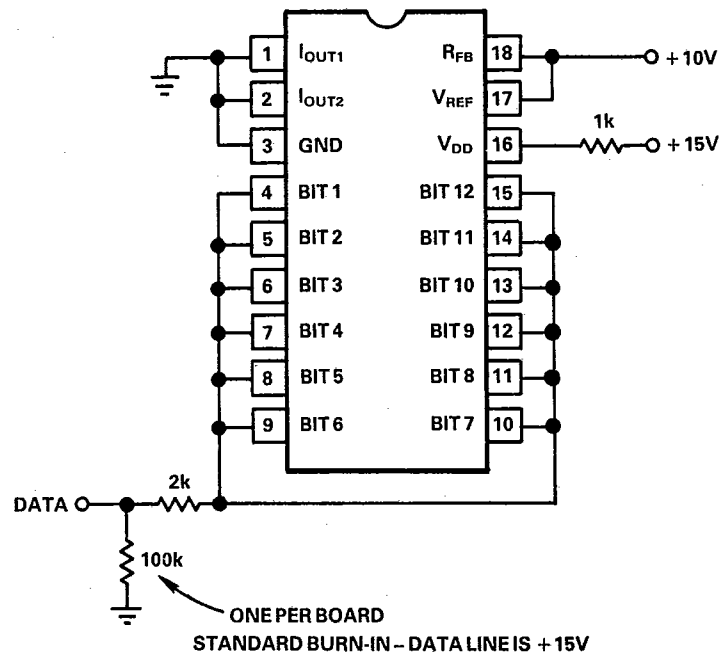
DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.**EPACKAGE (LCC)****3.2.4 Microcircuit Technology Group.**

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



REV.B.