February 2006

LM4982 Boomer® Audio Power Amplifier Series

Ground-Referenced, Ultra Low Noise, 80mW Stereo Headphone Amplifier with IntelliSense and I2C Volume Control

General Description

The LM4982 is a ground referenced, variable gain audio power amplifier capable of delivering 80mW of continuous average power into a 16Ω single-ended load with less than 1% THD+N from a 3V power supply. The I^2C volume control allows +18 to -76 dB gain settings.

The LM4982 utilizes advanced charge pump technology to generate the LM4982's negative supply voltage. This eliminates the need for output-coupling capacitors typically used with single-ended loads.

IntelliSense is a new circuit technology that allows the LM4982 to detect whether a mono or stereo headphone plug has been inserted into the output jack.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4982 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4982 incorporates selectable low-power consumption shutdown and channel select modes.

The LM4982 contains advanced pop & click circuitry that eliminates noises which would otherwise occur during turn-on and turn-off transitions.

Key Specifications

- Improved PSRR at 217Hz 66dB
- Stereo Output Power at V_{DD} = 3V, R_L = 32Ω, THD+N = 1% 51mW (typ)
- Shutdown current 0.1µA (typ)

Features

- Ground referenced outputs
- I^2C Volume and mode controls
- Available in space-saving micro SMD package
- Ultra low current shutdown mode
- Advanced pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 1.6 – 4.0V operation
- No output coupling capacitors, snubber networks, bootstrap capacitors or gain-setting resistors required
- Mono/Stereo headphone detect

Applications

- Notebook PCs
- Desktop PCs
- Mobile Phones
- PDAs
- Portable electronic devices
- MP3 Players

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LM4982 Ground-Referenced, Ultra Low Noise, 80mW Stereo Headphone Amplifier with IntelliSense and I2C Volume Control

Typical Application

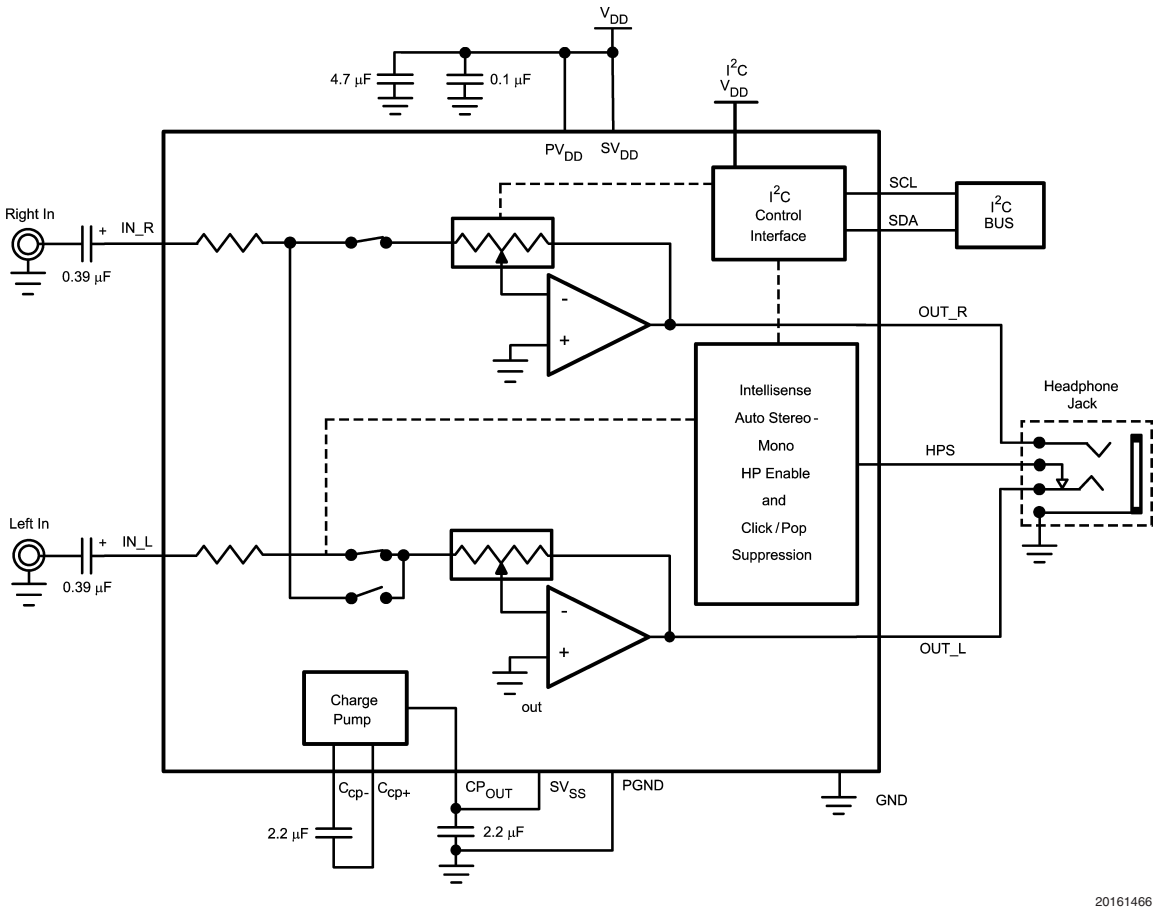
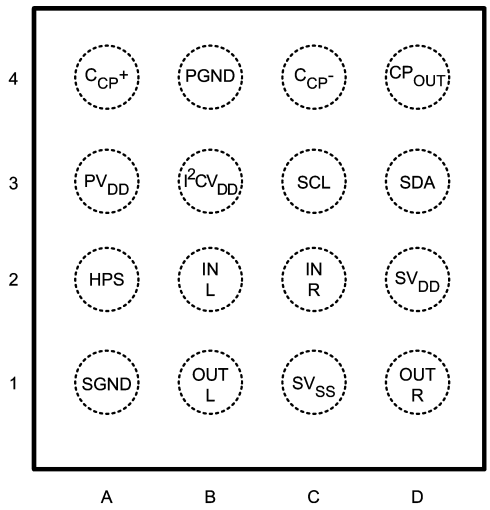


FIGURE 1. Typical Audio Amplifier Application Circuit

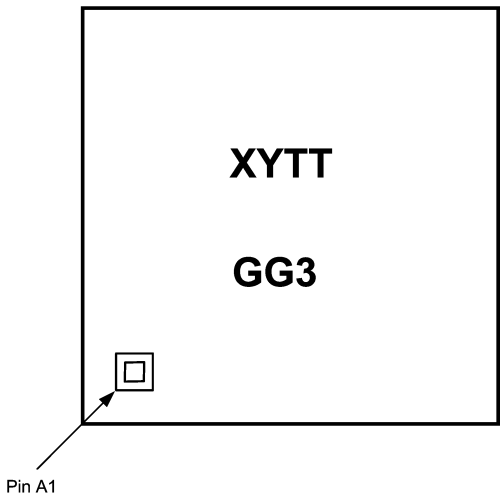
Connection Diagrams

micro SMD Package



Top View
Order Number LM4982TL

micro SMD Marking



Top View
XY - Date Code
TT - Lot Traceability
GG3 – LM4982
See NS Package Number LM4982TL

Pin Descriptions

Pin Designator	Pin Name	Pin Function
A1	SGND	Amplifier ground
A2	HPE	Headphone sende input
A3	PV_{DD}	Charge pump / digital power supply
A4	C_{CP+}	Charge pump fly capacitor positive side
B1	OUT_L	Left channel output
B2	IN_L	Left channel input
B3	$I^2C\_V_{DD}$	I^2C power supply
B4	PGND	Charge pump / digital ground
C1	SV_{SS}	Amplifier negative supply
C2	IN_R	Right channel input
C3	SCL	I^2C SCL line
C4	C_{CP-}	Charge pump fly capacitor negative side
D1	OUT_R	Right channel output
D2	SV_{DD}	Amplifier positive supply
D3	SDA	I^2C SDA line
D4	CP_{OUT}	Charge pump power output

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	4.5V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JA} (typ) - (TLA16XXX)	105˚C/W (Note X)

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	−40˚C ≤ T_A ≤ +85˚C
Supply Voltage	1.6V ≤ V_{DD} ≤ 4.0V

Audio Amplifier Electrical Characteristics V_{DD} = 3V (Notes 1, 2)

The following specifications apply for V_{DD} = 3V, R_L = 16Ω, A_V = 0dB, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4982		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current Full Power Mode	V_{IN} = 0V, inputs terminated, both channels enabled	8.1	11.5	mA (max)
		V_{IN} = 0V, inputs terminated, one channel enabled	5.1	7.3	mA
		V_{IN} = 0V, inputs terminated, No headphone inserted	2.15		mA
I_{SD}	Shutdown Current	With SD enabled	0.1	1.5	µA (max)
V_{OS}	Output Offset Voltage	R_L = 32Ω	0.7	4.5	mV (max)
A_V	Gain Max and Min settings	[B0:B4] = 00000	−70		dB
		[B0:B4] = 11111	+18		dB
R_{IN}	Input Resistance	gain setting 18dB	22	15 29	kΩ (min) kΩ (max)
		gain setting −76dB	200		kΩ
P_{OUT}	Stereo Output Power	THD+N = 1% (max); f = 1kHz, R_L = 16Ω, per channel	47	40	mW (min)
		THD+N = 1% (max); f = 1kHz, R_L = 32Ω, per channel	51		mW
THD+N	Total Harmonic Distortion + Noise	P_O = 50mW, f = 1kHz R_L = 16Ω, single channel	0.05		%
		P_O = 50mW, f = 1kHz R_L = 32Ω, single channel	0.025		
PSRR	Power Supply Rejection Ratio Full Power Mode	V_{RIPPLE} = 200mV_{P-P}, input referred			
		f = 217Hz	66	56	dB
		f = 1kHz	55		
		f = 20kHz	40		
SNR	Signal-to-Noise-Ratio	R_L = 32Ω, P_{OUT} = 20mW, f = 1kHz, BW = 20Hz to 22kHz	100		dB
T_{WU}	Wake Up Time From Shutdown	Charge Pump Wake-Up Time	300		µs
T_{WU}	Wake Up Time	Headphone Sense Debounce Time	200		ms
X_{TALK}	Crosstalk	R_L = 16Ω, P_{OUT} = 1.6mW, f = 1kHz, A-weighted filter	70		dB
Z_{OUT}	Output Impedance	In Shutdown Mode	180		kΩ
I_L	Input Leakage		±0.1		nA
Vih	HPS in threshold			0.9 x V_{DD} [min]	V
Vil	HPS in threshold			0.7 x V_{DD} [max]	V

Audio Amplifier Electrical Characteristics V_{DD} = 3V (Notes 1, 2) (Continued)

The following specifications apply for V_{DD} = 3V, R_L = 16Ω, A_V = 0dB, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4982		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
R_{INT}	Intellisense Threshold Resistance		6	3 9	Ω (min) Ω (max)

Control Interface Electrical Characteristics (Notes 1, 2)

The following specifications apply for 1.6V < V_{DD} < 4.0V, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4982		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
t_1	SCL period			2.5	µs (min)
t_2	SDA Setup Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}				0.7 x I^2CV_{DD}	V (min)
V_{IL}				0.3 x I^2CV_{DD}	V (max)

Note 1: All voltages are measured with respect to the GND pin unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4982, see power derating currents for more information.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF - 240pF discharged through all pins.

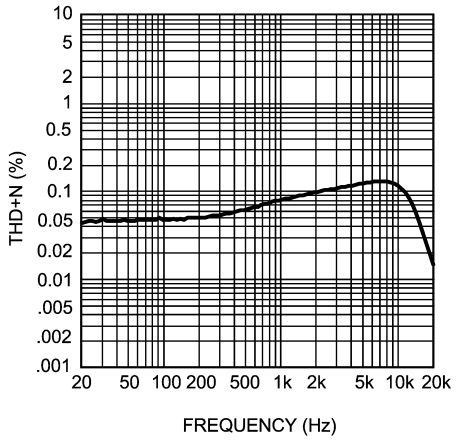
Note 6: Typicals are measured at +25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

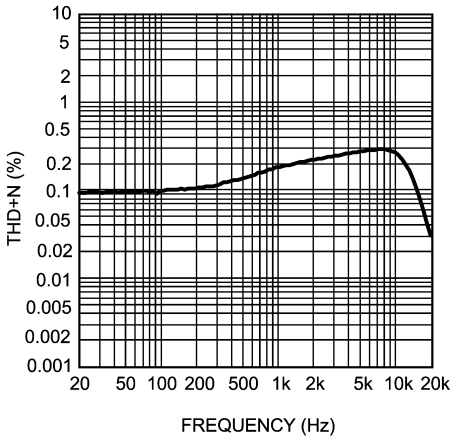
Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 16Ω,
P_O = 7mW, Mono



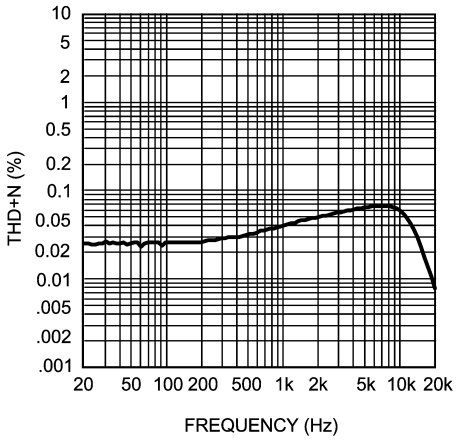
20161475

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 16Ω,
P_O = 2mW, Stereo



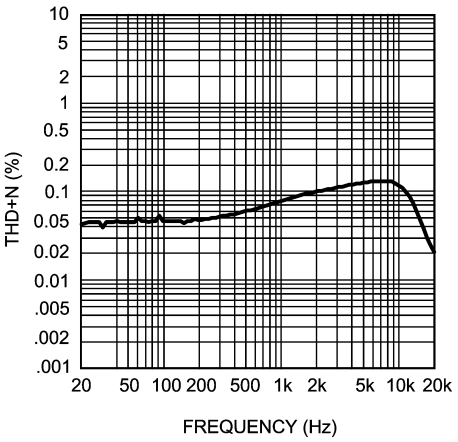
20161474

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 32Ω,
P_O = 7mW, Mono



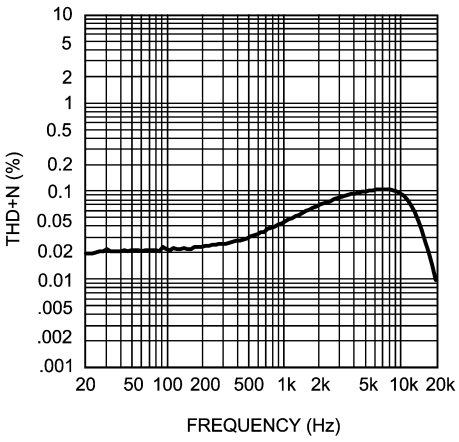
20161477

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 32Ω,
P_O = 2mW, Stereo



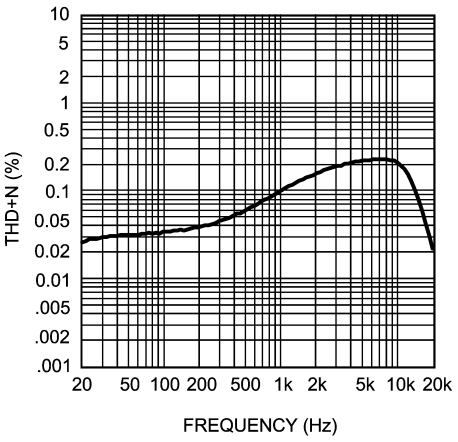
20161476

THD+N vs Frequency
V_{DD} = 3V, R_L = 16Ω,
P_O = 50mW, Mono



20161482

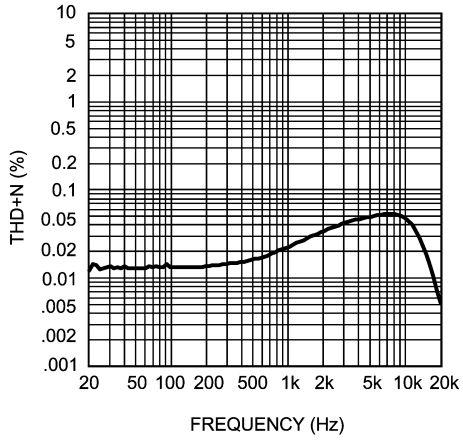
THD+N vs Frequency
V_{DD} = 3V, R_L = 16Ω,
P_O = 25mW, Stereo



20161483

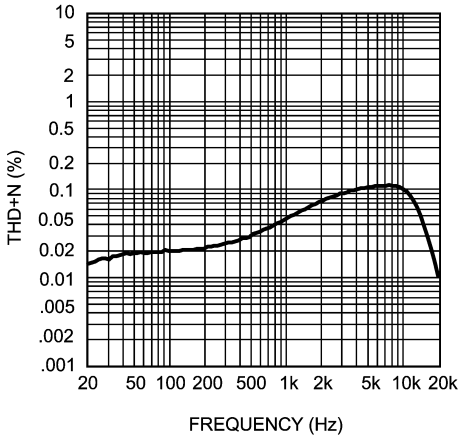
Typical Performance Characteristics (Continued)

THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω,
P_O = 50mW, Mono



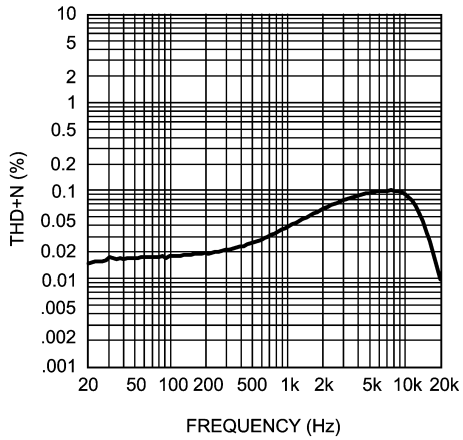
20161484

THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω,
P_O = 25mW, Stereo



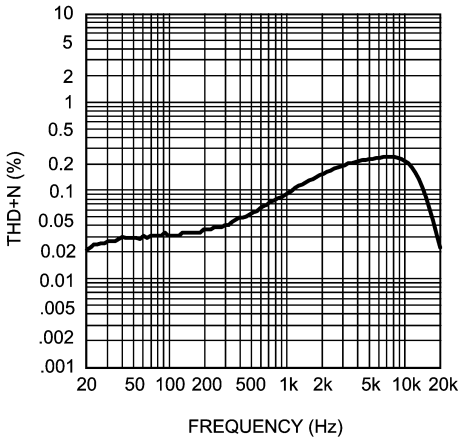
20161485

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 16Ω,
P_O = 100mW, Mono



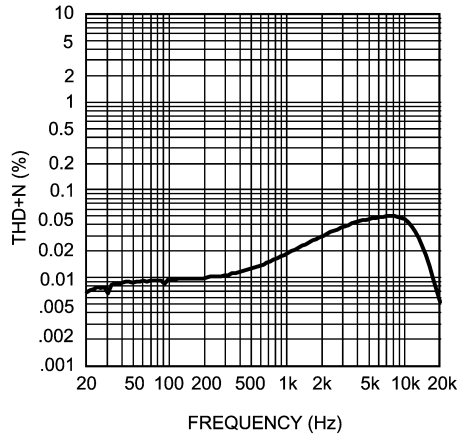
20161478

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 16Ω,
P_O = 60mW, Stereo



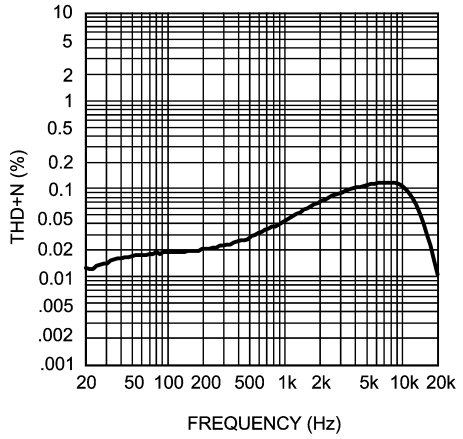
20161479

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω,
P_O = 100mW, Mono,



20161480

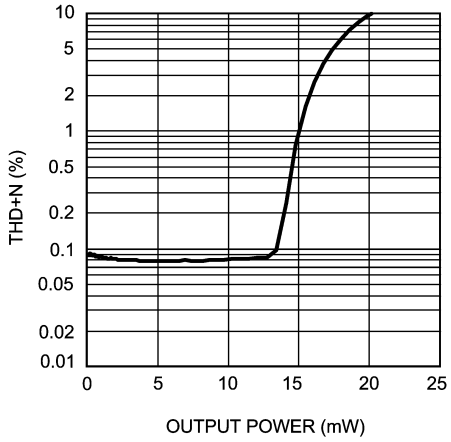
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω,
P_O = 60mW, Stereo



20161481

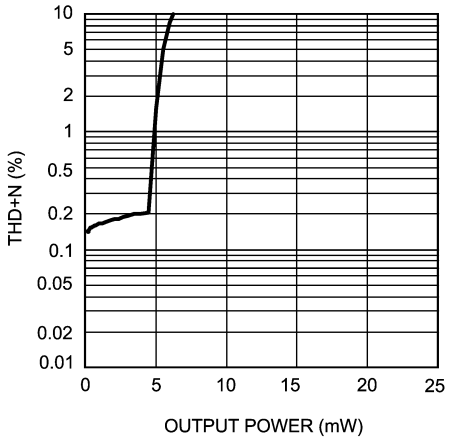
Typical Performance Characteristics (Continued)

THD+N vs Output Power
V_{DD} = 1.8V, R_L = 16Ω,
f = 1kHz, Mono



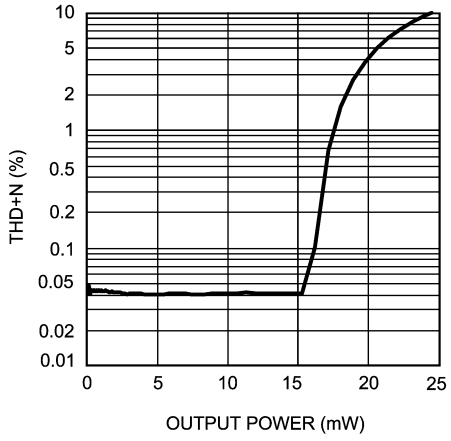
20161486

THD+N vs Output Power
V_{DD} = 1.8V, R_L = 16Ω,
f = 1kHz, Stereo



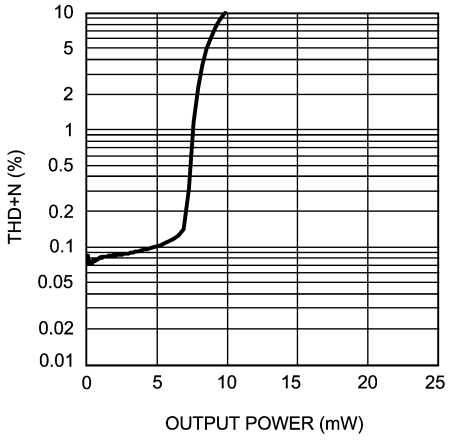
20161487

THD+N vs Output Power
V_{DD} = 1.8V, R_L = 32Ω,
f = 1kHz, Mono



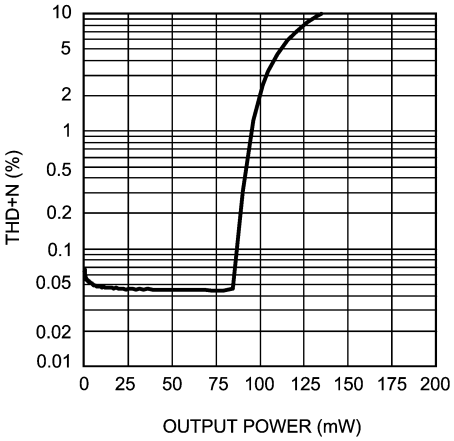
20161488

THD+N vs Output Power
V_{DD} = 1.8V, R_L = 32Ω,
f = 1kHz, Stereo



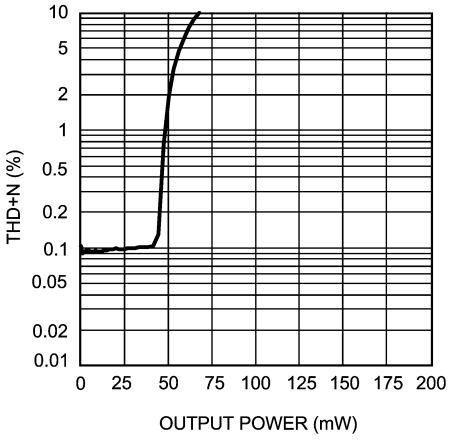
20161489

THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω,
f = 1kHz, Mono



20161494

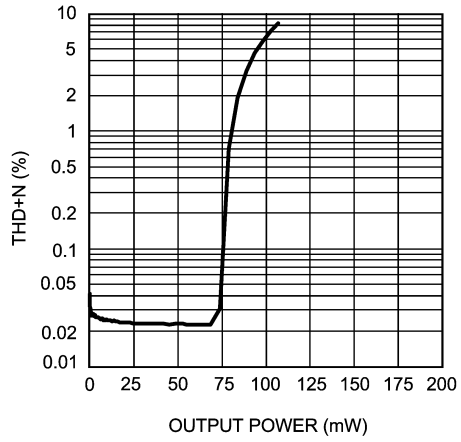
THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω,
f = 1kHz, Stereo



201614B2

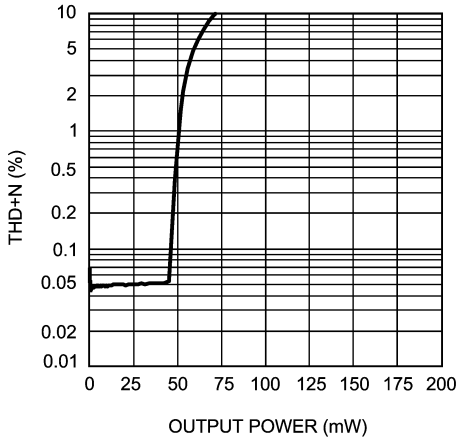
Typical Performance Characteristics (Continued)

THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω,
f = 1kHz, Mono



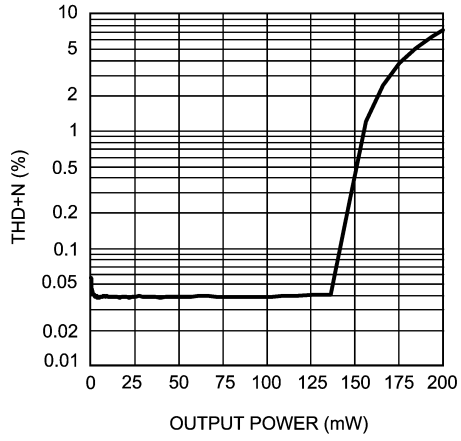
20161495

THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω,
f = 1kHz, Stereo



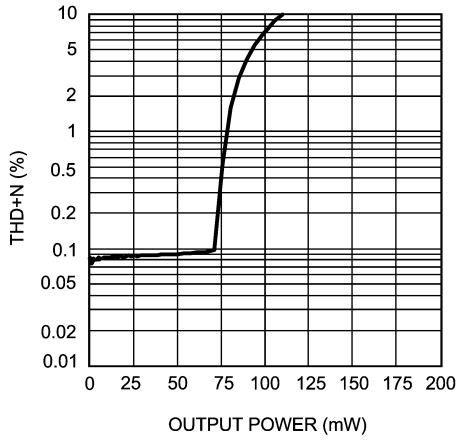
20161496

THD+N vs Output Power
V_{DD} = 3.6V, R_L = 16Ω,
f = 1kHz, Mono



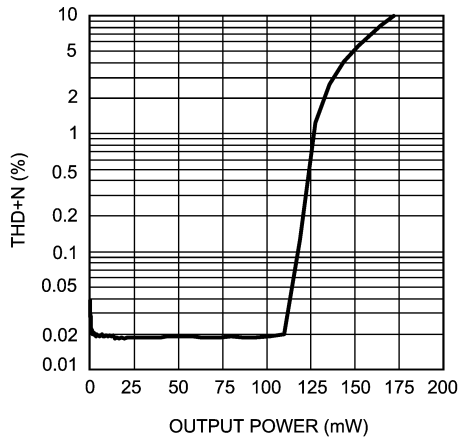
20161490

THD+N vs Output Power
V_{DD} = 3.6V, R_L = 16Ω,
f = 1kHz, Stereo



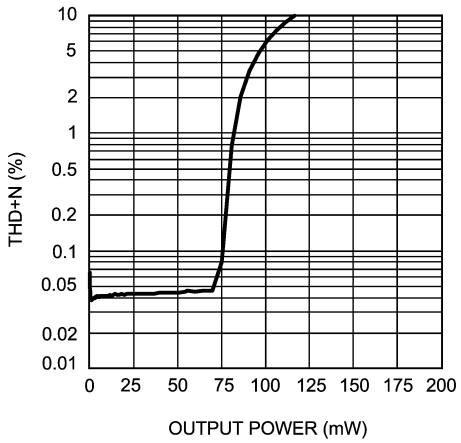
20161491

THD+N vs Output Power
V_{DD} = 3.6V, R_L = 32Ω,
f = 1kHz, Mono



20161492

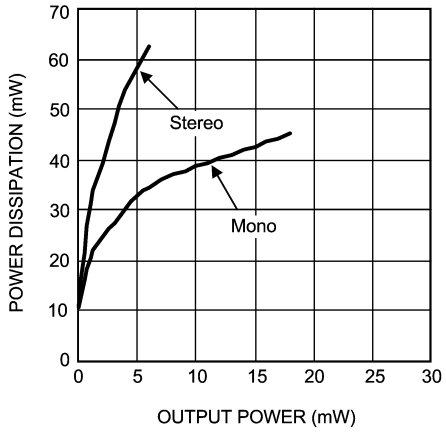
THD+N vs Output Power
V_{DD} = 3.6V, R_L = 32Ω,
f = 1kHz, Stereo



20161493

Typical Performance Characteristics (Continued)

Power Dissipation vs Output Power
V_{DD} = 1.8V, R_L = 16Ω, f = 1kHz



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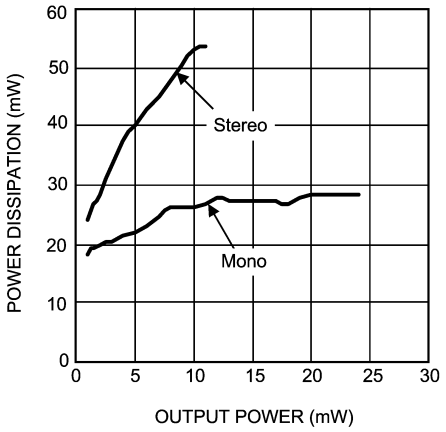
Power Dissipation vs Output Power
V_{DD} = 1.8V, R_L = 32Ω, f = 1kHz



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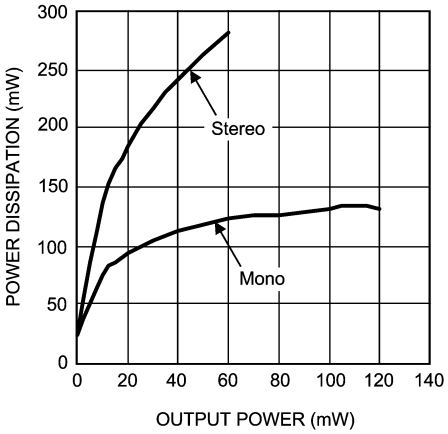
Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 16Ω, f = 1kHz



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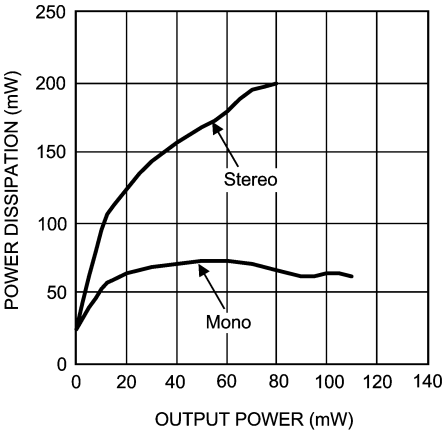
Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 32Ω, f = 1kHz



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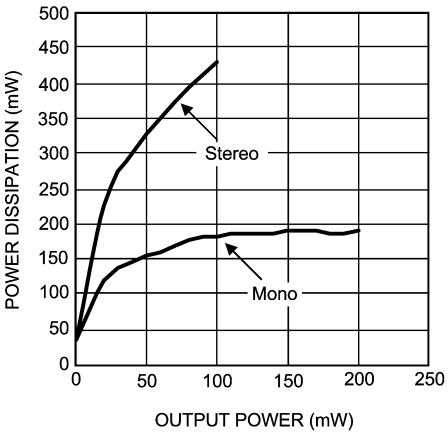
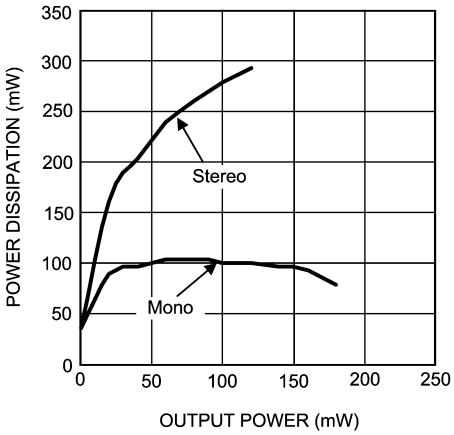
Power Dissipation vs Output Power
V_{DD} = 3.6V, R_L = 16Ω, f = 1kHz



201614A2

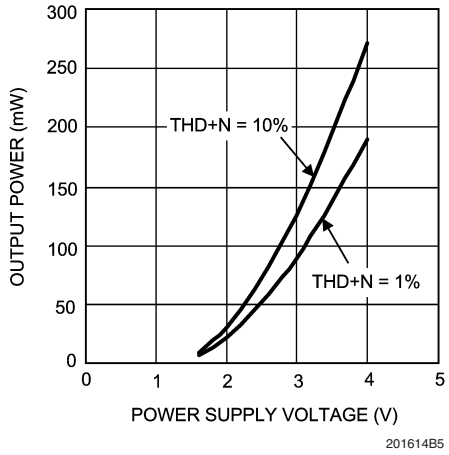
Power Dissipation vs Output Power
V_{DD} = 3.6V, R_L = 32Ω, f = 1kHz



201614A3

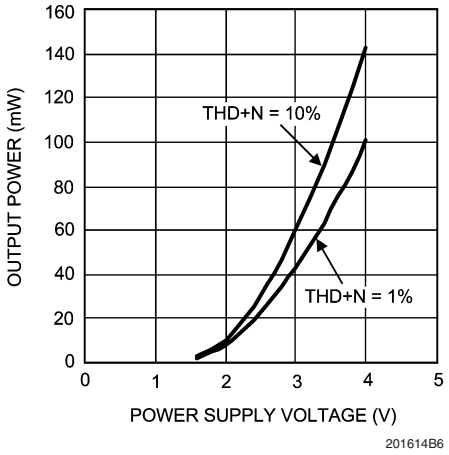
Typical Performance Characteristics (Continued)

Output Power vs Power Supply Voltage
R_L = 16Ω, f = 1kHz, Mono



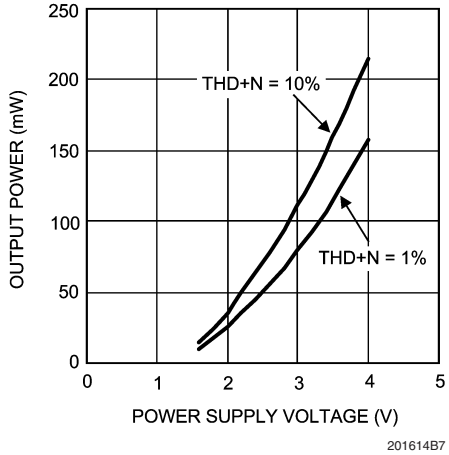
201614B5

Output Power vs Power Supply Voltage
R_L = 16Ω, f = 1kHz, Stereo



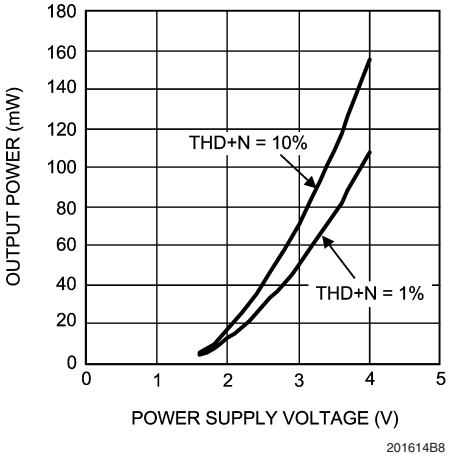
201614B6

Output Power vs Power Supply Voltage
R_L = 32Ω, f = 1kHz, Mono



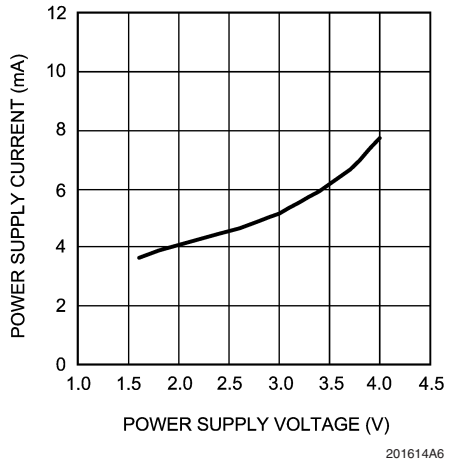
201614B7

Output Power vs Power Supply Voltage
R_L = 32Ω, f = 1kHz, Stereo



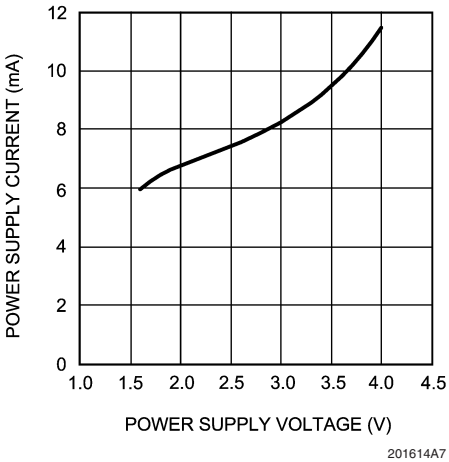
201614B8

Power Supply Current vs Power Supply Voltage
V_{IN} = 0V, Mono



201614A6

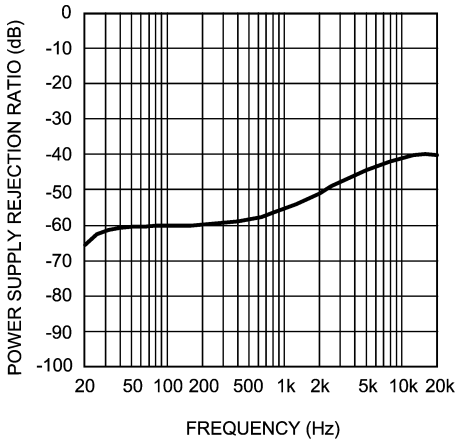
Power Supply Current vs Power Supply Voltage
V_{IN} = 0V, Stereo



201614A7

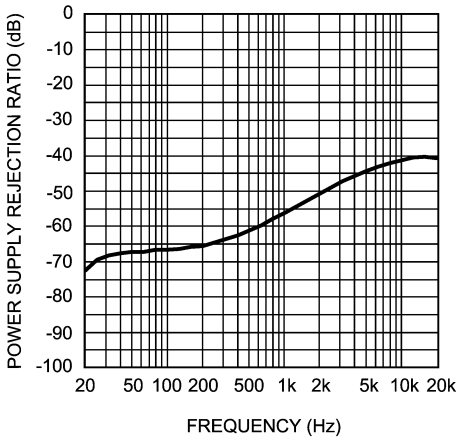
Typical Performance Characteristics (Continued)

PSRR vs Frequency
V_{DD} = 1.8V, Vripple = 200mVp-p



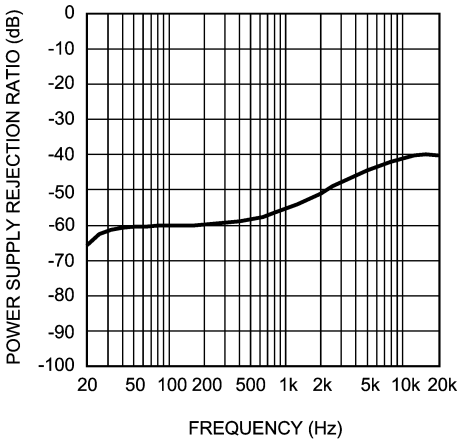
201614A8

PSRR vs Frequency
V_{DD} = 3V, Vripple = 200mVp-p



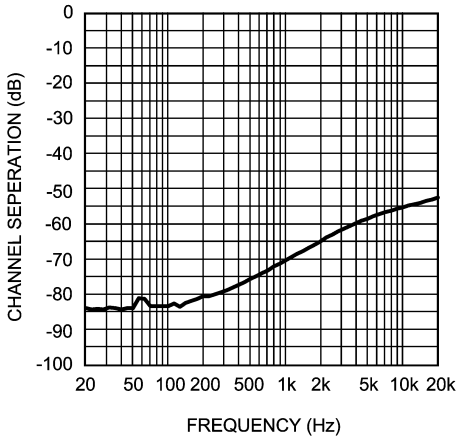
201614B1

PSRR vs Frequency
V_{DD} = 3.6V, Vripple = 200mVp-p



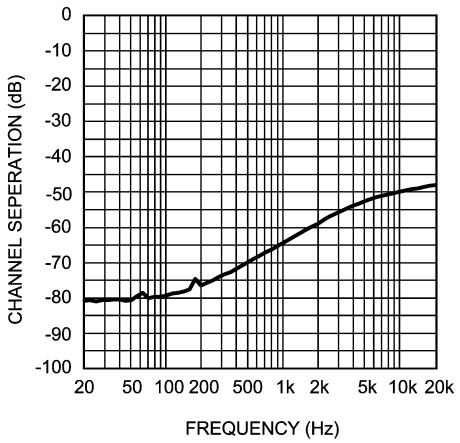
201614B0

Crosstalk
V_{DD} = 3V, RL = 16Ω, P_O= 50mW



201614B3

Crosstalk
V_{DD} = 3V, RL = 32Ω, P_O= 50mW



201614B4

Application Information

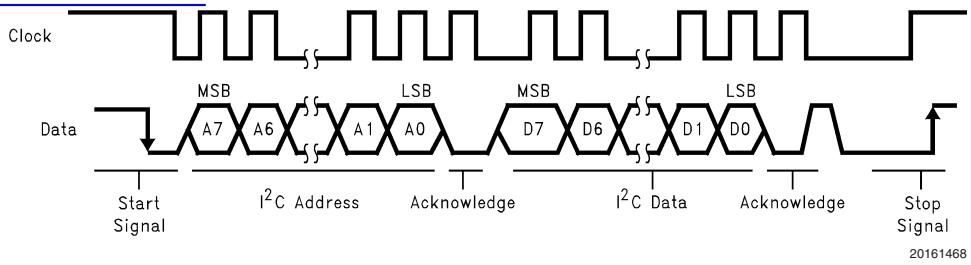


FIGURE 2. I²C Bus Format

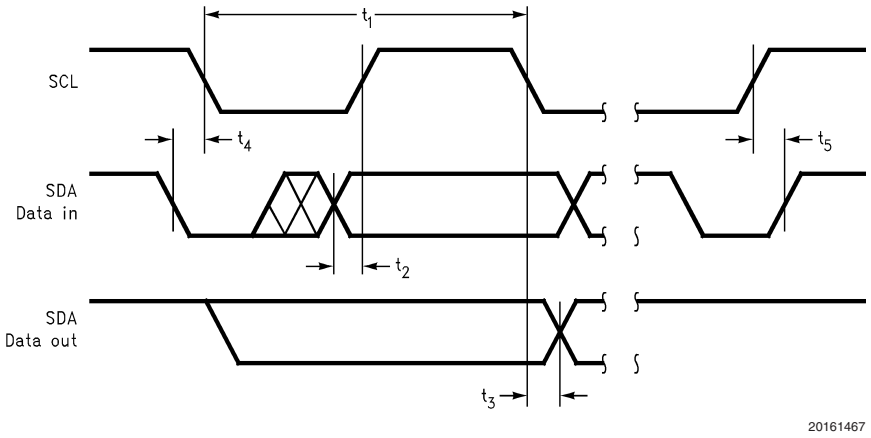


FIGURE 3. I²C Timing Diagram

TABLE 1. Chip Address

	D7	D6	D5	D4	D3	D2	D1	D0
Chip Address	1	1	1	0	1	1	0	0

TABLE 2. Control Registers

	D7	D6	D5	D4	D3	D2	D1	D0
Mode Control	0	0	0	0	CD3	CD2	CD1	CD0
Volume Control	1	0	0	VD4	VD3	VD2	VD1	VD0

TABLE 3. Mode Control

CD3	1	Intellisense Enabled
	0	Intellisense Disabled
CD2	1	Mute Enabled
	0	Mute Disabled
CD1	1	Stereo
	0	Mono *
CD0	1	Normal Operation
	0	Shutdown Enabled

*** Mono mode mixes (Left + Right) / 2, into Left output**

I²C VOLUME CONTROL

The LM4982 can be configured in 32 different gain steps by forcing I2C volume control bits to a desired gain according to the table below:

Application Information (Continued)

TABLE 4. Volume Control

VD4	VD3	VD2	VD1	VD0	Gain (dB)
0	0	0	0	0	−70
0	0	0	0	1	−60
0	0	0	1	0	−52
0	0	0	1	1	−44
0	0	1	0	0	−38
0	0	1	0	1	−34
0	0	1	1	0	−30
0	0	1	1	1	−27
0	1	0	0	0	−24
0	1	0	0	1	−21
0	1	0	1	0	−18
0	1	0	1	1	−16
0	1	1	0	0	−14
0	1	1	0	1	−12
0	1	1	1	0	−10
0	1	1	1	1	−8
1	0	0	0	0	−6
1	0	0	0	1	−4
1	0	0	1	0	−2
1	0	0	1	1	0
1	0	1	0	0	2
1	0	1	0	1	4
1	0	1	1	0	6
1	0	1	1	1	8
1	1	0	0	0	10
1	1	0	0	1	12
1	1	0	1	0	13
1	1	0	1	1	14
1	1	1	0	0	15
1	1	1	0	1	16
1	1	1	1	0	17
1	1	1	1	1	18

Application Information (Continued)

HP SENSE FUNCTION

Connecting headphones to the headphone jack disconnects the headphone jack contact pin from OUT_L and allows Rpu to pull the HP Sense pin up to V_{DD}. This enables the device. A microprocessor or a switch can replace the headphone jack contact pin.

Shutdown (Bit CD0)	HPS pin	Operational Mode
Logic High	Logic Low	Standby Mode
Logic High	Logic High	Full Power Mode
Logic Low	Logic Low	Micro-Power Shutdown
Logic Low	Logic High	Micro-Power Shutdown

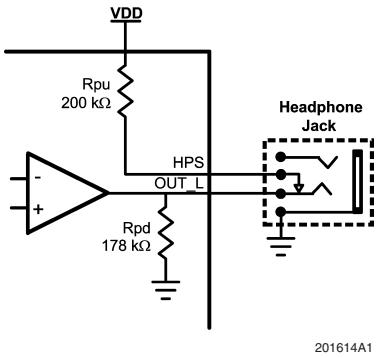


FIGURE 4.

INTELLISENSE

National's Intellisense technology allows the LM4982 to detect whether a mono or stereo headphone has been insterted in to the headphone jack. If a mono headphone is inserted into a device that is designed for a stereo headphone, one of the amplifiers will be shorted to ground. Without Intellisense, this may damage the device or, best case, the device will draw excessive current, shortening battery life.

Intellisense works by first waiting for one of the following events:

• When the device powers up, if a headphone is already inserted

• When a headphone is inserted, if the device is already powered up

• After the thermal shutdown circuitry is activated.

The occurrence of one of these events triggers the Intellisense circuitry to apply a small voltage on both left and right outputs and sense the resulting current through the load. If the load connected to the amplifier is greater than 9Ω, the amplifier driving it will be in full power mode. If the load is less than 3Ω, the LM4982 will assume a short to ground and shutdown the driving amplifier. Intellisense puts the LM4982 in mono mode when the right channel is shorted. For extra protection both amplifiers will be shutdown when the left channel is shorted to ground. The Intellisense feature can be enabled and disabled through an I2C command.

This Intellisense feature is designed for headphones with a nominal impedance of 16Ω or greater, using lower impedance loads may cause this feature to operate incorrectly.

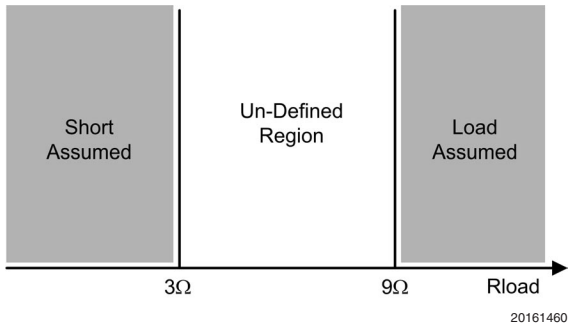


FIGURE 5.

MONO/STEREO OPERATION

When Intellisense is disabled the value of the CD1 bit of the mode control determines if the LM4982 is in mono or stereo mode. When the LM4982 is in mono mode the left and right input signals are mixed to the left channel amplifier and attenuated by -6dB. The right channel amplifier is put in shutdown to save power. The mixing function allows full reproduction of a stereo input signal in a mono headphone and optimum headroom is kept by attenuating by a factor of two.

I^2C COMPATIBLE INTERFACE

The LM4982 uses a serial bus, which conforms to the I^2C protocol, to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I^2C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4982.

The bus format for the I^2C interface is shown in Figure 2. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I^2C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is high.

After the last bit of the address bit is sent, the master releases the data line high (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4982 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not held low during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4982.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must check for another acknowledge to see if the LM4982 received the data.

If the master has more data bytes to send to the LM4982, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes high while the clock signal is high. The data line should be held high when not in use.

Application Information (Continued)

I²C INTERFACE POWER SUPPLY PIN (I^2CV_{DD})

The LM4982's I^2C interface is powered up through the I^2CV_{DD} pin. The LM4982's I^2C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I^2C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4982's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4982's power supply pins and ground as short as possible.

ELIMINATING THE OUTPUT COUPLING CAPACITOR

The LM4982 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the outputs of the LM4982 to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two, small ceramic charge pump capacitors, saving board space and cost.

Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor form a high pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM4982 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components.

In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM4982 when compared to a traditional headphone amplifier operating from the same supply voltage.

OUTPUT TRANSIENT ('CLICK AND POPS') ELIMINATED

The LM4982 contains advanced circuitry that virtually eliminates output transients ('clicks and pops'). This circuitry prevents all traces of transients when the supply voltage is first applied or when the part resumes operation after coming out of shutdown mode.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (2V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM4982 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. Even with large internal power dissipation, the LM4982 does not require heat sinking over a large range of ambient temperatures. The maximum power dissipation point obtained must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A) / (\theta_{JA}) \quad (2)$$

For the micro SMD package, θ_{JA} = 105˚C/W. T_{JMAX} = 150˚C for the LM4982. Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4982's performance requires properly selecting external components. Though the LM4982 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

Charge Pump Capacitor Selection

Use low ESR (equivalent series resistance) (<100mΩ) ceramic capacitors with an X7R dielectric for best performance. Low ESR capacitors keep the charge pump output impedance to a minimum, extending the headroom on the negative supply. Higher ESR capacitors result in reduced output power from the audio amplifiers.

Charge pump load regulation and output impedance are affected by the value of the flying capacitor (C1). A larger valued C1 (up to 3.3uF) improves load regulation and minimizes charge pump output resistance. Beyond 3.3uF, the switch-on resistance dominates the output impedance for capacitor values above 2.2uF.

The output ripple is affected by the value and ESR of the output capacitor (C2). Larger capacitors reduce output ripple on the negative power supply. Lower ESR capacitors minimize the output ripple and reduce the output impedance of the charge pump.

The LM4982 charge pump design is optimized for 2.2uF, low ESR, ceramic, flying, and output capacitors.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitors (C_i in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using high value input and output capacitors.

Besides affecting system cost and size, C_i has an effect on the LM4982's click and pop performance. The magnitude of the pop is directly proportional to the input capacitor's size.

Application Information (Continued)

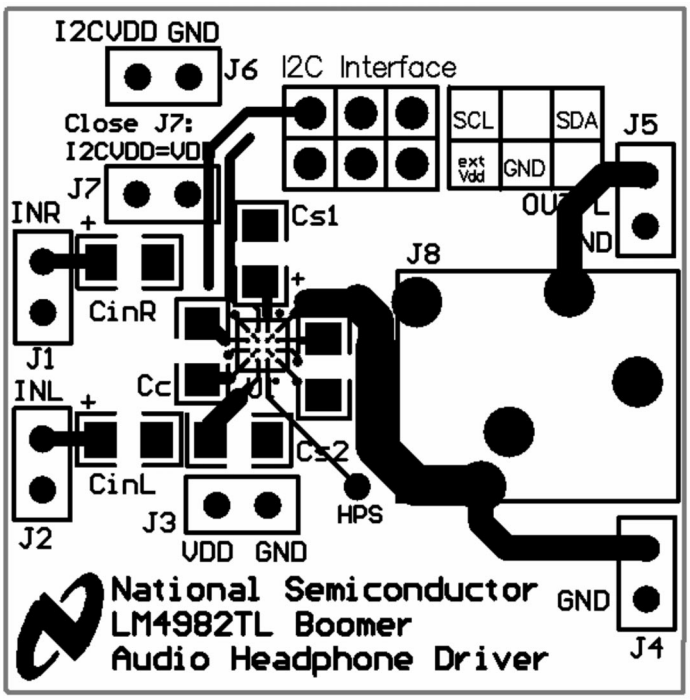
Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

As shown in Figure 1, the internal input resistor, R_i and the input capacitor, C_i, produce a -3dB high pass filter cutoff frequency that is found using Equation (3). Conventional headphone amplifiers require output capacitors; Equation (3) can be used, along with the value of R_L, to determine towards the value of output capacitor needed to produce a −3dB high pass filter cutoff frequency.

$$f_{i\text{-}3dB} = 1 / 2\pi R_i C_i \quad (3)$$

Also, careful consideration must be taken in selecting a certain type of capacitor to be used in the system. Different types of capacitors (tantalum, electrolytic, ceramic) have unique performance characteristics and may affect overall system performance. (See the section entitled Charge Pump Capacitor Selection.)

Demo Board Artwork



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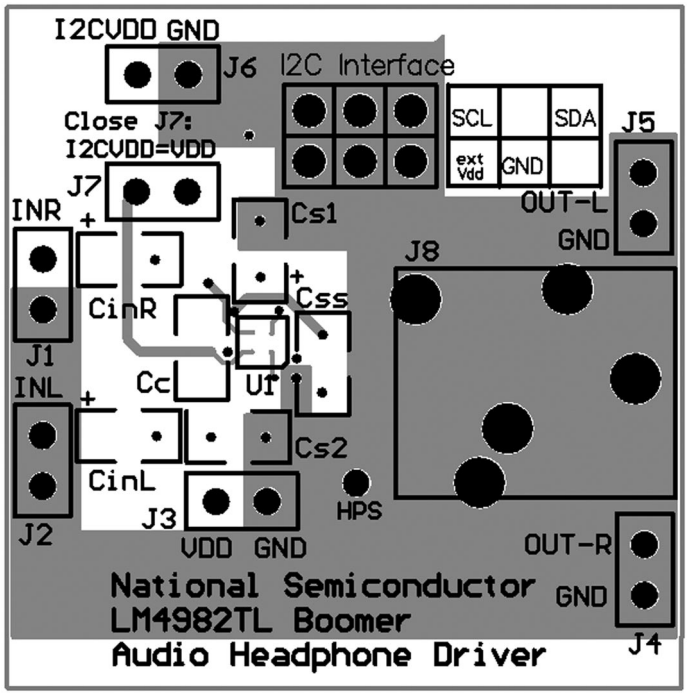
Top Layer



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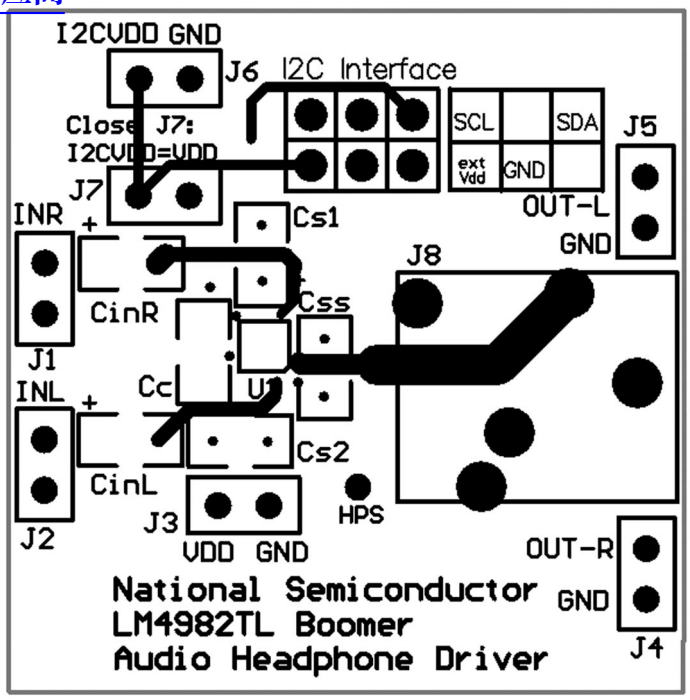
Mid Layer 1

Demo Board Artwork (Continued)



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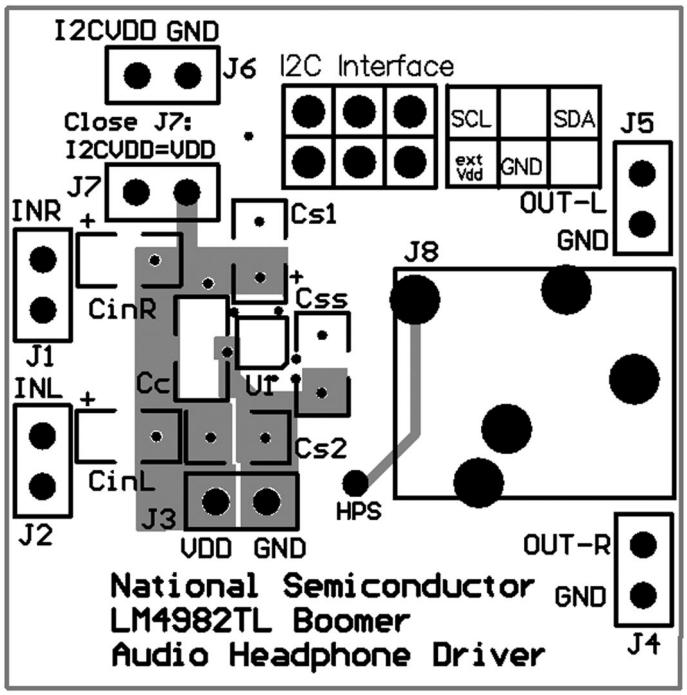
Mid Layer 2



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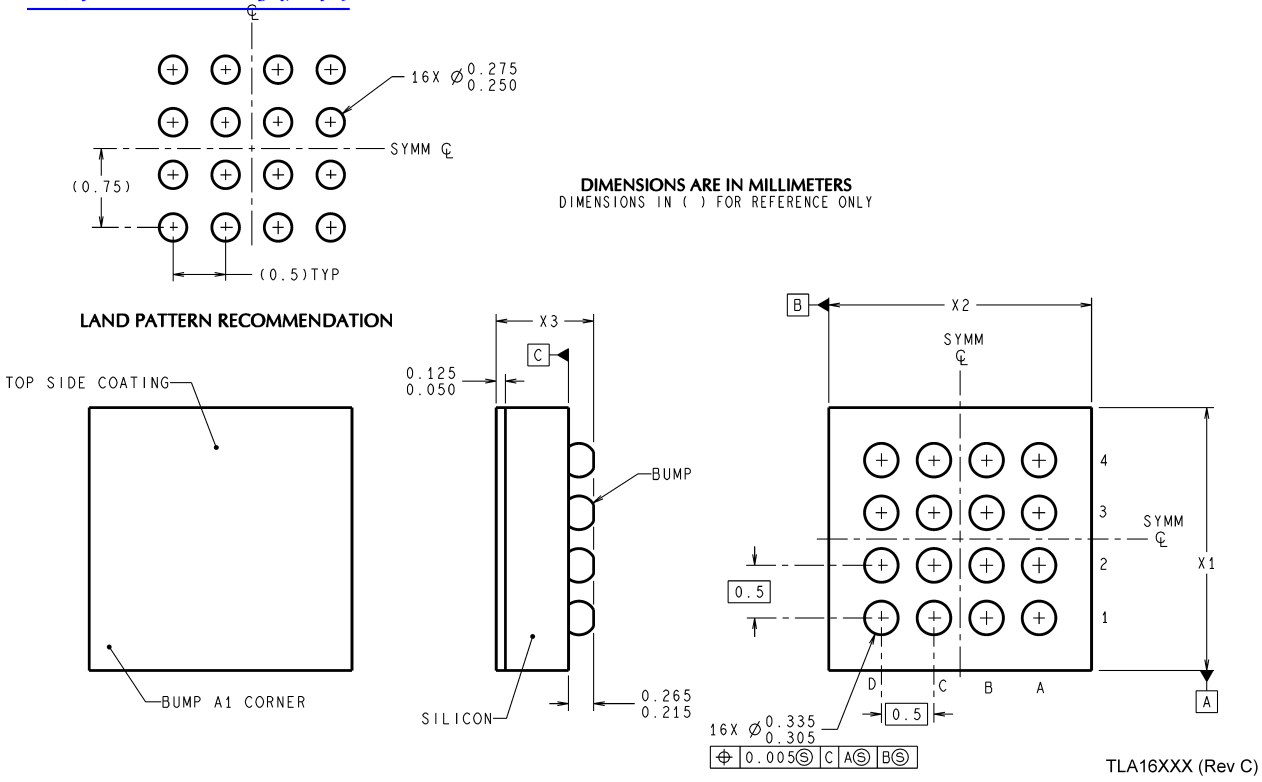
Bottom Layer

Revision History

Rev	Date	Description
1.0	7/19/05	First PDF.
1.1	7/26/05	Edited 20161401 (markings) and 20161459 (micro SMD pkg drawing)
1.2	10/26/05	Text edits input. Also replaced 201614 61 with 66.
1.3	10/28/05	Texts edit.
1.4	11/01/05	Deleted PSRR (Stndby Mode) in the 3V EC table (per Nisha).
1.5	11/03/05	Added the boards and few text edits
1.6	11/07/05	Few text edits.
1.7	01/23/06	Added the Typ Perf curves, boards, and text edits.
1.8	01/27/06	Fixed typos, edited 66, 01, and more of the curves.
1.9	2/09/06	Input few text edits. First WEB released.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Bump micro SMD
Order Number LM4982TL
NS Package Number TLA16CZA
X_1 = 2.543 ± 0.03 X_2 = 2.949 ± 0.03 X_3 = 0.6 ± 0.075

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