PRELIMINARY PRODUCT SPECIFICATIONS

SHARP

Integrated Circuits Group

# LRS1383H

## Stacked Chip

## 32M (x16) Boot Block Flash and 8M (x16) SRAM

(Model No.: LRS1383H)

Spec No.: MFM2-J14418
Issue Date: April 24, 2002

SHARP

| SPEC No. | MFM2-J14418 |
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PRELIMINARY

# SPECIFICATIONS

Product Type 32M (x16) Flash Memory +8M (x16) SRAM

# LRS1383H

Model No. ( LRS1383H )

This device specification is subject to change without notice.

*This specifications contains 39 pages including the cover and appendix.
*Refer to LH28F320BF, LH28F640BF, LH28F128BF Series Appendix (FUM00701).

CUSTOMERS ACCEPTANCE

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

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Contents

## 1. Description

The LRS1383H is a combination memory organized as 2,097,152 x16 bit flash memory and 524,288 x16 bit static RAM in one package.

### Features

- Power supply • • • • 2.7V to 3.3V
- Operating temperature • • • • -25°C to +85°C
- Not designed or rated as radiation hardened
- 72pin CSP (LCSP072-P-0811) plastic package
- Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon

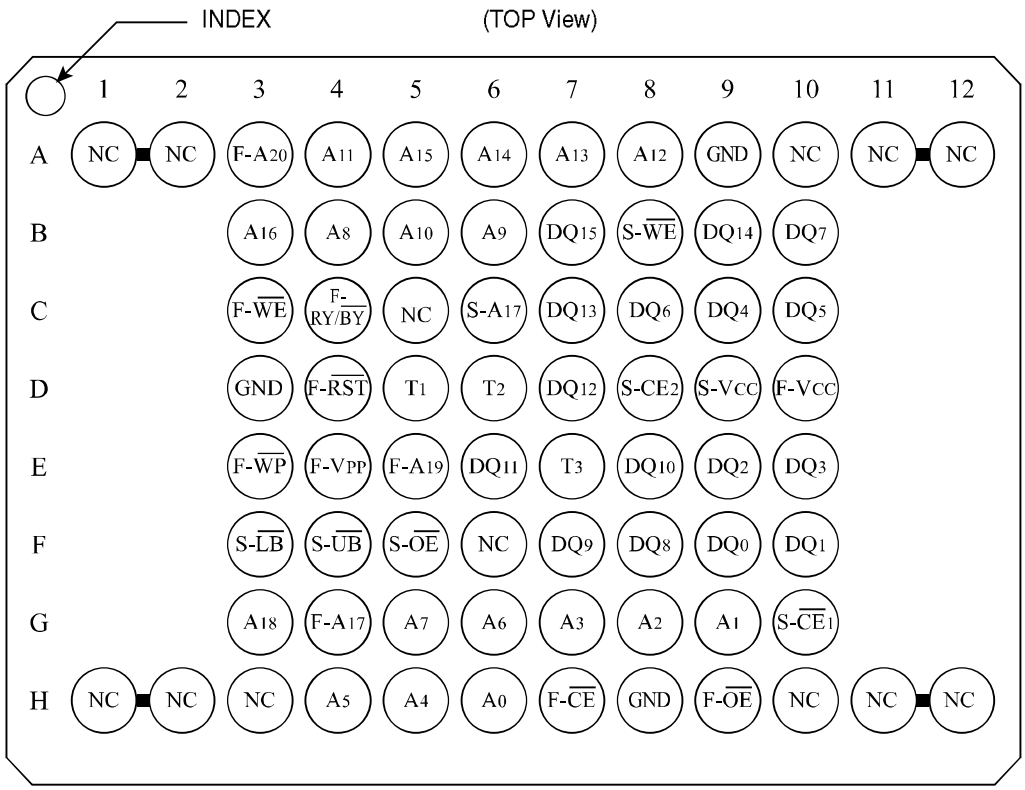
### Flash Memory

- Access Time • • • • 70 ns (Max.)
- Power supply current (The current for F-$V_{CC}$ pin and F-$V_{PP}$ pin)
  - Read • • • • 25 mA (Max. $t_{CYCLE}$ = 200ns, CMOS Input)
  - Word write • • • • 60 mA (Max.)
  - Block erase • • • • 30 mA (Max.)
  - Reset Power-Down • • • • 25 µA (Max. F-$\overline{RST}$ = GND ± 0.2V, $I_{OUT}$ (F-RY/$\overline{BY}$) = 0mA)
  - Standby • • • • 25 µA (Max. F-$\overline{CE}$ = F-$\overline{RST}$ = F-$V_{CC}$ ± 0.2V)
- Optimized Array Blocking Architecture
  - Eight 4K-word Parameter Blocks
  - Sixty-Three 32K-word Main Blocks
  - Bottom Parameter Location
- Extended Cycling Capability
  - 100,000 Block Erase Cycles (F-$V_{PP}$ = 1.65V to 3.3V)
  - 1,000 Block Erase Cycles and total 80 hours (F-$V_{PP}$ = 11.7V to 12.3V)
- Enhanced Automated Suspend Options
  - Word Write Suspend to Read
  - Block Erase Suspend to Word Write
  - Block Erase Suspend to Read
- OTP Block
  - 4 Word + 4 Word Array

### SRAM

- Access Time • • • • 70 ns (Max.)
- Power Supply current
  - Operating current • • • • 50 mA (Max. $t_{RC}$, $t_{WC}$ = Min.)
  - • • • • 8 mA (Max. $t_{RC}$, $t_{WC}$ = 1µs, CMOS Input)
  - Standby current • • • • 25 µA (Max.)
  - Data retention current • • • • 25 µA (Max. S-$V_{CC}$ = 3.0V)

2. Pin Configuration




Note) From T1 to T3 pins are needed to be open.
Two NC pins at the corner are connected.
Do not float any GND pins.

| Pin | Description | Type |
|---|---|---|
| $A_0$ to $A_{16}$, $A_{18}$ | Address Inputs (Common) | Input |
| F-$A_{17}$, F-$A_{19}$, F-$A_{20}$ | Address Inputs (Flash) | Input |
| S-$A_{17}$ | Address Input (SRAM) | Input |
| F-$\overline{CE}$ | Chip Enable Input (Flash) | Input |
| S-$\overline{CE}_1$, S-$CE_2$ | Chip Enable Inputs (SRAM) | Input |
| F-$\overline{WE}$ | Write Enable Input (Flash) | Input |
| S-$\overline{WE}$ | Write Enable Input (SRAM) | Input |
| F-$\overline{OE}$ | Output Enable Input (Flash) | Input |
| S-$\overline{OE}$ | Output Enable Input (SRAM) | Input |
| S-$\overline{LB}$ | SRAM Byte Enable Input ($DQ_0$ to $DQ_7$) | Input |
| S-$\overline{UB}$ | SRAM Byte Enable Input ($DQ_8$ to $DQ_{15}$) | Input |
| F-$\overline{RST}$ | Reset Power Down Input (Flash)<br>Block erase and Write : $V_{IH}$<br>Read : $V_{IH}$<br>Reset Power Down : $V_{IL}$ | Input |
| F-$\overline{WP}$ | Write Protect Input (Flash)<br>When F-$\overline{WP}$ is $V_{IL}$, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When F-$\overline{WP}$ is $V_{IH}$, lock-down is disabled. | Input |
| F-RY/$\overline{BY}$ | Ready/Busy Output (Flash)<br>During an Erase or Write operation : $V_{OL}$<br>Block Erase and Write Suspend : High-Z (High impedance) | Open Drain Output |
| $DQ_0$ to $DQ_{15}$ | Data Inputs and Outputs (Common) | Input / Output |
| F-$V_{CC}$ | Power Supply (Flash) | Power |
| S-$V_{CC}$ | Power Supply (SRAM) | Power |
| F-$V_{PP}$ | Monitoring Power Supply Voltage (Flash)<br>Block Erase and Write : F-$V_{PP}$ = $V_{PPH1/2}$<br>All Blocks Locked : F-$V_{PP}$ < $V_{PPLK}$ | Input |
| GND | GND (Common) | Power |
| NC | Non Connection | - |
| $T_1$ to $T_3$ | Test pins (Should be all open) | - |

3. Truth Table

3.1 Bus Operation(1)

| Flash | SRAM | Notes | F-$\overline{CE}$ | F-$\overline{RST}$ | F-$\overline{OE}$ | F-$\overline{WE}$ | S-$\overline{CE}_1$ | S-$CE_2$ | S-$\overline{OE}$ | S-$\overline{WE}$ | S-$\overline{LB}$ | S-$\overline{UB}$ | $DQ_0$ to $DQ_{15}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | Standby | 3,5 | L | H | L | H | (8) | | X | X | (8) | | (7) |
| Output Disable | | 5 | | | H | | | | | | | | High-Z |
| Write | | 2,3,4,5 | | | | L | | | | | | | $D_{IN}$ |
| Standby | Read | 5 | H | H | X | X | L | H | L | H | (9) | | |
| | Output Disable | 5 | | | | | | | H | H | X | X | High-Z |
| | | | | | | | | | X | X | H | H | |
| | Write | 5 | | | | | | | X | L | (9) | | |
| Reset Power Down | Read | 5,6 | X | L | X | X | L | H | L | H | (9) | | |
| | Output Disable | 5,6 | | | | | | | H | H | X | X | High-Z |
| | | | | | | | | | X | X | H | H | |
| | Write | 5,6 | | | | | | | X | L | (9) | | |
| Standby | Standby | 5 | H | H | X | X | (8) | | X | X | (8) | | High-Z |
| Reset Power Down | | 5,6 | X | L | | | | | | | | | |

Notes:

1. L = $V_{IL}$, H = $V_{IH}$, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. Command writes involving block erase, (page buffer) program or OTP program are reliably executed when F-$V_{PP}$ = $V_{PPH1/2}$ and F-$V_{CC}$ = 2.7V to 3.3V.
   Command writes involving full chip erase is reliably executed when F-$V_{PP}$ = $V_{PPH1}$ and F-$V_{CC}$ = 2.7V to 3.3V.
   Block erase, full chip erase, (page buffer) program or OTP program with F-$V_{PP}$ < $V_{PPH1/2}$ (Min.) produce spurious results and should not be attempted.
3. Never hold F-$\overline{OE}$ low and F-$\overline{WE}$ low at the same timing.
4. Refer Section 5. Command Definitions for Flash Memory valid $D_{IN}$ during a write operation.
5. F-$\overline{WP}$ set to $V_{IL}$ or $V_{IH}$.
6. Electricity consumption of Flash Memory is lowest when F-$\overline{RST}$ = GND ±0.2V.
7. Flash Read Mode

| Mode | Address | $DQ_0$ to $DQ_{15}$ |
|---|---|---|
| Read Array | X | $D_{OUT}$ |
| Read Identifier Codes/OTP | See 5.2 | See 5.2 |
| Read Query | Refer to the Appendix | Refer to the Appendix |

8. SRAM Standby Mode

| S-$\overline{CE}_1$ | S-$CE_2$ | S-$\overline{LB}$ | S-$\overline{UB}$ |
|---|---|---|---|
| H | X | X | X |
| X | L | X | X |
| X | X | H | H |

9. S-$\overline{UB}$, S-$\overline{LB}$ Control Mode

| S-$\overline{LB}$ | S-$\overline{UB}$ | $DQ_0$ to $DQ_7$ | $DQ_8$ to $DQ_{15}$ |
|---|---|---|---|
| L | L | $D_{OUT}/D_{IN}$ | $D_{OUT}/D_{IN}$ |
| L | H | $D_{OUT}/D_{IN}$ | High-Z |
| H | L | High-Z | $D_{OUT}/D_{IN}$ |

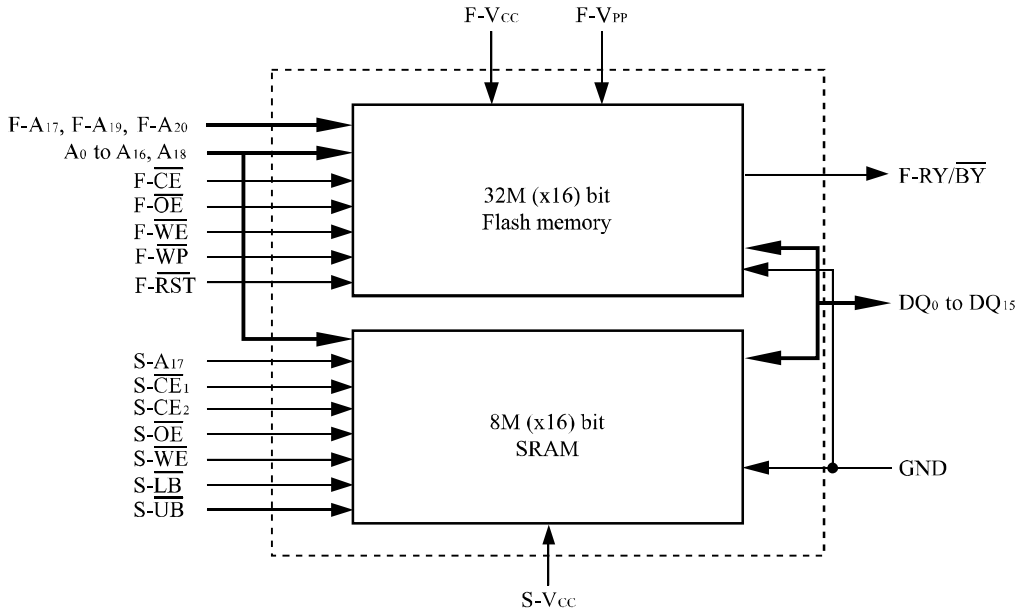
3.2 Simultaneous Operation Modes Allowed with Four Planes(1, 2)

| IF ONE PARTITION IS: | THEN THE MODES ALLOWED IN THE OTHER PARTITION IS: | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Read Array | Read ID/OTP | Read Status | Read Query | Word Program | Page Buffer Program | OTP Program | Block Erase | Full Chip Erase | Program Suspend | Block Erase Suspend |
| Read Array | X | X | X | X | X | X | | X | | X | X |
| Read ID/OTP | X | X | X | X | X | X | | X | | X | X |
| Read Status | X | X | X | X | X | X | X | X | X | X | X |
| Read Query | X | X | X | X | X | X | | X | | X | X |
| Word Program | X | X | X | X | | | | | | | X |
| Page Buffer Program | X | X | X | X | | | | | | | X |
| OTP Program | | | X | | | | | | | | |
| Block Erase | X | X | X | X | | | | | | | |
| Full Chip Erase | | | X | | | | | | | | |
| Program Suspend | X | X | X | X | | | | | | | X |
| Block Erase Suspend | X | X | X | X | X | X | | | | X | |

Notes:

1. “X” denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.
   Only one partition can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.

4. Block Diagram



## 5. Command Definitions for Flash Memory(11)

### 5.1 Command Definitions

| Command | Bus Cycles Req'd | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|---|
| | | | Oper(1) | Address(2) | Data(3) | Oper(1) | Address(2) | Data(3) |
| Read Array | 1 | 2 | Write | PA | FFH | | | |
| Read Identifier Codes/OTP | ≥2 | 2,3,4 | Write | PA | 90H | Read | IA or OA | ID or OD |
| Read Query | ≥2 | 2,3,4 | Write | PA | 98H | Read | QA | QD |
| Read Status Register | 2 | 2,3 | Write | PA | 70H | Read | PA | SRD |
| Clear Status Register | 1 | 2 | Write | PA | 50H | | | |
| Block Erase | 2 | 2,3,5 | Write | BA | 20H | Write | BA | D0H |
| Full Chip Erase | 2 | 2,5,9 | Write | X | 30H | Write | X | D0H |
| Program | 2 | 2,3,5,6 | Write | WA | 40H or 10H | Write | WA | WD |
| Page Buffer Program | ≥4 | 2,3,5,7 | Write | WA | E8H | Write | WA | N-1 |
| Block Erase and (Page Buffer) Program Suspend | 1 | 2,8,9 | Write | PA | B0H | | | |
| Block Erase and (Page Buffer) Program Resume | 1 | 2,8,9 | Write | PA | D0H | | | |
| Set Block Lock Bit | 2 | 2 | Write | BA | 60H | Write | BA | 01H |
| Clear Block Lock Bit | 2 | 2,10 | Write | BA | 60H | Write | BA | D0H |
| Set Block Lock-down Bit | 2 | 2 | Write | BA | 60H | Write | BA | 2FH |
| OTP Program | 2 | 2,3,9 | Write | OA | C0H | Write | OA | OD |
| Set Partition Configuration Register | 2 | 2,3 | Write | PCRC | 60H | Write | PCRC | 04H |

Notes:

1. Bus operations are defined in 3.1 Bus Operation.
2. The address which is written at the first bus cycle should be the same as the address which is written at the second bus cycle.
   X=Any valid address within the device.
   PA=Address within the selected partition.
   IA=Identifier codes address (See 5.2 Identifier Codes and OTP Address for Read Operation).
   QA=Query codes address. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA=Address of OTP block to be read or programmed (See 5.3 OTP Block Address Map).
   PCRC=Partition configuration register code presented on the address $A_0$-$A_{15}$.
3. ID=Data read from identifier codes (See 5.2 Identifier Codes and OTP Address for Read Operation).
   QD=Data read from query database. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
   SRD=Data read from status register. See 6. Status Register Definition for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (whichever goes high first).
   OD=Data to be programmed at location OA. Data is latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (whichever goes high first).
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See 5.2 Identifier Codes and OTP Address for Read Operation).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when F-$\overline{RST}$ is $V_{IH}$.

6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, inputs the program sequential address and write data of "N" times. Finally, input the any valid address within the target partition to be programmed and the confirm command (D0H). Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when F-$\overline{WP}$ is $V_{IL}$.
    When F-$\overline{WP}$ is $V_{IH}$, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

5.2 Identifier Codes and OTP Address for Read Operation

| | Code | Address [$A_{15}$-$A_0$](4) | Data [$DQ_{15}$-$DQ_0$] | Notes |
|---|---|---|---|---|
| Manufacturer Code | Manufacturer Code | 0000H | 00B0H | |
| Device Code | 32M Bottom Parameter Device Code | 0001H | 00B5H | 1 |
| Block Lock Configuration Code | Block is Unlocked | Block Address + 2 | $DQ_0$ = 0 | 2 |
| | Block is Locked | | $DQ_0$ = 1 | 2 |
| | Block is not Locked-Down | | $DQ_1$ = 0 | 2 |
| | Block is Locked-Down | | $DQ_1$ = 1 | 2 |
| Device Configuration Code | Partition Configuration Register | 0006H | PCRC | 3 |
| OTP | OTP Lock | 0080H | OTP-LK | 5 |
| | OTP | 0081-0088H | OTP | 6 |

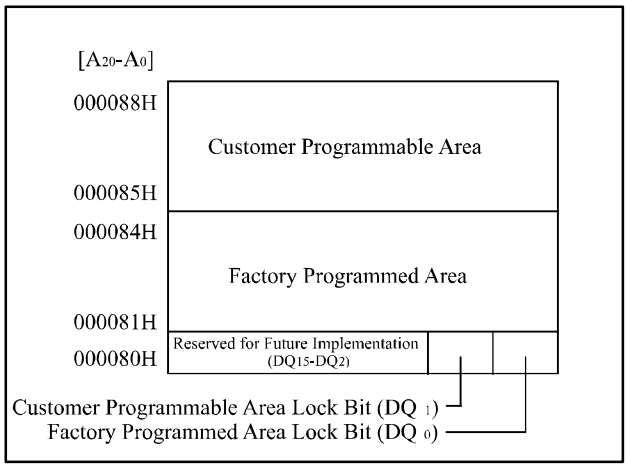
Notes:

1. Bottom parameter device has its parameter blocks in the plane 0 (The lowest address).
2. $DQ_{15}$-$DQ_2$ is reserved for future implementation.
3. PCRC=Partition Configuration Register Code.
4. The address $A_{20}$-$A_{16}$ are shown in below table for reading the manufacturer, device, lock configuration, device configuration code and OTP data.
   The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
   See Chapter 6. Partition Configuration Register Definition (P.15) for the partition configuration register.
5. OTP-LK=OTP Block Lock configuration.
6. OTP=OTP Block data.

Identifier Codes and OTP Address for Read Operation on Partition Configuration (32M-bit device)

| Partition Configuration Register | | | Address (32M-bit device) [$A_{20}$-$A_{16}$] |
|---|---|---|---|
| PCR.10 | PCR.9 | PCR.8 | |
| 0 | 0 | 0 | 00H |
| 0 | 0 | 1 | 00H or 08H |
| 0 | 1 | 0 | 00H or 10H |
| 1 | 0 | 0 | 00H or 18H |
| 0 | 1 | 1 | 00H or 08H or 10H |
| 1 | 1 | 0 | 00H or 10H or 18H |
| 1 | 0 | 1 | 00H or 08H or 18H |
| 1 | 1 | 1 | 00H or 08H or 10H or 18H |

5.3 OTP Block Address Map




OTP Block Address Map for OTP Program
(The area outside 80H - 88H cannot be used.)

5.4 Functions of Block Lock(1) and Block Lock-Down

| Current State | | | | | Erase/Program Allowed(3) |
|---|---|---|---|---|---|
| State | F-$\overline{WP}$ | $DQ_1$(2) | $DQ_0$(2) | State Name | |
| [000] | 0 | 0 | 0 | Unlocked | Yes |
| [001](4) | 0 | 0 | 1 | Locked | No |
| [011] | 0 | 1 | 1 | Locked-down | No |
| [100] | 1 | 0 | 0 | Unlocked | Yes |
| [101](4) | 1 | 0 | 1 | Locked | No |
| [110](5) | 1 | 1 | 0 | Lock-down Disable | Yes |
| [111] | 1 | 1 | 1 | Lock-down Disable | No |

Notes:

1. OTP (One Time Program) block has the lock function which is different from those described above.
2. $DQ_0$ = 1: a block is locked; $DQ_0$ = 0: a block is unlocked.
   $DQ_1$ = 1: a block is locked-down; $DQ_1$ = 0: a block is not locked-down.
3. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
4. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (F-$\overline{WP}$ = 0) or [101] (F-$\overline{WP}$ = 1), regardless of the states before power-off or reset operation.
5. When F-$\overline{WP}$ is driven to $V_{IL}$ in [110] state, the state changes to [011] and the blocks are automatically locked.

5.5 Block Locking State Transitions upon Command Write[4]

| Current State | | | | Result after Lock Command Written (Next State) | | |
|---|---|---|---|---|---|---|
| State | F-$\overline{WP}$ | $DQ_1$ | $DQ_0$ | Set Lock[1] | Clear Lock[1] | Set Lock-down[1] |
| [000] | 0 | 0 | 0 | [001] | No Change | [011][2] |
| [001] | 0 | 0 | 1 | No Change[3] | [000] | [011] |
| [011] | 0 | 1 | 1 | No Change | No Change | No Change |
| [100] | 1 | 0 | 0 | [101] | No Change | [111][2] |
| [101] | 1 | 0 | 1 | No Change | [100] | [111] |
| [110] | 1 | 1 | 0 | [111] | No Change | [111][2] |
| [111] | 1 | 1 | 1 | No Change | [110] | No Change |

Notes:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block ($DQ_0$ = 0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that F-$\overline{WP}$ is not changed and fixed $V_{IL}$ or $V_{IH}$.

5.6 Block Locking State Transitions upon F-$\overline{WP}$ Transition[4]

| Previous State | Current State | | | | Result after F-$\overline{WP}$ Transition (Next State) | |
|---|---|---|---|---|---|---|
| | State | F-$\overline{WP}$ | $DQ_1$ | $DQ_0$ | F-$\overline{WP}$ = 0→1[1] | F-$\overline{WP}$ = 1→0[1] |
| - | [000] | 0 | 0 | 0 | [100] | - |
| - | [001] | 0 | 0 | 1 | [101] | - |
| [110][2] | [011] | 0 | 1 | 1 | [110] | - |
| Other than [110][2] | | | | | [111] | - |
| - | [100] | 1 | 0 | 0 | - | [000] |
| - | [101] | 1 | 0 | 1 | - | [001] |
| - | [110] | 1 | 1 | 0 | - | [011][3] |
| - | [111] | 1 | 1 | 1 | - | [011] |

Notes:

1. "F-$\overline{WP}$ = 0→1" means that F-$\overline{WP}$ is driven to $V_{IH}$ and "F-$\overline{WP}$ = 1→0" means that F-$\overline{WP}$ is driven to $V_{IL}$.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When F-$\overline{WP}$ is driven to $V_{IL}$ in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

6. Status Register Definition

Status Register Definition

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| WSMS | BESS | BEFCES | PBPOPS | VPPS | PBPSS | DPS | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES)
1 = Error in Block Erase or Full Chip Erase
0 = Successful Block Erase or Full Chip Erase

SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS)
1 = Error in (Page Buffer) Program or OTP Program
0 = Successful (Page Buffer) Program or OTP Program

SR.3 = F-$V_{PP}$ STATUS (VPPS)
1 = F-$V_{PP}$ LOW Detect, Operation Abort
0 = F-$V_{PP}$ OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
1 = (Page Buffer) Program Suspended
0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)
1 = Erase or Program Attempted on a Locked Block, Operation Abort
0 = Unlocked

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:

Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.

Check SR.7 or F-RY/$\overline{BY}$ to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7= "0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, page buffer program, set/clear block lock bit, set block lock-down bit or set partition configuration register attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of F-$V_{PP}$ level. The WSM interrogates and indicates the F-$V_{PP}$ level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when F-$V_{PP} \neq V_{PPH1/2}$ or $V_{PPLK}$.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Extended Status Register Definition

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SMS | R | R | R | R | R | R | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| | |
|---|---|
| XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)<br><br>XSR.7 = STATE MACHINE STATUS (SMS)<br>1 = Page Buffer Program available<br>0 = Page Buffer Program not available<br><br>XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | Notes:<br><br>After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.<br><br>XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register. |

Partition Configuration Register Definition

| R | R | R | R | R | PC2 | PC1 | PC0 |
|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| R | R | R | R | R | R | R | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)
- 000 = No partitioning. Dual Work is not allowed.
- 001 = Plane1-3 are merged into one partition. (default in a bottom parameter device)
- 010 = Plane 0-1 and Plane2-3 are merged into one partition respectively.
- 100 = Plane 0-2 are merged into one partition. (default in a top parameter device)
- 011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:
After power-up or device reset, PCR10-8 (PC2-0) is set to "001" in a bottom parameter device and "100" in a top parameter device.

See the table below for more details.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when polling the partition configuration register.

Partition Configuration

| PC2 PC1 PC0 | PARTITIONING FOR DUAL WORK | PC2 PC1 PC0 | PARTITIONING FOR DUAL WORK |
|---|---|---|---|
| 0 0 0 | PARTITION0: PLANE3, PLANE2, PLANE1, PLANE0 | 0 1 1 | PARTITION2: PLANE3, PLANE2 / PARTITION1: PLANE1 / PARTITION0: PLANE0 |
| 0 0 1 | PARTITION1: PLANE3, PLANE2, PLANE1 / PARTITION0: PLANE0 | 1 1 0 | PARTITION2: PLANE3 / PARTITION1: PLANE2 / PARTITION0: PLANE1, PLANE0 |
| 0 1 0 | PARTITION1: PLANE3, PLANE2 / PARTITION0: PLANE1, PLANE0 | 1 0 1 | PARTITION2: PLANE3 / PARTITION1: PLANE2, PLANE1 / PARTITION0: PLANE0 |
| 1 0 0 | PARTITION1: PLANE3 / PARTITION0: PLANE2, PLANE1, PLANE0 | 1 1 1 | PARTITION3: PLANE3 / PARTITION2: PLANE2 / PARTITION1: PLANE1 / PARTITION0: PLANE0 |

7. Memory Map for Flash Memory

Bottom Parameter

| | BLOCK NUMBER | | ADDRESS RANGE |
|---|---|---|---|
| PLANE3 (UNIFORM PLANE) | 70 | 32K-WORD | 1F8000h - 1FFFFFh |
| | 69 | 32K-WORD | 1F0000h - 1F7FFFh |
| | 68 | 32K-WORD | 1E8000h - 1EFFFFh |
| | 67 | 32K-WORD | 1E0000h - 1E7FFFh |
| | 66 | 32K-WORD | 1D8000h - 1DFFFFh |
| | 65 | 32K-WORD | 1D0000h - 1D7FFFh |
| | 64 | 32K-WORD | 1C8000h - 1CFFFFh |
| | 63 | 32K-WORD | 1C0000h - 1C7FFFh |
| | 62 | 32K-WORD | 1B8000h - 1BFFFFh |
| | 61 | 32K-WORD | 1B0000h - 1B7FFFh |
| | 60 | 32K-WORD | 1A8000h - 1AFFFFh |
| | 59 | 32K-WORD | 1A0000h - 1A7FFFh |
| | 58 | 32K-WORD | 198000h - 19FFFFh |
| | 57 | 32K-WORD | 190000h - 197FFFh |
| | 56 | 32K-WORD | 188000h - 18FFFFh |
| | 55 | 32K-WORD | 180000h - 187FFFh |
| PLANE2 (UNIFORM PLANE) | 54 | 32K-WORD | 178000h - 17FFFFh |
| | 53 | 32K-WORD | 170000h - 177FFFh |
| | 52 | 32K-WORD | 168000h - 16FFFFh |
| | 51 | 32K-WORD | 160000h - 167FFFh |
| | 50 | 32K-WORD | 158000h - 15FFFFh |
| | 49 | 32K-WORD | 150000h - 157FFFh |
| | 48 | 32K-WORD | 148000h - 14FFFFh |
| | 47 | 32K-WORD | 140000h - 147FFFh |
| | 46 | 32K-WORD | 138000h - 13FFFFh |
| | 45 | 32K-WORD | 130000h - 137FFFh |
| | 44 | 32K-WORD | 128000h - 12FFFFh |
| | 43 | 32K-WORD | 120000h - 127FFFh |
| | 42 | 32K-WORD | 118000h - 11FFFFh |
| | 41 | 32K-WORD | 110000h - 117FFFh |
| | 40 | 32K-WORD | 108000h - 10FFFFh |
| | 39 | 32K-WORD | 100000h - 107FFFh |

| | BLOCK NUMBER | | ADDRESS RANGE |
|---|---|---|---|
| PLANE1 (UNIFORM PLANE) | 38 | 32K-WORD | 0F8000h - 0FFFFFh |
| | 37 | 32K-WORD | 0F0000h - 0F7FFFh |
| | 36 | 32K-WORD | 0E8000h - 0EFFFFh |
| | 35 | 32K-WORD | 0E0000h - 0E7FFFh |
| | 34 | 32K-WORD | 0D8000h - 0DFFFFh |
| | 33 | 32K-WORD | 0D0000h - 0D7FFFh |
| | 32 | 32K-WORD | 0C8000h - 0CFFFFh |
| | 31 | 32K-WORD | 0C0000h - 0C7FFFh |
| | 30 | 32K-WORD | 0B8000h - 0BFFFFh |
| | 29 | 32K-WORD | 0B0000h - 0B7FFFh |
| | 28 | 32K-WORD | 0A8000h - 0AFFFFh |
| | 27 | 32K-WORD | 0A0000h - 0A7FFFh |
| | 26 | 32K-WORD | 098000h - 09FFFFh |
| | 25 | 32K-WORD | 090000h - 097FFFh |
| | 24 | 32K-WORD | 088000h - 08FFFFh |
| | 23 | 32K-WORD | 080000h - 087FFFh |
| PLANE0 (PARAMETER PLANE) | 22 | 32K-WORD | 078000h - 07FFFFh |
| | 21 | 32K-WORD | 070000h - 077FFFh |
| | 20 | 32K-WORD | 068000h - 06FFFFh |
| | 19 | 32K-WORD | 060000h - 067FFFh |
| | 18 | 32K-WORD | 058000h - 05FFFFh |
| | 17 | 32K-WORD | 050000h - 057FFFh |
| | 16 | 32K-WORD | 048000h - 04FFFFh |
| | 15 | 32K-WORD | 040000h - 047FFFh |
| | 14 | 32K-WORD | 038000h - 03FFFFh |
| | 13 | 32K-WORD | 030000h - 037FFFh |
| | 12 | 32K-WORD | 028000h - 02FFFFh |
| | 11 | 32K-WORD | 020000h - 027FFFh |
| | 10 | 32K-WORD | 018000h - 01FFFFh |
| | 9 | 32K-WORD | 010000h - 017FFFh |
| | 8 | 32K-WORD | 008000h - 00FFFFh |
| | 7 | 4K-WORD | 007000h - 007FFFh |
| | 6 | 4K-WORD | 006000h - 006FFFh |
| | 5 | 4K-WORD | 005000h - 005FFFh |
| | 4 | 4K-WORD | 004000h - 004FFFh |
| | 3 | 4K-WORD | 003000h - 003FFFh |
| | 2 | 4K-WORD | 002000h - 002FFFh |
| | 1 | 4K-WORD | 001000h - 001FFFh |
| | 0 | 4K-WORD | 000000h - 000FFFh |

8. Absolute Maximum Ratings

| Symbol | Parameter | Notes | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 1,2 | -0.2 to +3.9 | V |
| $V_{IN}$ | Input voltage | 1,2,3,4 | -0.2 to $V_{CC}$ +0.3 | V |
| $T_A$ | Operating temperature | | -25 to +85 | °C |
| $T_{STG}$ | Storage temperature | | -55 to +125 | °C |
| F-$V_{PP}$ | F-$V_{PP}$ voltage | 1,3,5 | -0.2 to +12.6 | V |

Notes:

1. The maximum applicable voltage on any pins with respect to GND.
2. Except F-$V_{PP}$.
3. -2.0V undershoot and $V_{CC}$ +2.0V overshoot are allowed when the pulse width is less than 20 nsec.
4. $V_{IN}$ should not be over $V_{CC}$ +0.3V.
5. Applying 12V ±0.3V to F-$V_{PP}$ during erase/write can only be done for a maximum of 1000 cycles on each block. F-$V_{PP}$ may be connected to 12V ±0.3V for total of 80 hours maximum. +12.6V overshoot is allowed when the pulse width is less than 20 nsec.

9. Recommended DC Operating Conditions

($T_A$ = -25°C to +85°C)

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 | 2.7 | 3.0 | 3.3 | V |
| $V_{PP}$ | F-$V_{PP}$ Voltage (Write Operation) | | 1.65 | | 3.3 | V |
| | F-$V_{PP}$ Voltage (Read Operation) | | 0 | | 3.3 | V |
| $V_{IH}$ | Input Voltage | 1 | 2.2 | | $V_{CC}$ +0.2 | V |
| $V_{IL}$ | Input Voltage | | -0.2 | | 0.6 | V |

Notes:

1. $V_{CC}$ is the lower of F-$V_{CC}$ or S-$V_{CC}$.
2. $V_{CC}$ includes both F-$V_{CC}$ and S-$V_{CC}$.

10. Pin Capacitance(1)

($T_A$ = 25°C, f = 1MHz)

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | | | | 15 | pF | $V_{IN}$ = 0V |
| $C_{I/O}$ | I/O capacitance | | | | 25 | pF | $V_{I/O}$ = 0V |

Note:

1. Sampled but not 100% tested.

11. DC Electrical Characteristics[1]

DC Electrical Characteristics

($T_A$ = -25°C to +85°C, $V_{CC}$ = 2.7V to 3.3V)

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | | | | ±2 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{LO}$ | Output Leakage Current | | | | ±2 | µA | $V_{OUT}$ = $V_{CC}$ or GND |
| $I_{CCS}$ | F-$V_{CC}$ Standby Current | 2,9 | | 4 | 20 | µA | F-$V_{CC}$ = F-$V_{CC}$ Max., F-$\overline{CE}$ = F-$\overline{RST}$ = F-$V_{CC}$ ±0.2V, F-$\overline{WP}$ = F-$V_{CC}$ or GND |
| $I_{CCAS}$ | F-$V_{CC}$ Automatic Power Savings Current | 2,5 | | 4 | 20 | µA | F-$V_{CC}$ = F-$V_{CC}$ Max., F-$\overline{CE}$ = GND ±0.2V, F-$\overline{WP}$ = F-$V_{CC}$ or GND |
| $I_{CCD}$ | F-$V_{CC}$ Reset Power-Down Current | 2 | | 4 | 20 | µA | F-$\overline{RST}$ = GND ±0.2V $I_{OUT}$ (F-RY/$\overline{BY}$) = 0mA |
| $I_{CCR}$ | Average F-$V_{CC}$ Read Current Normal Mode | 2,8 | | 15 | 25 | mA | F-$V_{CC}$ = F-$V_{CC}$ Max., F-$\overline{CE}$ = $V_{IL}$, F-$\overline{OE}$ = $V_{IH}$, f = 5MHz $I_{OUT}$ = 0mA |
| | Average F-$V_{CC}$ Read Current Page Mode (8 Word Read) | 2,8 | | 5 | 10 | mA | |
| $I_{CCW}$ | F-$V_{CC}$ (Page Buffer) Program Current | 2,6,8 | | 20 | 60 | mA | F-$V_{PP}$ = $V_{PPH1}$ |
| | | 2,6,8 | | 10 | 20 | mA | F-$V_{PP}$ = $V_{PPH2}$ |
| $I_{CCE}$ | F-$V_{CC}$ Block Erase, Full Chip Erase Current | 2,6,8 | | 10 | 30 | mA | F-$V_{PP}$ = $V_{PPH1}$ |
| | | 2,6,8 | | 10 | 30 | mA | F-$V_{PP}$ = $V_{PPH2}$ |
| $I_{CCWS}$ $I_{CCES}$ | F-$V_{CC}$ (Page Buffer) Program or Block Erase Suspend Current | 2,3,8 | | 10 | 200 | µA | F-$\overline{CE}$ = $V_{IH}$ |
| $I_{PPS}$ $I_{PPR}$ | F-$V_{PP}$ Standby or Read Current | 2,7,8 | | 2 | 5 | µA | F-$V_{PP}$ ≤ F-$V_{CC}$ |
| $I_{PPW}$ | F-$V_{PP}$ (Page Buffer) Program Current | 2,6,7,8 | | 2 | 5 | µA | F-$V_{PP}$ = $V_{PPH1}$ |
| | | 2,6,7,8 | | 10 | 30 | mA | F-$V_{PP}$ = $V_{PPH2}$ |
| $I_{PPE}$ | F-$V_{PP}$ Block Erase, Full Chip Erase Current | 2,6,7,8 | | 2 | 5 | µA | F-$V_{PP}$ = $V_{PPH1}$ |
| | | 2,6,7,8 | | 5 | 15 | mA | F-$V_{PP}$ = $V_{PPH2}$ |
| $I_{PPWS}$ | F-$V_{PP}$ (Page Buffer) Program Suspend Current | 2,7,8 | | 2 | 5 | µA | F-$V_{PP}$ = $V_{PPH1}$ |
| | | 2,7,8 | | 10 | 200 | µA | F-$V_{PP}$ = $V_{PPH2}$ |
| $I_{PPES}$ | F-$V_{PP}$ Block Erase Suspend Current | 2,7,8 | | 2 | 5 | µA | F-$V_{PP}$ = $V_{PPH1}$ |
| | | 2,7,8 | | 10 | 200 | µA | F-$V_{PP}$ = $V_{PPH2}$ |

DC Electrical Characteristics (Continue)

($T_A$ = -25°C to +85°C, $V_{CC}$ = 2.7V to 3.3V)

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Conditions | |
|---|---|---|---|---|---|---|---|---|
| $I_{SB}$ | S-$V_{CC}$ Standby Current | | | 2 | 25 | µA | S-$\overline{CE}_1$, S-$CE_2$ ≥ S-$V_{CC}$ - 0.2V or S-$CE_2$ ≤ 0.2V | |
| $I_{SB1}$ | S-$V_{CC}$ Standby Current | | | | 3 | mA | S-$\overline{CE}_1$ = $V_{IH}$, S-$CE_2$ = $V_{IL}$ | |
| $I_{CC1}$ | S-$V_{CC}$ Operation Current | | | | 50 | mA | S-$\overline{CE}_1$ = $V_{IL}$, S-$CE_2$ = $V_{IH}$, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | $t_{CYCLE}$ = Min. $I_{I/O}$ = 0mA |
| $I_{CC2}$ | S-$V_{CC}$ Operation Current | | | | 8 | mA | S-$\overline{CE}_1$ ≤ 0.2V, S-$CE_2$ ≥ S-$V_{CC}$-0.2V, $V_{IN}$ ≥ S-$V_{CC}$-0.2V or ≤ 0.2V | $t_{CYCLE}$ = 1µs $I_{I/O}$ = 0mA |
| $V_{IL}$ | Input Low Voltage | 6 | -0.2 | | 0.6 | V | | |
| $V_{IH}$ | Input High Voltage | 6 | 2.2 | | Vcc +0.2 | V | | |
| $V_{OL}$ | Output Low Voltage | 6,9 | | | 0.4 | V | $I_{OL}$ = 0.5mA | |
| $V_{OH}$ | Output High Voltage | 6 | 2.4 | | | V | $I_{OH}$ = -0.5mA | |
| $V_{PPLK}$ | F-$V_{PP}$ Lockout during Normal Operations | 4,6,7 | | | 0.4 | V | | |
| $V_{PPH1}$ | F-$V_{PP}$ during Block Erase, Full Chip Erase,(PageBuffer) Program or OTP Program Operations | 7 | 1.65 | 3 | 3.3 | V | | |
| $V_{PPH2}$ | F-$V_{PP}$ during Block Erase, (PageBuffer) Program or OTP Program Operations | 7 | 11.7 | 12 | 12.3 | V | | |
| $V_{LKO}$ | F-$V_{CC}$ Lockout Voltage | | 1.5 | | | V | | |

Notes:

1. $V_{CC}$ includes both F-$V_{CC}$ and S-$V_{CC}$.
2. All currents are in RMS unless otherwise noted. Typical values are the reference values at $V_{CC}$ = 3.0V and $T_A$=+25°C unless $V_{CC}$ is specified.
3. $I_{CCWS}$ and $I_{CCES}$ are specified with the device de-selected. If read or (page buffer) program while in block erase suspend mode, the device's current draw is the sum of $I_{CCWS}$ or $I_{CCES}$ and $I_{CCR}$ or $I_{CCW}$, respectively.
4. Block erase, full chip erase, (page buffer) program and OTP program are inhibited when F-$V_{PP}$ ≤ $V_{PPLK}$, and not guaranteed in the range between $V_{PPLK}$ (max.) and $V_{PPH1}$ (min.) , between $V_{PPH1}$ (max.) and $V_{PPH2}$ (min.) and above $V_{PPH2}$ (max.).
5. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings ($t_{AVQV}$) provide new data when addresses are changed.
6. Sampled, not 100% tested.
7. F-$V_{PP}$ is not used for power supply pin. With F-$V_{PP}$ ≤ $V_{PPLK}$, block erase, full chip erase, (page buffer) program and OTP program cannot be executed and should not be attempted.
   Applying 12V ±0.3V to F-$V_{PP}$ provides fast erasing or fast programming mode. In this mode, F-$V_{PP}$ is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the $V_{CC}$ power bus.
   Applying 12V ±0.3V to F-$V_{PP}$ during erase/program can only be done for a maximum of 1000 cycles on each block.
   F-$V_{PP}$ may be connected to 12V ±0.3V for a total of 80 hours maximum.
8. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
9. Includes F-RY/$\overline{BY}$.

12. AC Electrical Characteristics for Flash Memory

12.1 AC Test Conditions

| | |
|---|---|
| Input pulse level | 0 V to 2.7 V |
| Input rise and fall time | 5 ns |
| Input and Output timing Ref. level | 1.35 V |
| Output load | 1TTL + $C_L$ (50pF) |

12.2 Read Cycle

($T_A$ = -25°C to +85°C, F-$V_{CC}$ = 2.7V to 3.3V)

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | Read Cycle Time | | 70 | | ns |
| $t_{AVQV}$ | Address to Output Delay | | | 70 | ns |
| $t_{ELQV}$ | F-$\overline{CE}$ to Output Delay | 2 | | 70 | ns |
| $t_{APA}$ | Page Address Access Time | | | 25 | ns |
| $t_{GLQV}$ | F-$\overline{OE}$ to Output Delay | 2 | | 20 | ns |
| $t_{PHQV}$ | F-$\overline{RST}$ High to Output Delay | | | 150 | ns |
| $t_{EHQZ}$, $t_{GHQZ}$ | F-$\overline{CE}$ or F-$\overline{OE}$ to Output in High - Z, Whichever Occurs First | 1 | | 20 | ns |
| $t_{ELQX}$ | F-$\overline{CE}$ to Output in Low - Z | 1 | 0 | | ns |
| $t_{GLQX}$ | F-$\overline{OE}$ to Output in Low - Z | 1 | 0 | | ns |
| $t_{OH}$ | Output Hold from First Occurring Address, F-$\overline{CE}$ or F-$\overline{OE}$ change | 1 | 0 | | ns |

Notes:

1. Sampled, not 100% tested.
2. F-$\overline{OE}$ may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of F-$\overline{CE}$ without impact to $t_{ELQV}$.

12.3 Write Cycle (F-$\overline{WE}$ / F-$\overline{CE}$ Controlled)[1,2]

($T_A$ = -25°C to +85°C, F-$V_{CC}$ = 2.7V to 3.3V)

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | Write Cycle Time | | 70 | | ns |
| $t_{PHWL}$ ($t_{PHEL}$) | F-$\overline{RST}$ High Recovery to F-$\overline{WE}$ (F-$\overline{CE}$) Going Low | 3 | 150 | | ns |
| $t_{ELWL}$ ($t_{WLEL}$) | F-$\overline{CE}$ (F-$\overline{WE}$) Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going Low | 4 | 0 | | ns |
| $t_{WLWH}$ ($t_{ELEH}$) | F-$\overline{WE}$ (F-$\overline{CE}$) Pulse Width | 4 | 60 | | ns |
| $t_{DVWH}$ ($t_{DVEH}$) | Data Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High | 8 | 40 | | ns |
| $t_{AVWH}$ ($t_{AVEH}$) | Address Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High | 8 | 50 | | ns |
| $t_{WHEH}$ ($t_{EHWH}$) | F-$\overline{CE}$ (F-$\overline{WE}$) Hold from F-$\overline{WE}$ (F-$\overline{CE}$) High | | 0 | | ns |
| $t_{WHDX}$ ($t_{EHDX}$) | Data Hold from F-$\overline{WE}$ (F-$\overline{CE}$) High | | 0 | | ns |
| $t_{WHAX}$ ($t_{EHAX}$) | Address Hold from F-$\overline{WE}$ (F-$\overline{CE}$) High | | 0 | | ns |
| $t_{WHWL}$ ($t_{EHEL}$) | F-$\overline{WE}$ (F-$\overline{CE}$) Pulse Width High | 5 | 30 | | ns |
| $t_{SHWH}$ ($t_{SHEH}$) | F-$\overline{WP}$ High Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High | 3 | 0 | | ns |
| $t_{VVWH}$ ($t_{VVEH}$) | F-$V_{PP}$ Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High | 3 | 200 | | ns |
| $t_{WHGL}$ ($t_{EHGL}$) | Write Recovery before Read | | 30 | | ns |
| $t_{QVSL}$ | F-$\overline{WP}$ High Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z | 3, 6 | 0 | | ns |
| $t_{QVVL}$ | F-$V_{PP}$ Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z | 3, 6 | 0 | | ns |
| $t_{WHR0}$ ($t_{EHR0}$) | F-$\overline{WE}$ (F-$\overline{CE}$) High to SR.7 Going "0" | 3, 7 | | $t_{AVQV}$+40 | ns |
| $t_{WHRL}$ ($t_{EHRL}$) | F-$\overline{WE}$ (F-$\overline{CE}$) High to F-RY/$\overline{BY}$ Going Low | 3 | | 100 | ns |

Notes:

1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. See the AC Characteristics for read cycle.
2. A write operation can be initiated and terminated with either F-$\overline{CE}$ or F-$\overline{WE}$.
3. Sampled, not 100% tested.
4. Write pulse width ($t_{WP}$) is defined from the falling edge of F-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes low last) to the rising edge of F-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high ($t_{WPH}$) is defined from the rising edge of F-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes high first) to the falling edge of F-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. F-$V_{PP}$ should be held at F-$V_{PP}$=$V_{PPH1/2}$ until determination of block erase, (page buffer) program or OTP program success (SR.1/3/4/5=0) and held at F-$V_{PP}$=$V_{PPH1}$ until determination of full chip erase or OTP program success (SR.1/3/5=0).
7. $t_{WHR0}$ ($t_{EHR0}$) after the Read Query or Read Identifier Codes/OTP command=$t_{AVQV}$+100ns.
8. See 5.1 Command Definitions for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.

12.4 Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance[3]

($T_A$ = -25°C to +85°C, F-$V_{CC}$ = 2.7V to 3.3V)

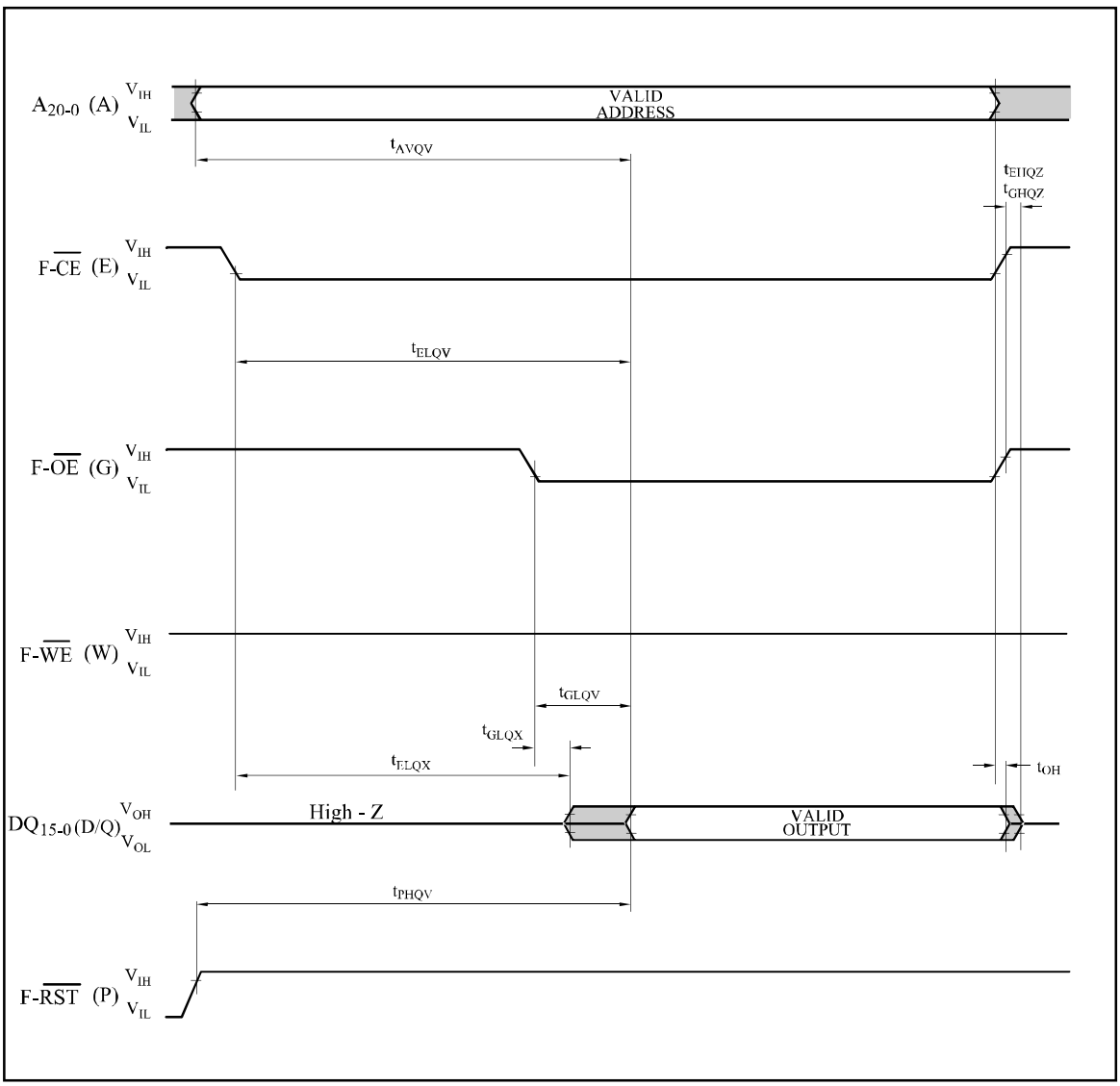
| Symbol | Parameter | Notes | Page Buffer Command is Used or not Used | F-$V_{PP}$=$V_{PPH1}$ (In System) | | | F-$V_{PP}$=$V_{PPH2}$ (In Manufacturing) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.[1] | Max.[2] | Min. | Typ.[1] | Max.[2] | |
| $t_{WPB}$ | 4K-Word Parameter Block Program Time | 2 | Not Used | | 0.05 | 0.3 | | 0.04 | 0.12 | s |
| | | 2 | Used | | 0.03 | 0.12 | | 0.02 | 0.06 | s |
| $t_{WMB}$ | 32K-Word Main Block Program Time | 2 | Not Used | | 0.38 | 2.4 | | 0.31 | 1 | s |
| | | 2 | Used | | 0.24 | 1 | | 0.17 | 0.5 | s |
| $t_{WHQV1}$/ $t_{EHQV1}$ | Word Program Time | 2 | Not Used | | 11 | 200 | | 9 | 185 | µs |
| | | 2 | Used | | 7 | 100 | | 5 | 90 | µs |
| $t_{WHOV1}$/ $t_{EHOV1}$ | OTP Program Time | 2 | Not Used | | 36 | 400 | | 27 | 185 | µs |
| $t_{WHQV2}$/ $t_{EHQV2}$ | 4K-Word Parameter Block Erase Time | 2 | - | | 0.3 | 4 | | 0.2 | 4 | s |
| $t_{WHQV3}$/ $t_{EHQV3}$ | 32K-Word Main Block Erase Time | 2 | - | | 0.6 | 5 | | 0.5 | 5 | s |
| | Full Chip Erase Time | 2 | | | 40 | 350 | | | | s |
| $t_{WHRH1}$/ $t_{EHRH1}$ | (Page Buffer) Program Suspend Latency Time to Read | 4 | - | | 5 | 10 | | 5 | 10 | µs |
| $t_{WHRH2}$/ $t_{EHRH2}$ | Block Erase Suspend Latency Time to Read | 4 | - | | 5 | 20 | | 5 | 20 | µs |
| $t_{ERES}$ | Latency Time from Block Erase Resume Command to Block Erase Suspend Command | 5 | - | 500 | | | 500 | | | µs |

Notes:

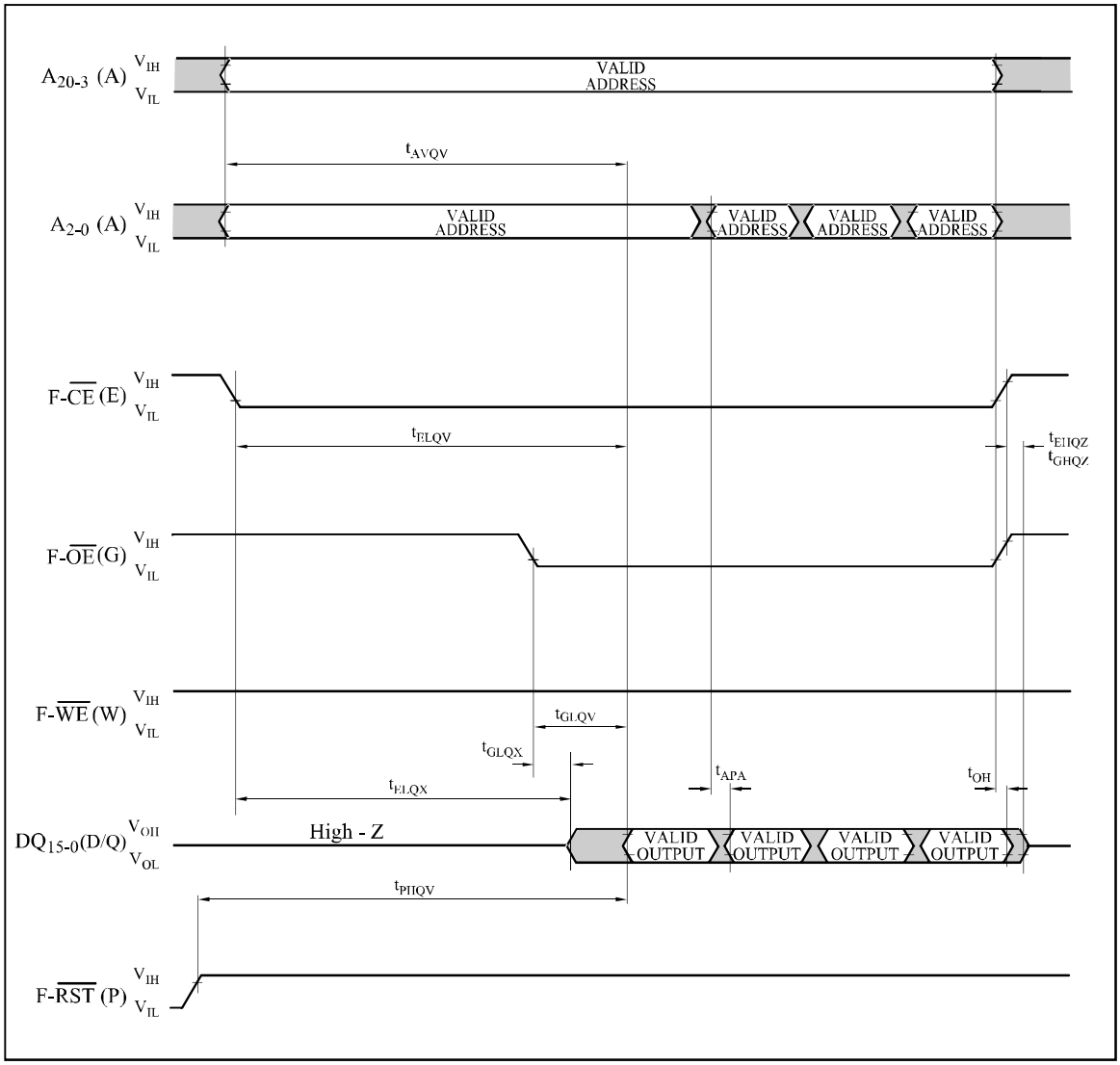
1. Typical values measured at F-$V_{CC}$ = 3.0V, F-$V_{PP}$ = 3.0V or 12V, and $T_A$= +25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (F-$\overline{WE}$ or F-$\overline{CE}$ going high) until SR.7 going "1" or F-RY/$\overline{BY}$ going High-Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than $t_{ERES}$ and its sequence is repeated, the block erase operation may not be finished.

12.5 Flash Memory AC Characteristics Timing Chart

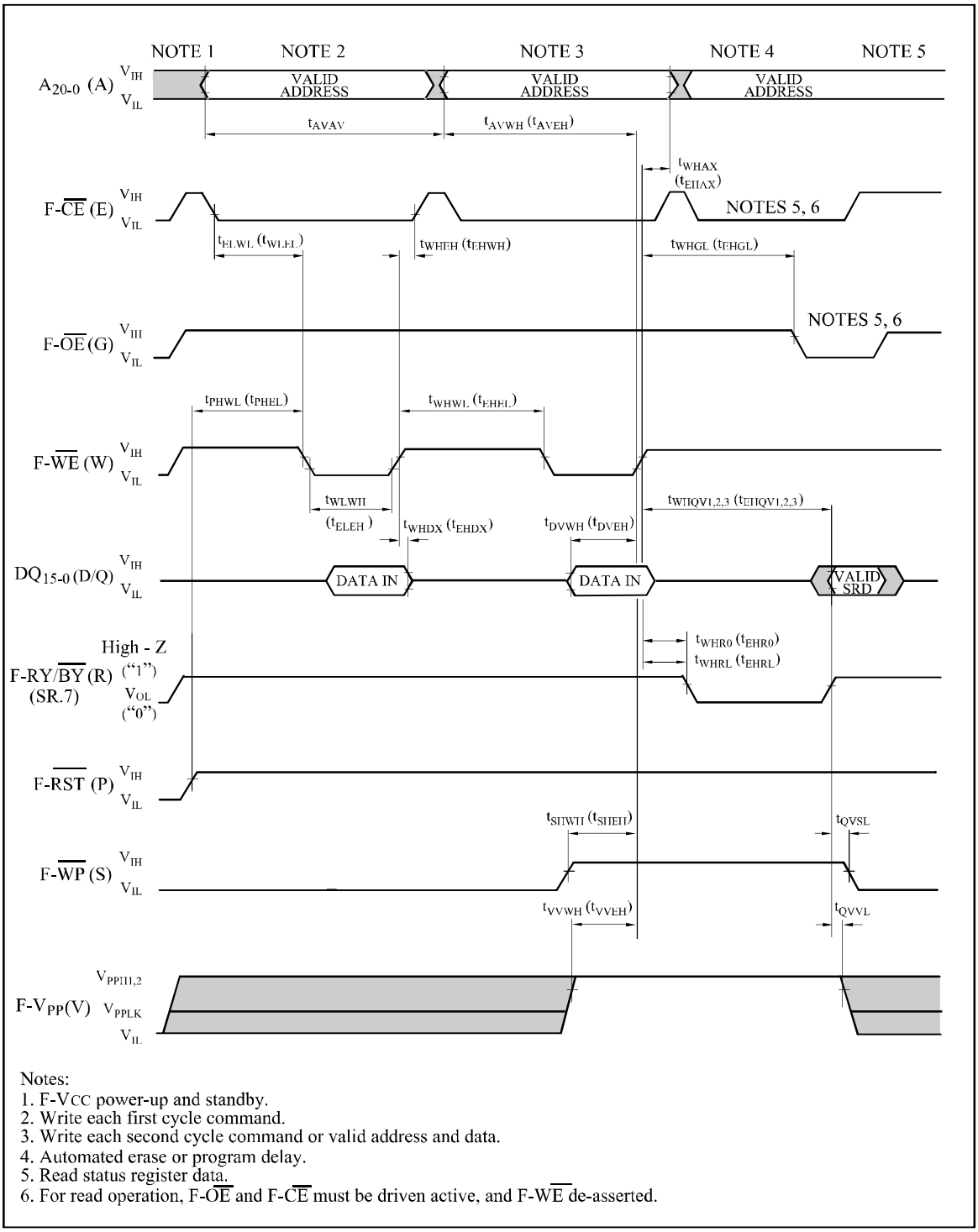
AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code



AC Waveform for Asynchronous Page Mode Read Operations from Main Blocks or Parameter Blocks



AC Waveform for Write Operations(F-$\overline{WE}$ / F-$\overline{CE}$ Controlled)




Notes:
1. F-$V_{CC}$ power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, F-$\overline{OE}$ and F-$\overline{CE}$ must be driven active, and F-$\overline{WE}$ de-asserted.

12.6 Reset Operations

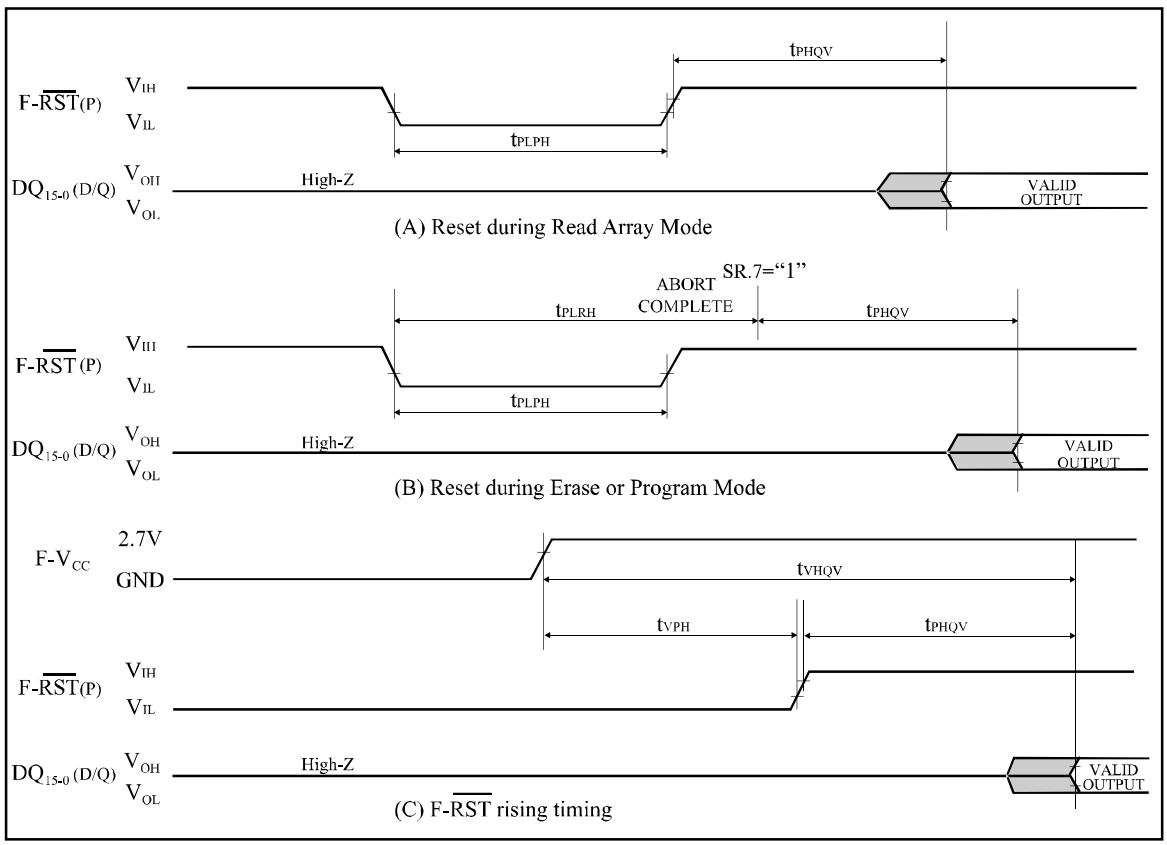
($T_A$ = -25°C to +85°C, F-$V_{CC}$ = 2.7V to 3.3V)

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{PLPH}$ | F-$\overline{RST}$ Low to Reset during Read (F-$\overline{RST}$ should be low during power-up.) | 1, 2, 3 | 100 | | ns |
| $t_{PLRH}$ | F-$\overline{RST}$ Low to Reset during Erase or Program | 1, 3, 4 | | 22 | µs |
| $t_{VPH}$ | F-$V_{CC}$ 2.7V to F-$\overline{RST}$ High | 1, 3, 5 | 100 | | ns |
| $t_{VHQV}$ | F-$V_{CC}$ 2.7V to Output Delay | 3 | | 1 | ms |

Notes:

1. A reset time, $t_{PHQV}$, is required from the later of SR.7 (F-RY/$\overline{BY}$) going "1" (High-Z) or F-$\overline{RST}$ going high until outputs are valid. See the AC Characteristics - read cycle for $t_{PHQV}$.
2. $t_{PLPH}$ is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If F-$\overline{RST}$ asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding F-$\overline{RST}$ low minimum 100ns is required after F-$V_{CC}$ has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



13. AC Electrical Characteristics for SRAM

13.1 AC Test Conditions

| | |
|---|---|
| Input pulse level | 0.4 V to 2.2 V |
| Input rise and fall time | 5 ns |
| Input and Output timing Ref. level | 1.5 V |
| Output load | 1TTL +$C_L$ (30pF)(1) |

Note:

1. Including scope and socket capacitance.

13.2 Read Cycle

($T_A$ = -25°C to +85°C, S-$V_{CC}$ = 2.7V to 3.3V)

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | | 70 | | ns |
| $t_{AA}$ | Address Access Time | | | 70 | ns |
| $t_{ACE1}$ | Chip Enable Access Time (S-$\overline{CE}_1$) | | | 70 | ns |
| $t_{ACE2}$ | Chip Enable Access Time (S-$CE_2$) | | | 70 | ns |
| $t_{BE}$ | Byte Enable Access Time | | | 70 | ns |
| $t_{OE}$ | Output Enable to Output Valid | | | 40 | ns |
| $t_{OH}$ | Output Hold from Address Change | | 10 | | ns |
| $t_{LZ1}$ | S-$\overline{CE}_1$ Low to Output Active | 1 | 10 | | ns |
| $t_{LZ2}$ | S-$CE_2$ High to Output Active | 1 | 10 | | ns |
| $t_{OLZ}$ | S-$\overline{OE}$ Low to Output Active | 1 | 5 | | ns |
| $t_{BLZ}$ | S-$\overline{UB}$ or S-$\overline{LB}$ Low to Output Active | 1 | 5 | | ns |
| $t_{HZ1}$ | S-$\overline{CE}_1$ High to Output in High-Z | 1 | 0 | 25 | ns |
| $t_{HZ2}$ | S-$CE_2$ Low to Output in High-Z | 1 | 0 | 25 | ns |
| $t_{OHZ}$ | S-$\overline{OE}$ High to Output in High-Z | 1 | 0 | 25 | ns |
| $t_{BHZ}$ | S-$\overline{UB}$ or S-$\overline{LB}$ High to Output in High-Z | 1 | 0 | 25 | ns |

Note:

1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

13.3 Write Cycle

($T_A$ = -25°C to +85°C, S-$V_{CC}$ = 2.7V to 3.3V)

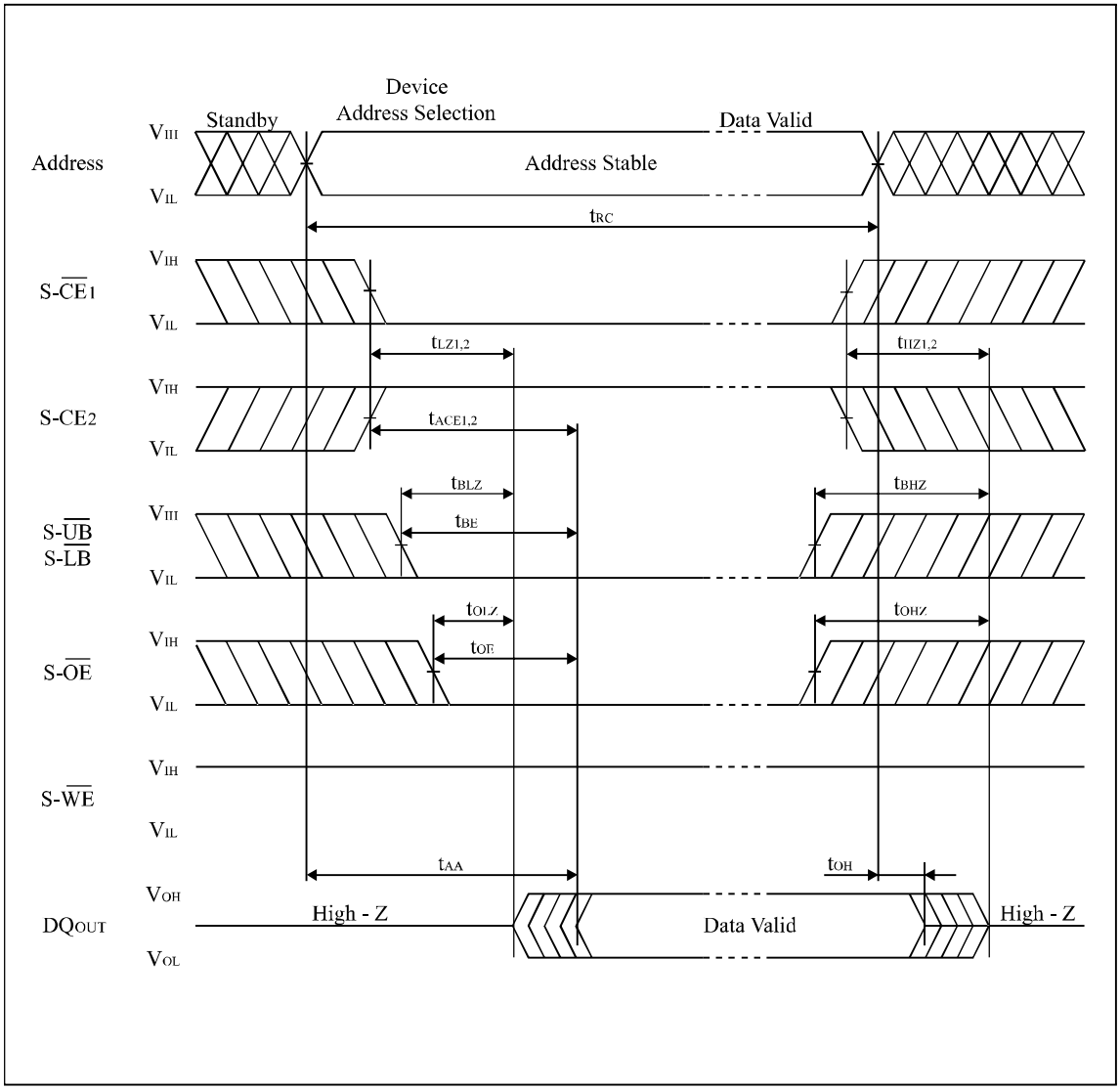
| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | | 70 | | ns |
| $t_{CW}$ | Chip Enable to End of Write | | 60 | | ns |
| $t_{AW}$ | Address Valid to End of Write | | 60 | | ns |
| $t_{BW}$ | Byte Select Time | | 55 | | ns |
| $t_{AS}$ | Address Setup Time | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | | 50 | | ns |
| $t_{WR}$ | Write Recovery Time | | 0 | | ns |
| $t_{DW}$ | Input Data Setup Time | | 30 | | ns |
| $t_{DH}$ | Input Data Hold Time | | 0 | | ns |
| $t_{OW}$ | S-$\overline{WE}$ High to Output Active | 1 | 5 | | ns |
| $t_{WZ}$ | S-$\overline{WE}$ Low to Output in High-Z | 1 | 0 | 25 | ns |

Note:

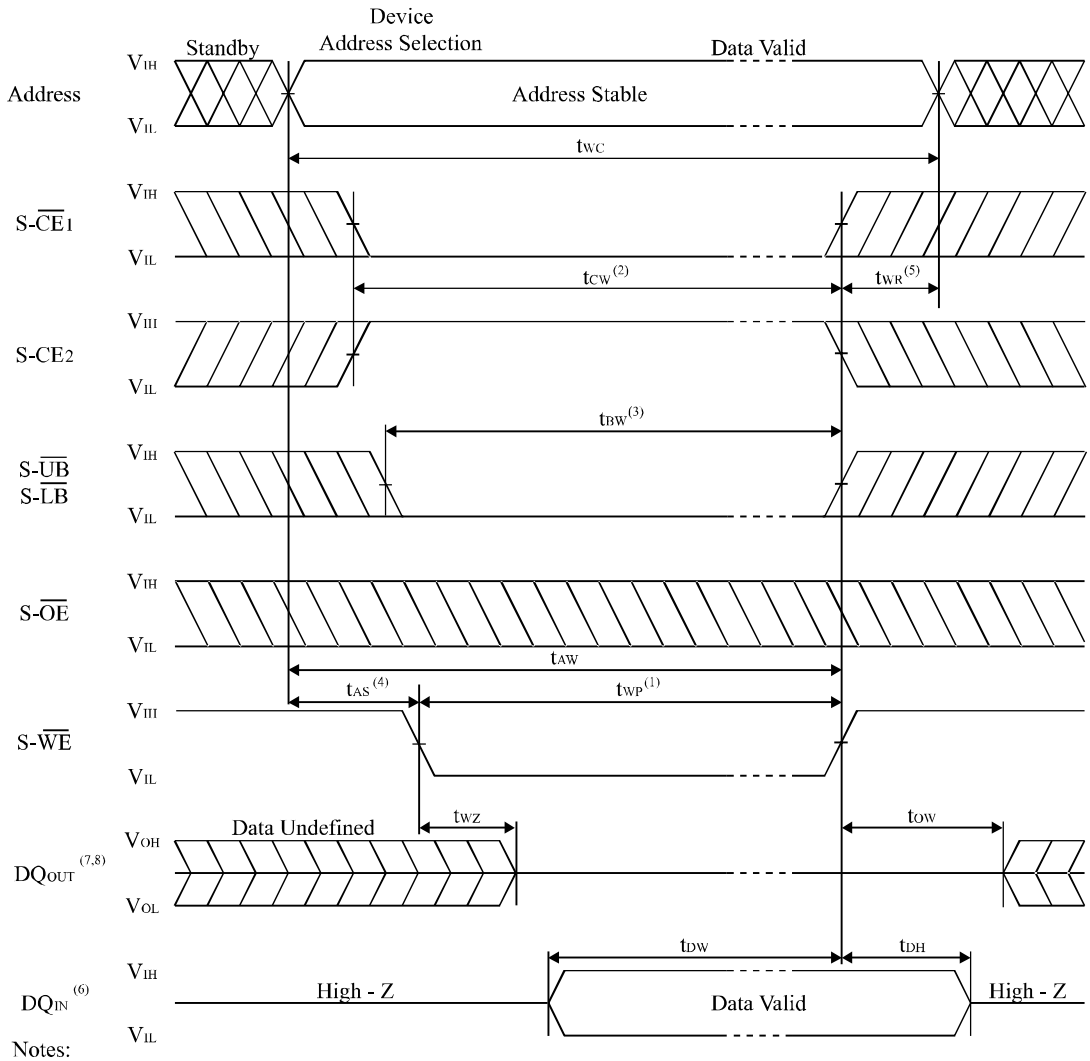
1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

13.4 SRAM AC Characteristics Timing Chart

Read Cycle Timing Chart



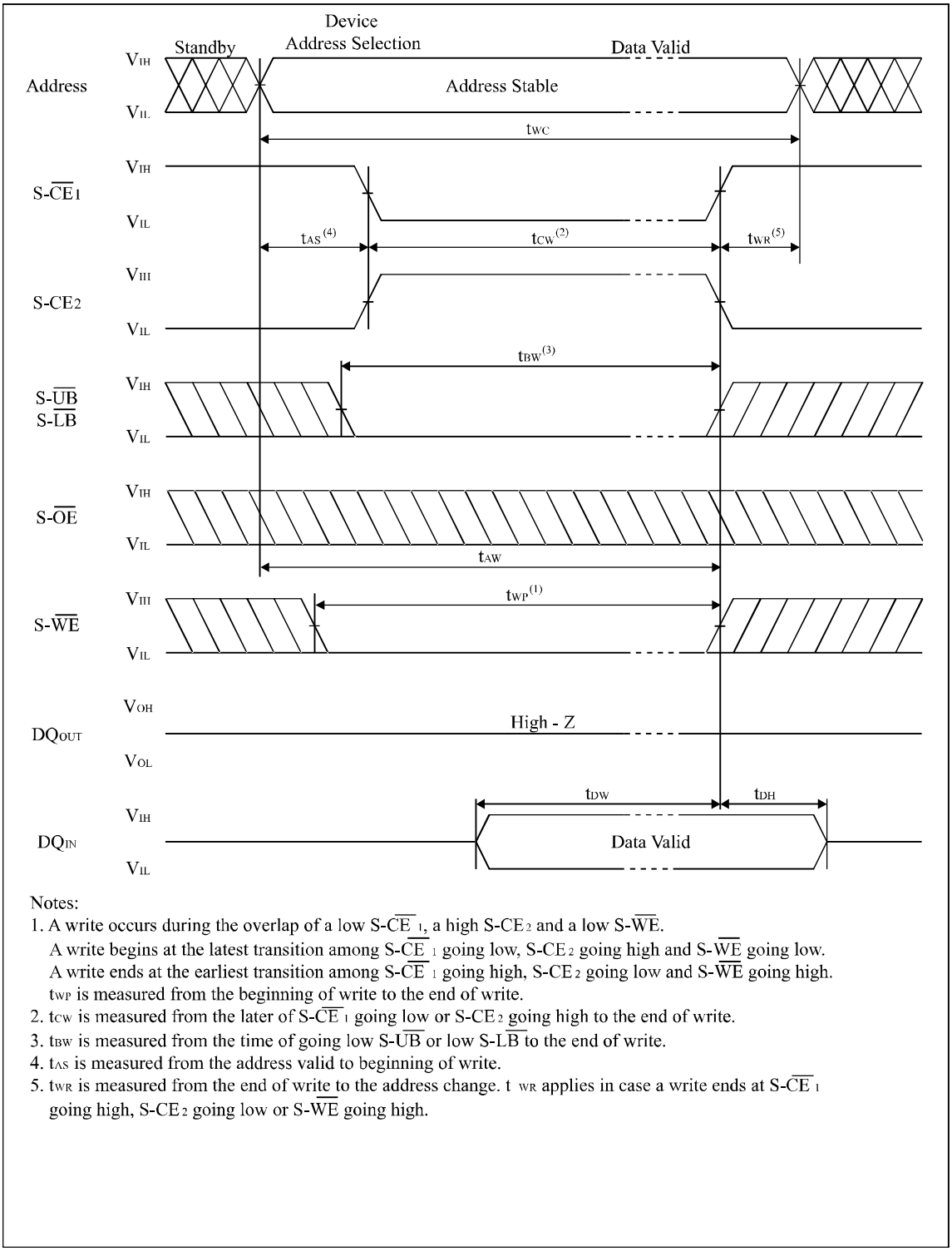
Write Cycle Timing Chart (S-$\overline{WE}$ Controlled)




Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-$CE_2$ and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-$CE_2$ going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-$CE_2$ going low and S-$\overline{WE}$ going high.
   $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the later of S-$\overline{CE}_1$ going low or S-$CE_2$ going high to the end of write.
3. $t_{BW}$ is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. $t_{AS}$ is measured from the address valid to beginning of write.
5. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applies in case a write ends at S-$\overline{CE}_1$ going high, S-$CE_2$ going low or S-$\overline{WE}$ going high.
6. During this period DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If S-$\overline{CE}_1$ goes low or S-$CE_2$ goes high simultaneously with S-$\overline{WE}$ going low or after S-$\overline{WE}$ going low, the outputs remain in high impedance state.
8. If S-$\overline{CE}_1$ goes high or S-$CE_2$ goes low simultaneously with S-$\overline{WE}$ going high or before S-$\overline{WE}$ going high, the outputs remain in high impedance state.

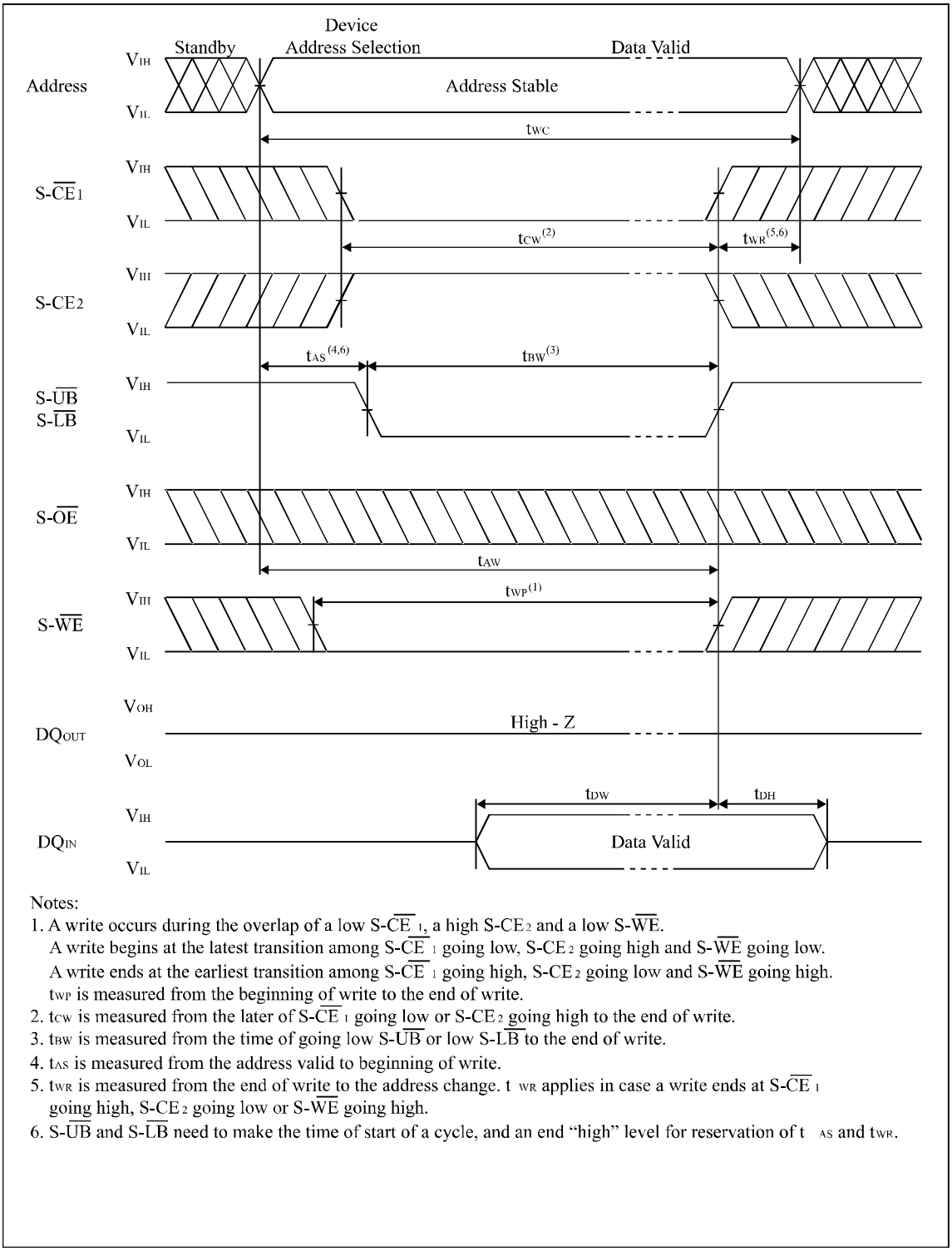
Write Cycle Timing Chart (S-$\overline{CE}$ Controlled)




Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-$CE_2$ and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-$CE_2$ going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-$CE_2$ going low and S-$\overline{WE}$ going high.
   $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the later of S-$\overline{CE}_1$ going low or S-$CE_2$ going high to the end of write.
3. $t_{BW}$ is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. $t_{AS}$ is measured from the address valid to beginning of write.
5. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applies in case a write ends at S-$\overline{CE}_1$ going high, S-$CE_2$ going low or S-$\overline{WE}$ going high.

Write Cycle Timing Chart (S-$\overline{UB}$, S-$\overline{LB}$ Controlled)




Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE$_2$ and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE$_2$ going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE$_2$ going low and S-$\overline{WE}$ going high.
   $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the later of S-$\overline{CE}_1$ going low or S-CE$_2$ going high to the end of write.
3. $t_{BW}$ is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. $t_{AS}$ is measured from the address valid to beginning of write.
5. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE$_2$ going low or S-$\overline{WE}$ going high.
6. S-$\overline{UB}$ and S-$\overline{LB}$ need to make the time of start of a cycle, and an end "high" level for reservation of $t_{AS}$ and $t_{WR}$.

14. Data Retention Characteristics for SRAM

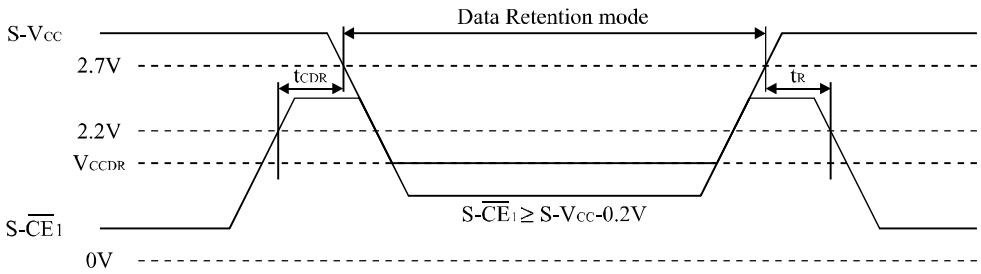
($T_A$ = -25°C to +85°C)

| Symbol | Parameter | Note | Min. | Typ.(1) | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{CCDR}$ | Data Retention Supply voltage | 2 | 1.5 | | 3.3 | V | S-$CE_2$ ≤ 0.2V or S-$\overline{CE}_1$ ≥ S-$V_{CC}$ - 0.2V |
| $I_{CCDR}$ | Data Retention Supply current | 2 | | 2 | 25 | µA | S-$V_{CC}$ = 3.0V, S-$CE_2$ ≤ 0.2V or S-$\overline{CE}_1$ ≥ S-$V_{CC}$ - 0.2V |
| $t_{CDR}$ | Chip enable setup time | | 0 | | | ns | |
| $t_R$ | Chip enable hold time | | $t_{RC}$ | | | ns | |

Notes

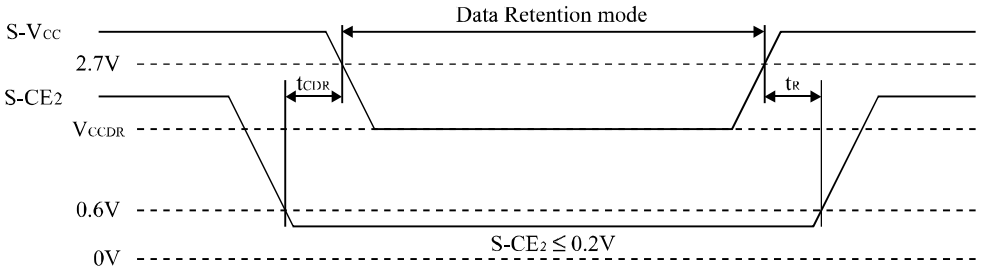
1. Reference value at $T_A$ = 25°C, S-$V_{CC}$ = 3.0V.
2. S-$\overline{CE}_1$ ≥ S-$V_{CC}$ - 0.2V, S-$CE_2$ ≥ S-$V_{CC}$ - 0.2V (S-$\overline{CE}_1$ controlled) or S-$CE_2$ ≤ 0.2V (S-$CE_2$ controlled).

Data Retention timing chart (S-$\overline{CE}_1$ Controlled)(1)




Note:
1. To control the data retention mode at S-$\overline{CE}_1$, fix the input level of S-$CE_2$ between "$V_{CCDR}$ and $V_{CCDR}$-0.2V" or "0V and 0.2V" during the data retention mode.

Data Retention timing chart (S-$CE_2$ Controlled)



15. Notes

This product is a stacked CSP package that a 32M (x16) bit Flash Memory and a 8M (x16) bit SRAM are assembled into.

- Supply Power

  Maximum difference (between F-$V_{CC}$ and S-$V_{CC}$) of the voltage is less than 0.3V.

- Power Supply and Chip Enable of Flash Memory and SRAM (F-$\overline{CE}$, S-$\overline{CE}_1$, S-$CE_2$)

  S-$\overline{CE}_1$ should not be “low” and S-$CE_2$ should not be “high” when F-$\overline{CE}$ is “low” simultaneously.

  If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

  Both F-$V_{CC}$ and S-$V_{CC}$ are needed to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

- Power Up Sequence

  When turning on Flash memory power supply, keep F-$\overline{RST}$ “low”. After F-$V_{CC}$ reaches over 2.7V, keep F-$\overline{RST}$ “low” for more than 100 nsec.

- Device Decoupling

  The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals (F-$\overline{CE}$, S-$\overline{CE}_1$, S-$CE_2$).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto F-$\overline{WE}$ signal or power supply, may be interpreted as false commands and causes undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate:

■ The below describes data protection method.

1. Protection of data in each block
   - Any locked block by setting its block lock bit is protected against the data alternation. When F-$\overline{WP}$ is low, any locked-down block by setting its block lock-down bit is protected from lock status changes.
     By using this function, areas can be defined, for example, program area (locked blocks), and data area (unlocked blocks).
   - For detailed block locking scheme, see Chapter 5.Command Definitions for Flash Memory.

2. Protection of data with F-$V_{PP}$ control
   - When the level of F-$V_{PP}$ is lower than $V_{PPLK}$ (F-$V_{PP}$ lockout voltage), write functions to all blocks including OTP block are disabled. All blocks are locked and the data in the blocks are completely protected.

3. Protection of data with F-$\overline{RST}$
   - Especially during power transitions such as power-up and power-down, the flash memory enters reset mode by bringing F-$\overline{RST}$ to low, which inhibits write operation to all blocks including OTP block.
   - For detailed description on F-$\overline{RST}$ control, see Chapter 12.6 AC Electrical Characteristics for Flash Memory, Reset Operations.

■ Protection against noises on F-$\overline{WE}$ signal

To prevent the recognition of false commands as write commands, system designer should consider the method for reducing noises on F-$\overline{WE}$ signal.

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a 0.1µF ceramic capacitor connected between its F-$V_{CC}$ and GND and between its F-$V_{PP}$ and GND.
Low inductance capacitors should be placed as close as possible to package leads.

2. F-$V_{PP}$ Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the F-$V_{PP}$ Power Supply trace. Use similar trace widths and layout considerations given to the F-$V_{CC}$ power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprograming "0" for the bit which has already been programed "0". Overwrite operation may generate unerasable bit.

In case of reprograming "0" to the data which has been programed "1".
- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programed "0".

For example, changing data from "1011110110111101" to "1010110110111100"
requires "1110111111111110" programing.

4. Power Supply

Block erase, full chip erase, word write and OTP program with an invalid F-$V_{PP}$ (See Chapter 11. DC Electrical Characteristics) produce spurious results and should not be attempted.
Device operations at invalid F-$V_{CC}$ voltage (See Chapter 11. DC Electrical Characteristics) produce spurious results and should not be attempted.

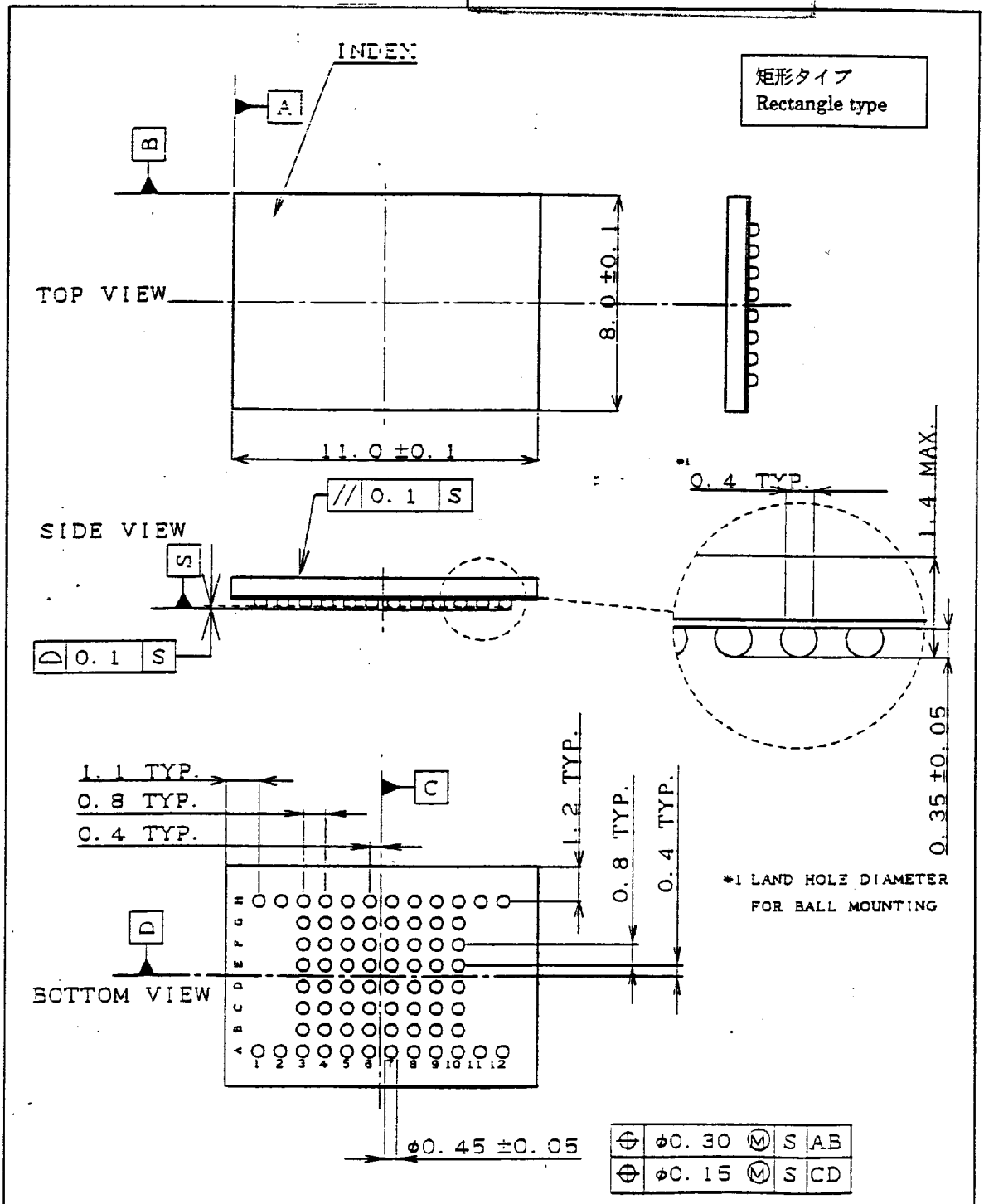
18. Related Document Information(1)

| Document No. | Document Name |
|---|---|
| FUM00701 | LH28F320BF, LH28F640BF, LH28F128BF Series Appendix |

Note:
1. International customers should contact their local SHARP or distribution sales offices.

SHARP

PRELIMINARY



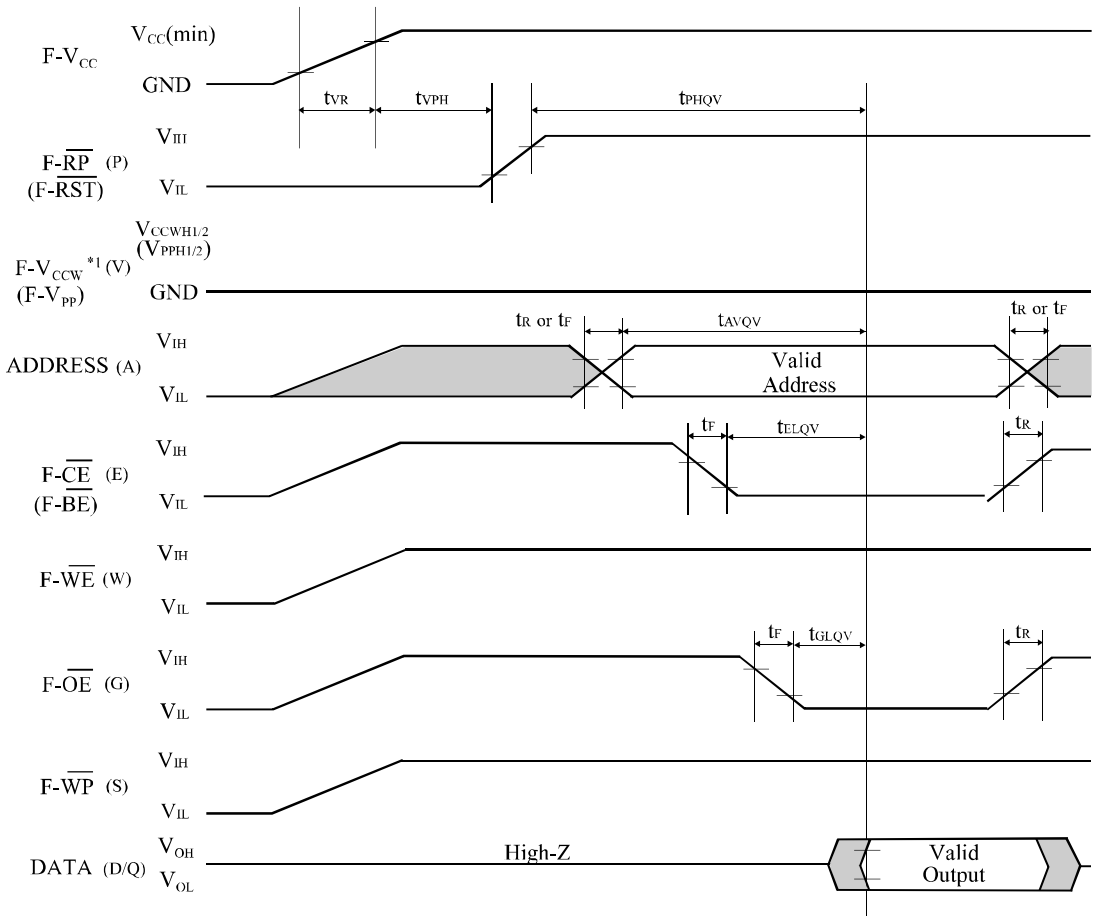

| | | | |
|---|---|---|---|
| 名称 NAME | FBGA072/064-P-0811(LCSP072/064-P-0811) | | 備考 NOTE |
| DRAWING NO. | AA2149 | 単位 UNIT | mm |

20010910

## A-1 RECOMMENDED OPERATING CONDITIONS

### A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.




*1 To prevent the unwanted writes, system designers should consider the design, which applies F-V CCW (F-VPP) to 0V during read operations and V CCWH1/2 (VPPH1/2) during write or erase operations.
See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications $t_{VR}$, $t_R$, $t_F$ in the figure, refer to the next page. See the "AC Electrical Characteristics for Flash Memory" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

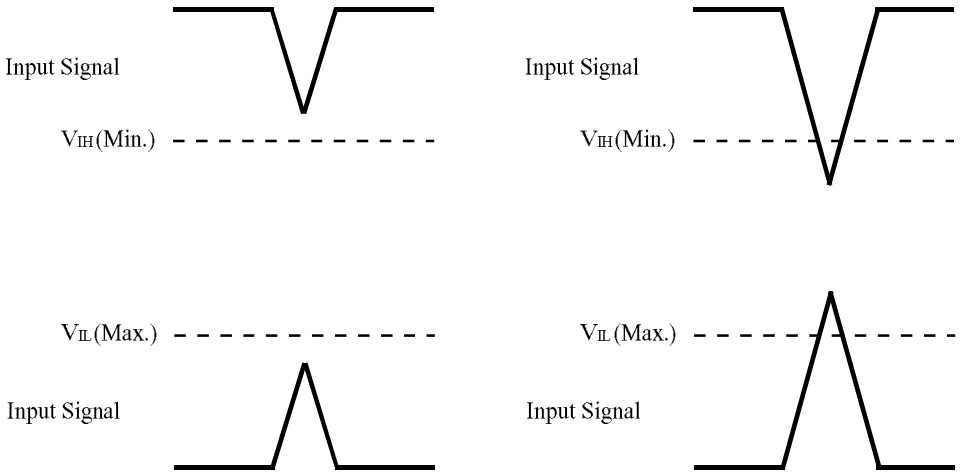
### A-1.1.1 Rise and Fall Time

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{VR}$ | F-$V_{CC}$ Rise Time | 1 | 0.5 | 30000 | µs/V |
| $t_R$ | Input Signal Rise Time | 1, 2 | | 1 | µs/V |
| $t_F$ | Input Signal Fall Time | 1, 2 | | 1 | µs/V |

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

## A-1.2 Glitch Noises

Do not input the glitch noises which are below $V_{IH}$ (Min.) or above $V_{IL}$ (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).




(a) Acceptable Glitch Noises (b) NOT Acceptable Glitch Noises

Figure A-2. Waveform for Glitch Noises

See the "DC Electrical Characteristics" described in specifications for $V_{IH}$ (Min.) and $V_{IL}$ (Max.).

## A-2 RELATED DOCUMENT INFORMATION(1)

| Document No. | Document Name |
|---|---|
| AP-001-SD-E | Flash Memory Family Software Drivers |
| AP-006-PT-E | Data Protection Method of SHARP Flash Memory |
| AP-007-SW-E | RP#, $V_{PP}$ Electric Potential Switching Circuit |

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

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