

FCP13N60N / FCPF13N60NT

N-Channel MOSFET

600V, 13A, 0.258Ω

Features

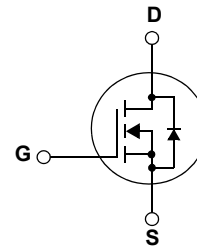
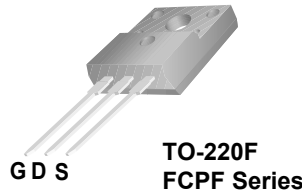
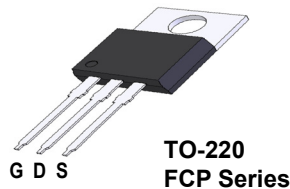
- $R_{DS(on)} = 0.244\Omega$ (Typ.) @ $V_{GS} = 10V$, $I_D = 6.5A$
- Ultra Low Gate Charge (Typ. $Q_g = 30.4nC$)
- Low Effective Output Capacitance
- 100% Avalanche Tested
- RoHS Compliant



Description

The SupreMOS MOSFET, Fairchild's next generation of high voltage super-junction MOSFETs, employs a deep trench filling process that differentiates it from preceding multi-epi based technologies. By utilizing this advanced technology and precise process control, SupreMOS provides world class R_{sp} , superior switching performance and ruggedness.

This SupreMOS MOSFET fits the industry's AC-DC SMPS requirements for PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	FCP13N60N	FCPF13N60NT	Units
V_{DSS}	Drain to Source Voltage	600		V
V_{GSS}	Gate to Source Voltage	±30		V
I_D	Drain Current	13	13*	A
	-Continuous ($T_C = 100^\circ C$)	8.2	8.2*	
I_{DM}	Drain Current - Pulsed (Note 1)	39	39	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	235		mJ
I_{AR}	Avalanche Current	4.3		A
E_{AR}	Repetitive Avalanche Energy	1.16		mJ
dv/dt	MOSFET dv/dt Ruggedness	100		V/ns
	Peak Diode Recovery dv/dt (Note 3)	20		V/ns
P_D	Power Dissipation	116	33.8	W
	- Derate above $25^\circ C$	0.93	0.27	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ C$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCP13N60N	FCPF13N60NT	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.07	3.7	$^\circ C/W$
$R_{\theta CS}$	Thermal Resistance, Case to Heat Sink (Typical)	0.5	0.5	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

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Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCP13N60N	FCP13N60N	TO-220	-	-	50
FCPF13N60NT	FCPF13N60NT	TO-220F	-	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{mA}$, $V_{GS} = 0\text{V}$, $T_C = 25^\circ\text{C}$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{mA}$, Referenced to 25°C	-	0.73	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{V}$, $V_{GS} = 0\text{V}$	-	-	10	μA
		$V_{DS} = 480\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 6.5\text{A}$	-	0.244	0.258	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{V}$, $I_D = 6.5\text{A}$	-	16.3	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	1325	1765	pF
C_{oss}	Output Capacitance		-	50	65	pF
C_{rss}	Reverse Transfer Capacitance		-	3	5	pF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	30	-	pF
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{V}$ to 480V , $V_{GS} = 0\text{V}$	-	145	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{V}$, $I_D = 6.5\text{A}$ $V_{GS} = 10\text{V}$ (Note 4)	-	30.4	39.5	nC
Q_{gs}	Gate to Source Gate Charge		-	6.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	9.5	-	nC
ESR	Equivalent Series Resistance (G-S)	Drain Open	-	2.8	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{V}$, $I_D = 6.5\text{A}$ $R_G = 4.7\Omega$ (Note 4)	-	14.5	39	ns
t_r	Turn-On Rise Time		-	10.6	31.2	ns
$t_{d(off)}$	Turn-Off Delay Time		-	45	100	ns
t_f	Turn-Off Fall Time		-	9.8	29.6	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	13	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	39	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 6.5A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 6.5A dI _F /dt = 100A/μs	-	287	-	ns
Q _{rr}	Reverse Recovery Charge		-	3.5	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 4.3\text{A}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 13\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

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Typical Performance Characteristics

Figure 1. On-Region Characteristics

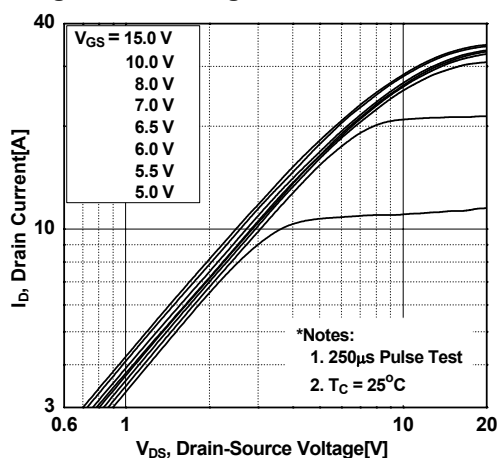


Figure 2. Transfer Characteristics

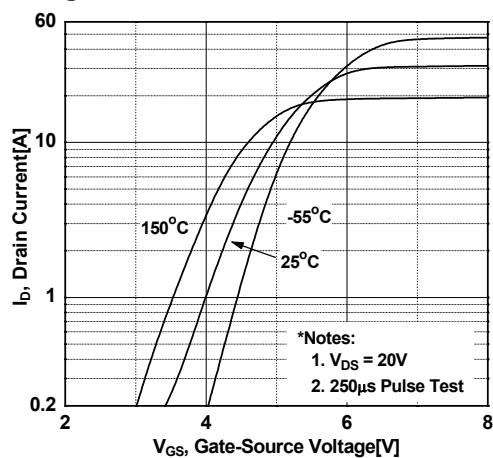


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

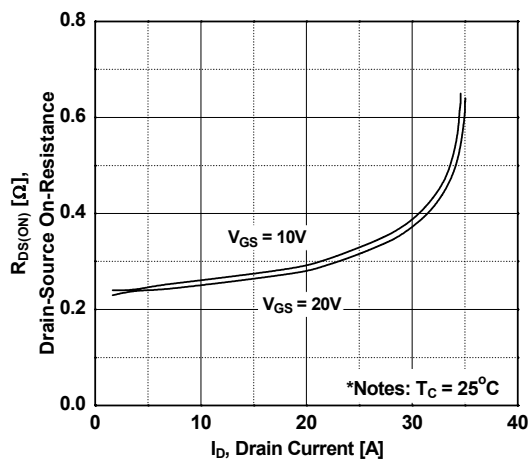


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

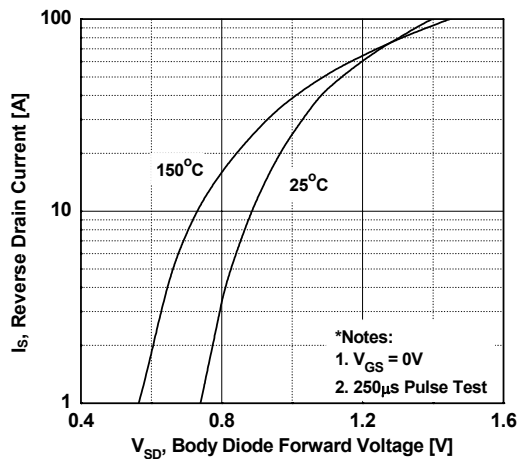


Figure 5. Capacitance Characteristics

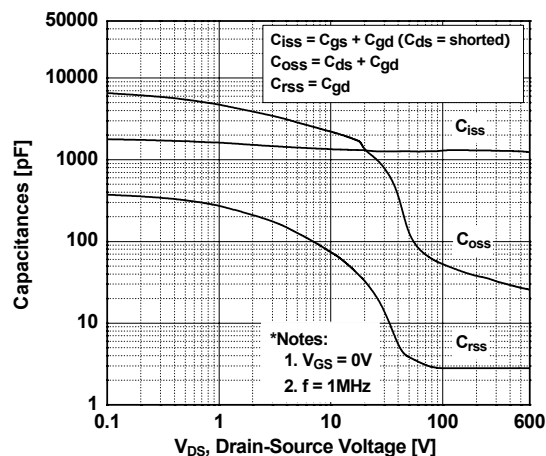
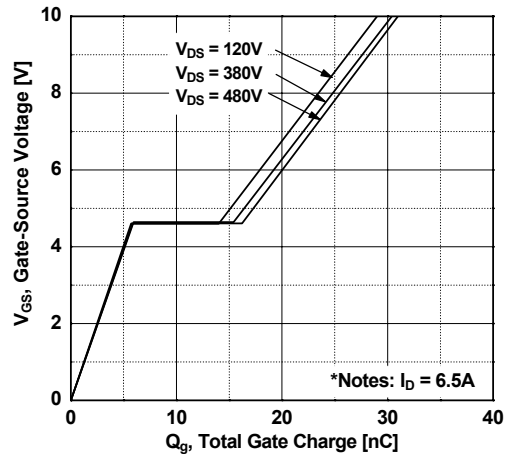


Figure 6. Gate Charge Characteristics



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Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

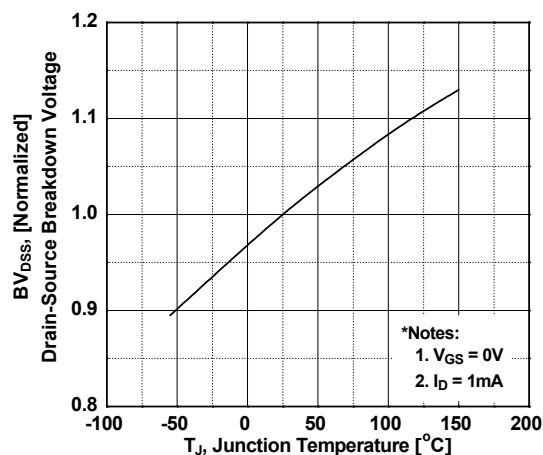


Figure 8. On-Resistance Variation vs. Temperature

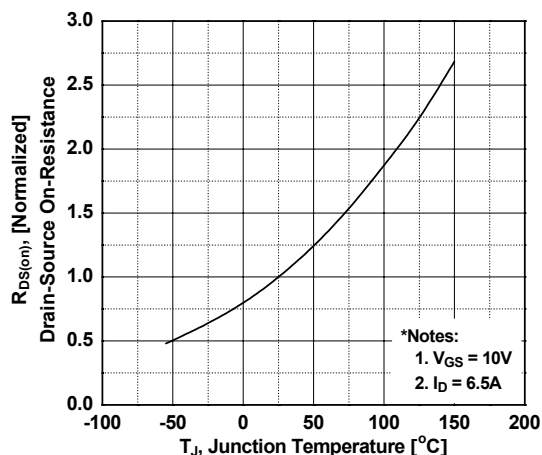


Figure 9. Maximum Safe Operating Area _ FCP13N60N

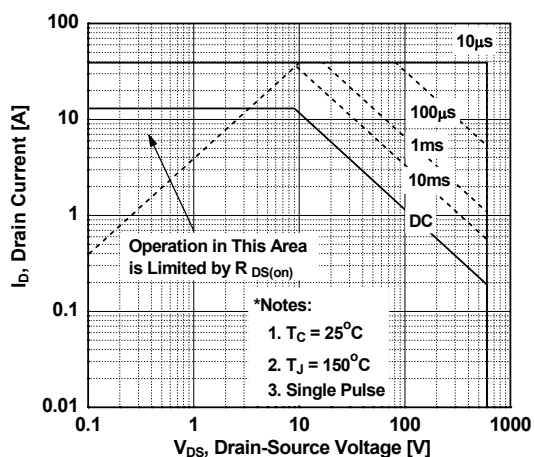


Figure 10. Maximum Safe Operating Area _ FCPF13N60NT

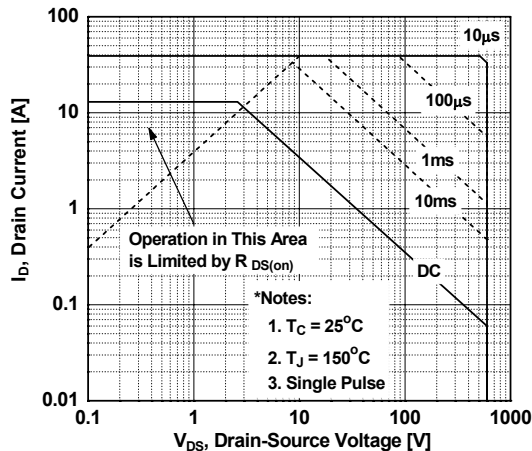


Figure 11. Maximum Drain Current vs. Case Temperature

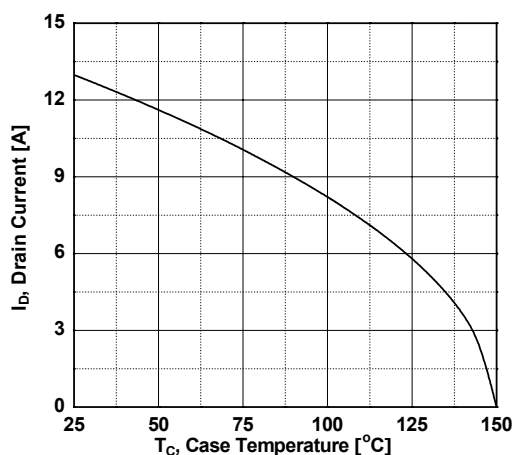


Figure 12. Transient Thermal Response Curve _ FCP13N60N

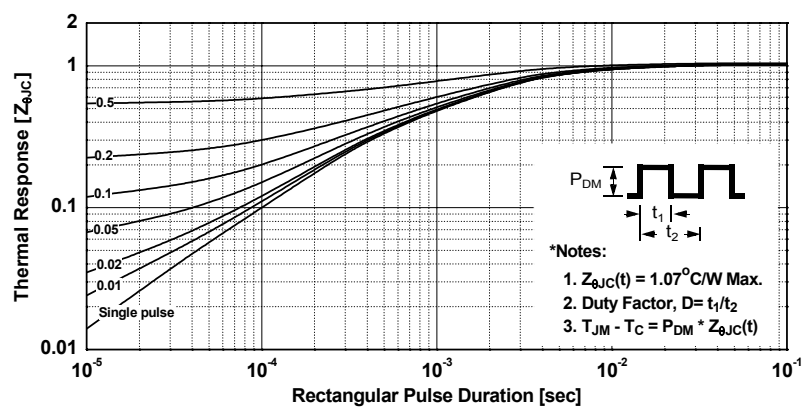
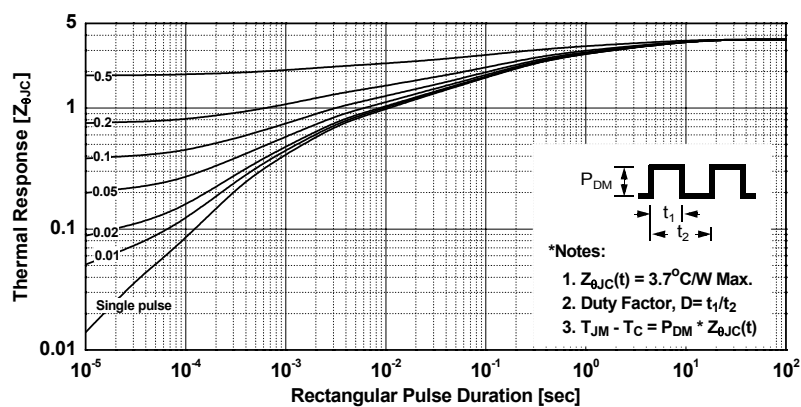
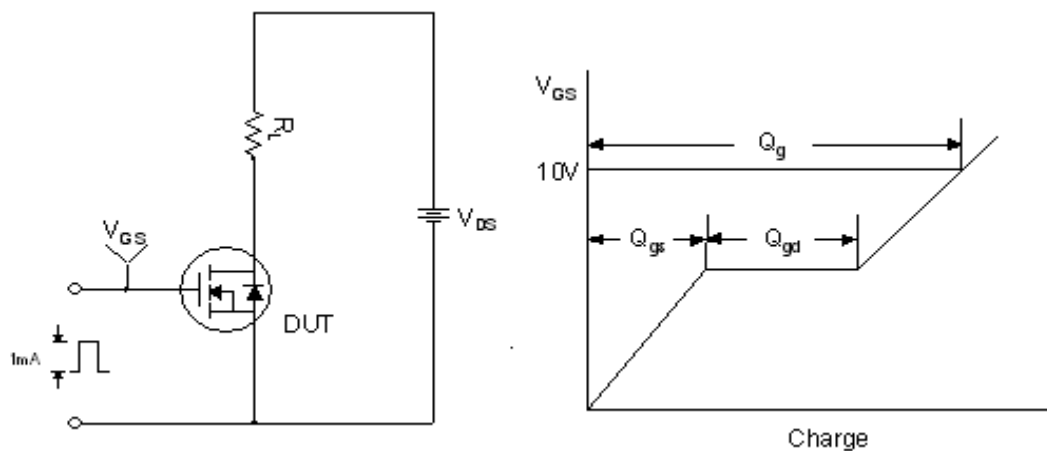


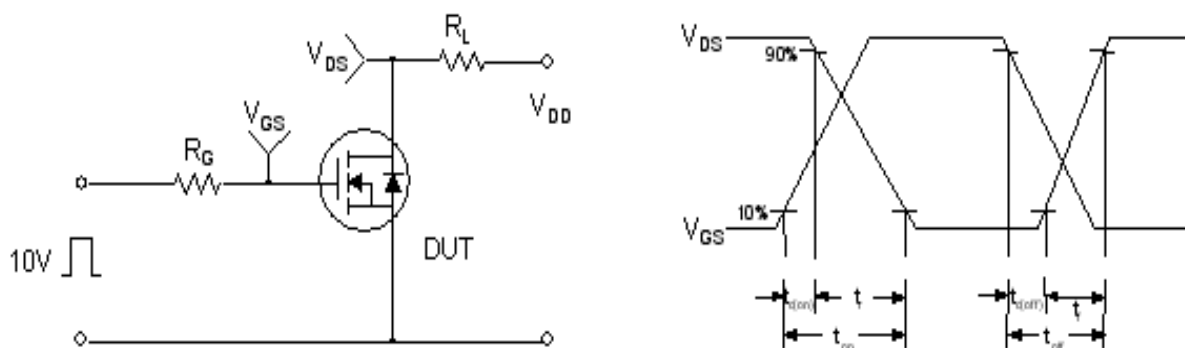
Figure 13. Transient Thermal Response Curve _ FCPF13N60NT



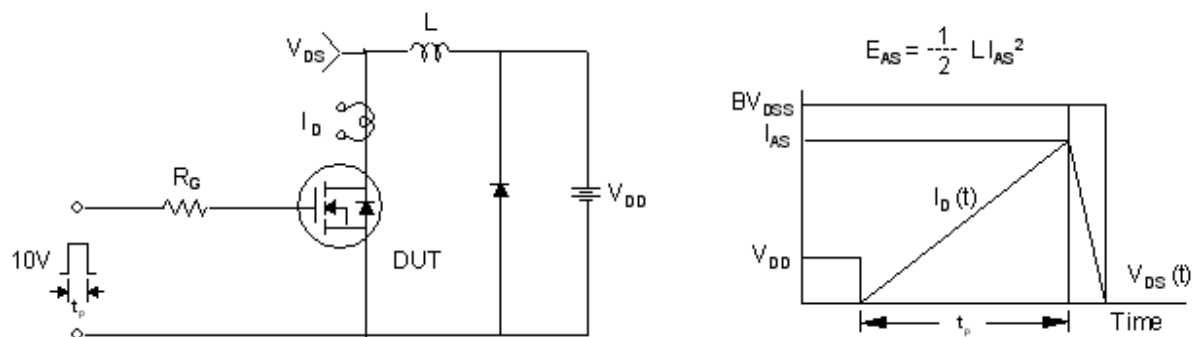
Gate Charge Test Circuit & Waveform



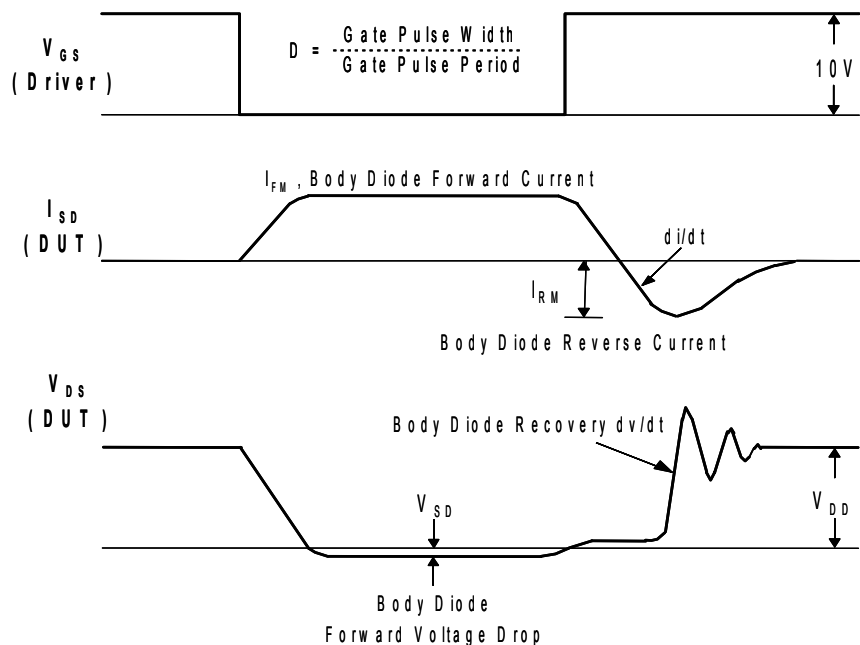
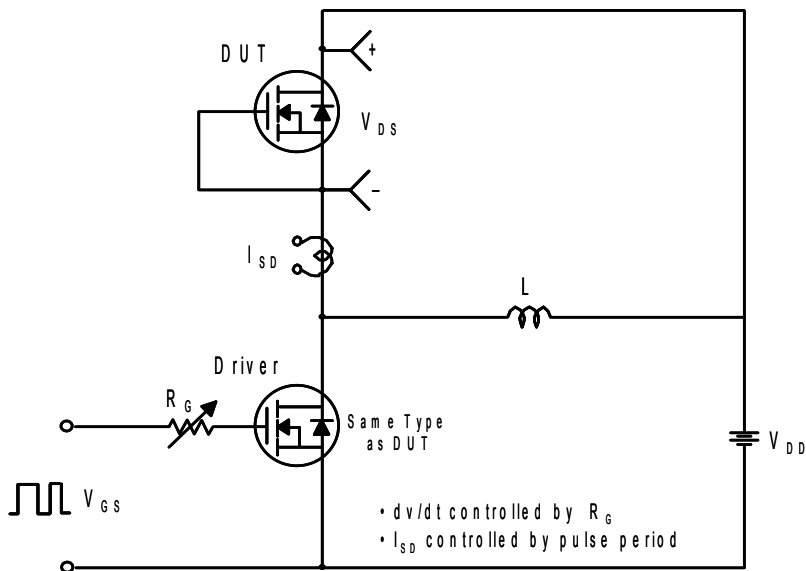
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



Technical drawing of a mechanical part showing three views: front, side, and top.

Front View Dimensions:

- Overall width: 10.67 (9.65)
- Overall height: 9.40 (8.38)
- Top hole diameter: $\varnothing 4.09$ (3.50)
- Top hole position: 3.43 (2.54) from top edge
- Bottom hole position: 16.51 (14.22) from bottom edge
- Pin 1 position: 1.78 (1.14) from left edge
- Pin 2 position: 1.02 (0.38) from left edge
- Pin 3 position: 5.08 from left edge
- Pin 1 length: 6.35 MAX
- Pin 2 length: 14.73 (12.70)
- Pin 3 length: 2.54

Side View Dimensions:

- Overall width: 4.83 (3.56)
- Overall height: 1.40 (0.51)
- Pin 1 position: 6.86 (5.84) from top edge
- Pin 2 position: 0.61 (0.33) from left edge
- Pin 3 position: 2.92 (2.03) from left edge

Top View Dimensions:

- Overall width: 8.89 (6.86)
- Overall height: 13.40 (12.19)
- Pin 1 position: 3.43 (2.54) from top edge
- Pin 2 position: 1.78 (1.14) from top edge
- Pin 3 position: 1.02 (0.38) from top edge
- Pin 1 length: 6.35 MAX
- Pin 2 length: 14.73 (12.70)
- Pin 3 length: 2.54

Notes:

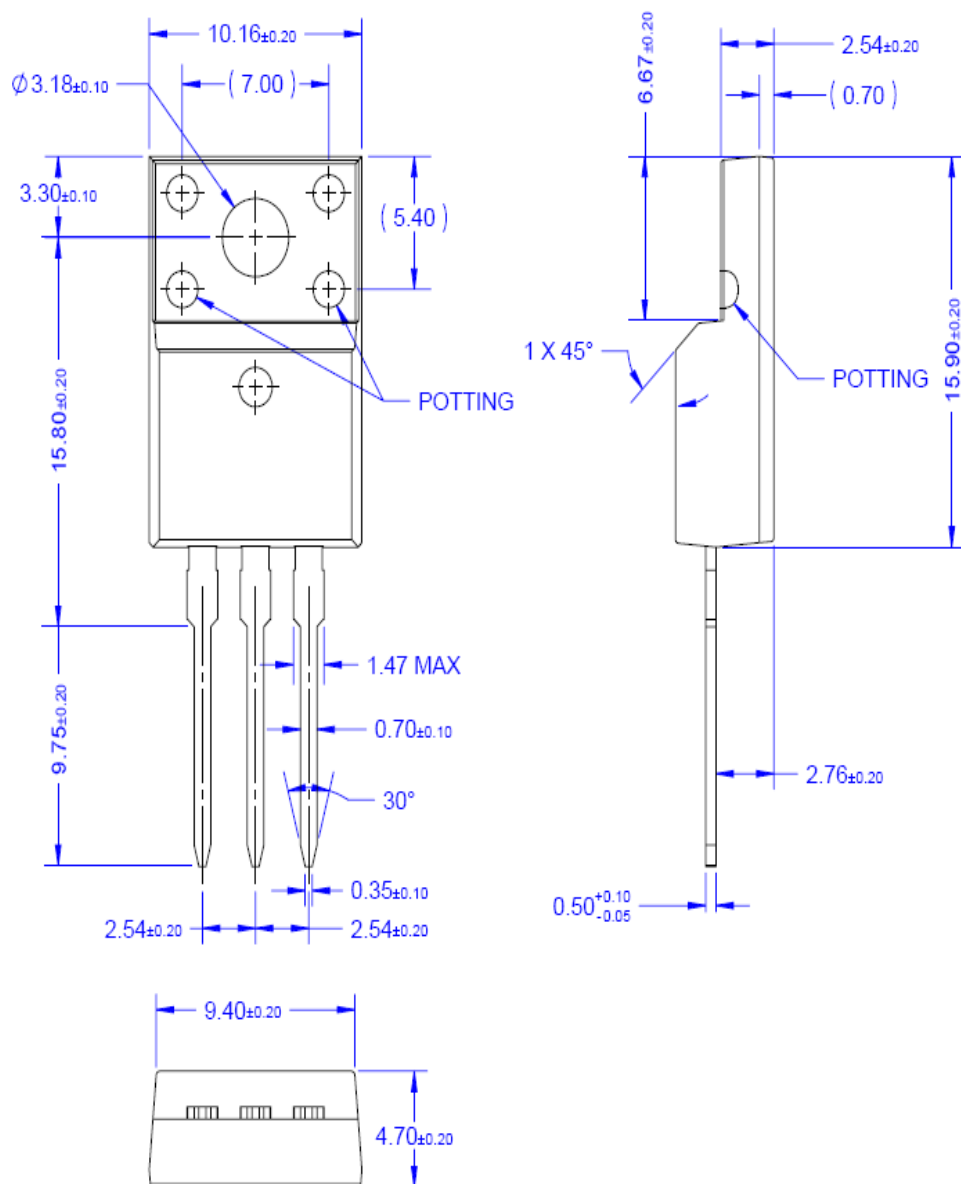
- Surface texture symbol: $\sqrt{0.36}$ (M) B A (M)
- Angle: 5°

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Mechanical Dimensions

TO-220F



Dimensions in Millimeters

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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