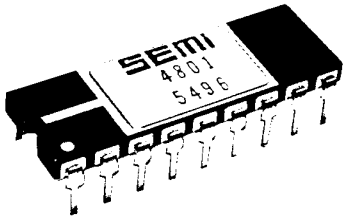
SEMI 4801 450NSEC, STATIC, TTL IN/OUT 4096x1 N-MOS RAM

FEATURES

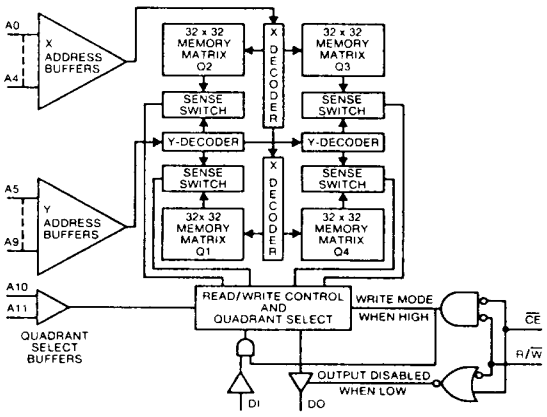
- Single +5V Power Supply
- 4Kx1 Organization
- Replaces 4 1024x1 Static RAMs
- Completely Static—No Clocks or Refresh
- 18 Pin Package
- Access/Cycle Times As Low As 400 nsec max
- 250 mw Typical Operating Power
- Separate Data In and Data Out
- TTL Compatible I/O
- Three State Outputs
- Data Bus Compatible I/O Function

GENERAL DESCRIPTION

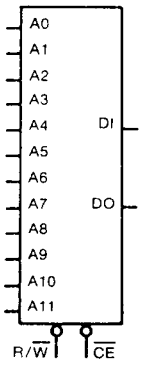


Part Number 4801 is a 4K semiconductor random access memory organized as 4096 1-bit words. It is fully static and needs no clock or refresh pulses. It requires a single +5 volt power supply and is fully TTL compatible on input and output lines. The 4801 is packaged in a convenient 18 pin dual-in-line package.

BLOCK DIAGRAM



LOGIC SYMBOL

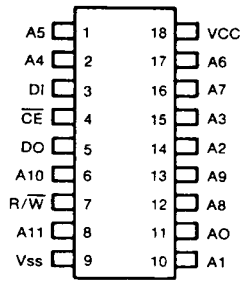


TRUTH TABLE

$\overline{CE}$	R/$\overline{W}$	DI	DO	STATUS	MODE
H	Don't Care	Don't Care	High Z	Deselect	Standby
L	H	Don't Care	Data	Selected	READ
L	L	L	High Z	Selected	Write 0
L	L	H	High Z	Selected	Write 1

PIN CONFIGURATION

AN	Address Inputs
DI	Data Input
DO	Data Output
$\overline{CE}$	Chip Enable
R/$\overline{W}$	Read/Write
Vss	Ground
Vcc	+5V Power Supply



RECOMMENDED OPERATING CONDITIONS AMB = 0°C to +70°C

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Level	V_{IH}	2.4		V_{CC}	Vdc
Input Low Level	V_{IL}	−0.5		0.8	Vdc

DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage & Temperature Range Unless Otherwise Noted)

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Leakage Current	I_{LI}	−10		+10	μA	V_{IN} = 0.5V or +5V
Output Leakage Current	I_{LO}	−10		+10	μA	V_{OUT} = 2.4V
Output Voltage High	V_{OH}	2.4		V_{CC}	Vdc	I_{OH} = −200μa
Output Voltage Low	V_{OL}			0.4	Vdc	I_{OL} = 2.0ma
Power Supply Current	I_{CC}		45	75	ma	V_{CC} = 5V; 25°C
	I_{CC}		65	100	ma	V_{CC} = 5V; 70°C

READ CYCLE—AC CHARACTERISTICS

PARAMETER	SYMBOL	4801 MIN	4801 MAX	4801A MIN	4801A MAX	4801B MIN	4801B MAX	CONDITIONS
Read Cycle Time	T_{RC}	600		450		400		Full Operating Voltage and Temperature Range
Access Time	T_A		600		450		400	
Chip Enable to Output Enable	T_{CO}		200		150		140	
Data Valid After Address	T_{OH1}	150		100		85		
Previous Data Valid After Chip De-Select	T_{OH2}	25		25		25		

WRITE CYCLE—AC CHARACTERISTICS

PARAMETER	SYMBOL	4801 MIN	4801 MAX	4801A MIN	4801A MAX	4801B MIN	4801B MAX	CONDITIONS
Write Cycle Time	T_{WC}	600		450		400		Full Operating Voltage and Temperature Range
Address To Write Time	T_{AW}	100		75		65		
Write Pulse Switch	T_{WP}	500		375		330		
Write Recovery Time	T_{WR}	0		0		0		
Data Set Up Time	T_{DW}	350		250		225		
Data Hold Time	T_{DH}	0		0		0		
Output Disable From Write or Chip Enable	T_{OTW}		150		125		110	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Capacitance	C			5	pF	V_{IN} = 2.4V
Output Capacitance	C			10	pF	

ABSOLUTE MAXIMUM RATINGS

(See Note 1) (Referenced to Gnd)

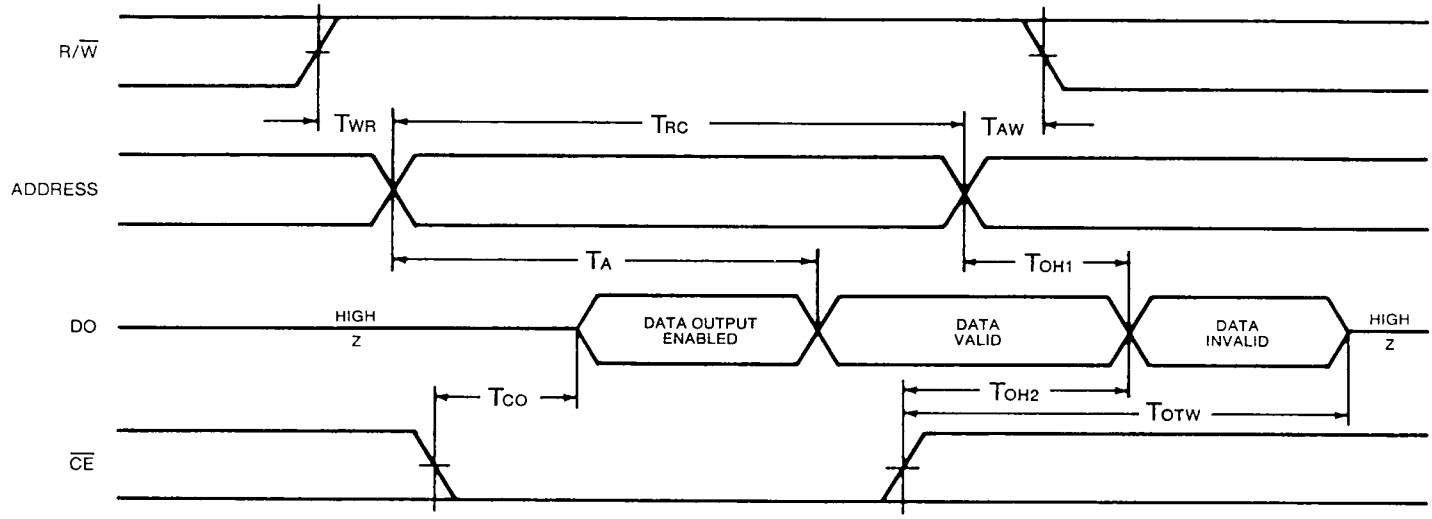
RATING	VALUE	UNIT
Voltage On Any Pin With Respect To GND	−0.5 to +7	VDC
Power Dissipation	1.6 (Note 2)	W
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

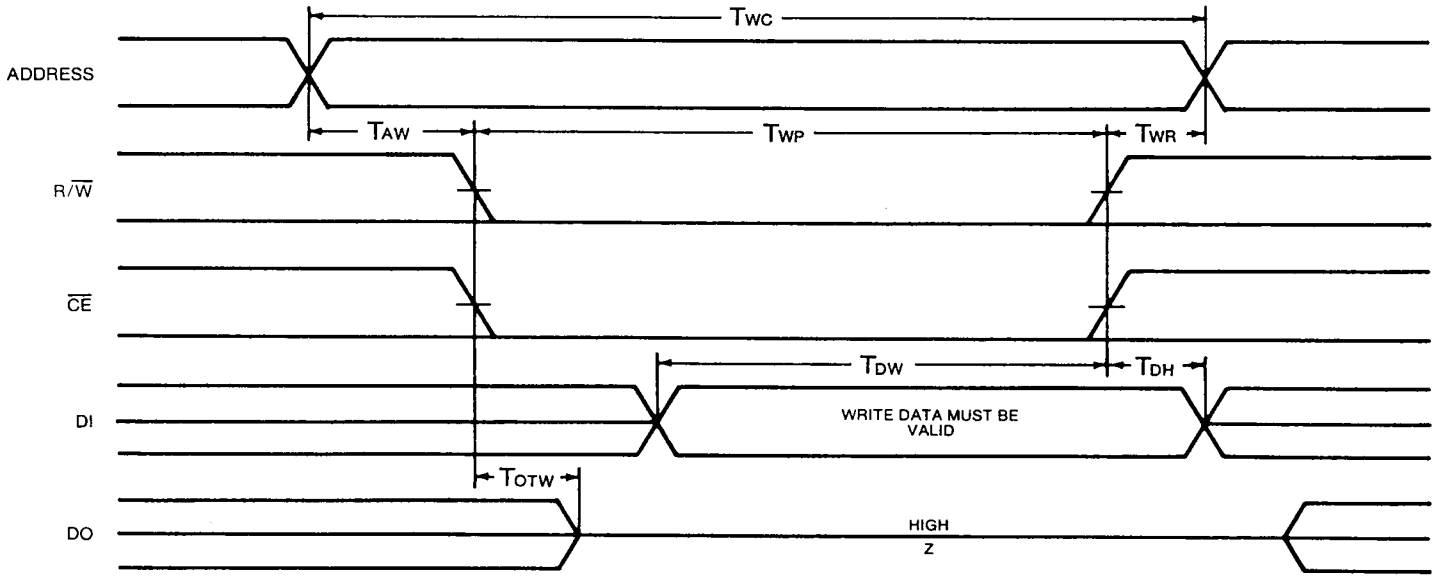
NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25 C Ambient. Derate 13.5 mw/ C.

READ CYCLE TIMING



WRITE CYCLE TIMING



FUNCTIONAL DESCRIPTION

EMM SEMI 4801 is a 4096 bit static RAM organized as 4096 words x 1 bit. After addressing the proper word on pins A_0 through A_{11}, data is read or written on separate data input/output pins (DI and DO) under the control of Read/Write (R/$\overline{W}$) or Chip Enable ($\overline{CE}$).

Data access is particularly simple since address setup time is not required. The chip is in a read mode whenever R/$\overline{W}$ is high. If $\overline{CE}$ is held low, the array may be read by toggling addresses. Valid output data will be available within time T_A of stable address. If $\overline{CE}$ is used to control the read mode, data access time must always be equal to or greater than T_A, but can not occur earlier than T_{CO} from $\overline{CE}$ going low.

The write mode occurs when both $\overline{CE}$ and R/$\overline{W}$ are low. Data storage, therefore, is unaffected by change in state on pins A_N, DI, DO, $\overline{CE}$ or R/$\overline{W}$ as long as either $\overline{CE}$ or R/$\overline{W}$ are high. To write, addresses must be stable for time T_{AW} before writing plus T_{WP} while writing.

There are three possible modes of writing.

1. $\overline{CE}$ is held low. T_{AW} and T_{WP} are then defined by R/$\overline{W}$ going from a high state to a low state and T_{WR} is defined by R/$\overline{W}$ going from a low state to a high state.
2. R/$\overline{W}$ is held low. $\overline{CE}$ going low is then used to define T_{AW} and T_{WP}. $\overline{CE}$ going high is used to define T_{WR}.
3. $\overline{CE}$ and R/$\overline{W}$ are both used. Timing at the beginning of the cycle is then defined by the latter of $\overline{CE}$ or R/$\overline{W}$ going low and timing at the end of the cycle is determined by the earlier of $\overline{CE}$ or R/$\overline{W}$ going high.

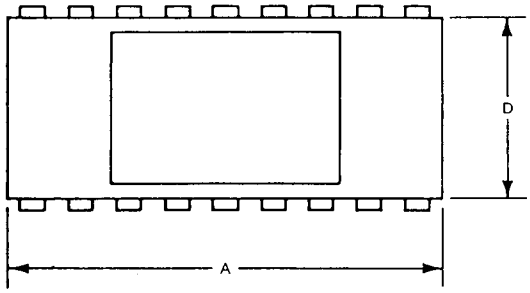
The addresses must remain stable for the entire Write cycle, but data inputs are not required to remain stable. The correct logic level will be entered as long as the input data is stable for time T_{DW} during the write cycle.

Since Data Out is high impedance during a Write cycle, Data In and Data Out may be wire-ored for applications requiring a common data bus.

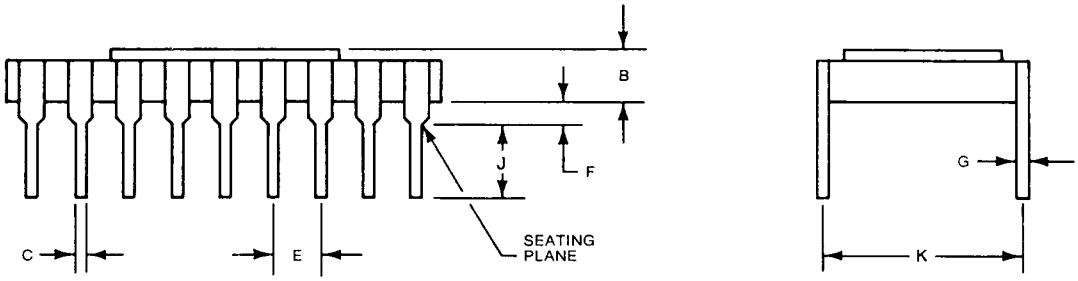
NOTES

1. T_{AW} is measured from the latter of $\overline{CE}$ or R/$\overline{W}$ going low.
2. T_{WP} is measured from the latter of $\overline{CE}$ or R/$\overline{W}$ going low to the earlier of $\overline{CE}$ or R/$\overline{W}$ going high.
3. T_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high.
4. T_{DH} and T_{DW} are measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high.
5. T_{OTW} is measured from R/$\overline{W}$ going low or $\overline{CE}$ going high, whichever occurs first.
6. Timing diagrams are based on loading to simulate the capacitive effect of five additional outputs plus the current loading effect of one TTL input.
7. Input pulse levels 0.8 volts logic low to 2.4 volts logic high.
8. Input rise and fall times 10 nsec.
9. Timings measured from 1.5 volt level whether pulse is going high or low.
10. Output is high impedance during a write mode or when $\overline{CE}$ is high. Input always represents a high impedance.

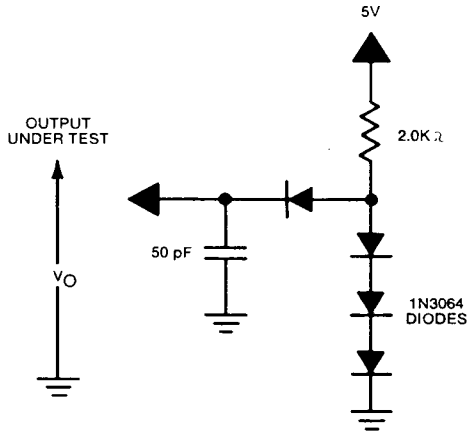
PACKAGING DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.6	23.1	0.890	0.910
B	—	3.18	—	0.125
C	0.38	0.53	0.015	0.021
D	7.06	7.57	0.278	0.298
E	2.29	2.79	0.090	0.110
F	0.64	1.65	0.025	0.065
G	0.20	0.31	0.008	0.012
J	2.54	3.81	0.100	0.150
K	7.62 Ref		0.300 Ref.	



TEST OUTPUT LOAD



• Capacitive loading to simulate effect of five additional outputs plus one TTL input

5

ORDERING INFORMATION

Part Number	Speed	Package	Temperature Range
4801 UCC	600 nsec	Ceramic	0°C to +70°C
4801 ACC	450 nsec	Ceramic	0°C to +70°C
4801 BCC	400 nsec	Ceramic	0°C to +70°C

EMM/SEMI reserves the right to make changes at any time in order to improve design and to supply the best product possible.

WARNING:

MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or in conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

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