

54F/74F109

Dual JK Positive Edge-Triggered Flip-Flop

General Description

The 'F109 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and K inputs.

Asynchronous Inputs:

LOW input to $\bar{S}_D$ sets Q to HIGH level
 LOW input to $\bar{C}_D$ sets Q to LOW level
 Clear and Set are independent of clock
 Simultaneous LOW on $\bar{C}_D$ and $\bar{S}_D$ makes both Q and $\bar{Q}$ HIGH

Features

- Guaranteed 4000V minimum ESD protection.

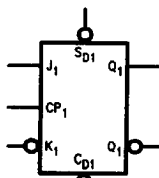
Ordering Code: See Section 11

Commercial	Military	Package Number	Package Description
74F109PC		N16E	16-Lead (0.300" Wide) Molded Dual-in-Line
	54F109DM (Note 2)	J16A	16-Lead Ceramic Dual-in-Line
74F109SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F109SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F109FM (Note 2)	W16A	16-Lead Cerpack
	54F109LM (Note 2)	E20A	16-Lead Ceramic Leadless Chip Carrier, Type C

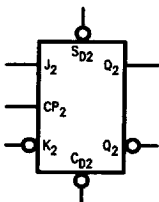
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

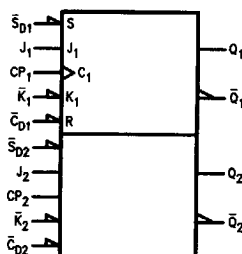


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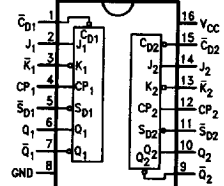
IEEE/IEC



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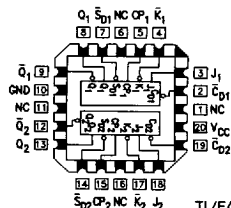
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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Pin Assignment for LCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

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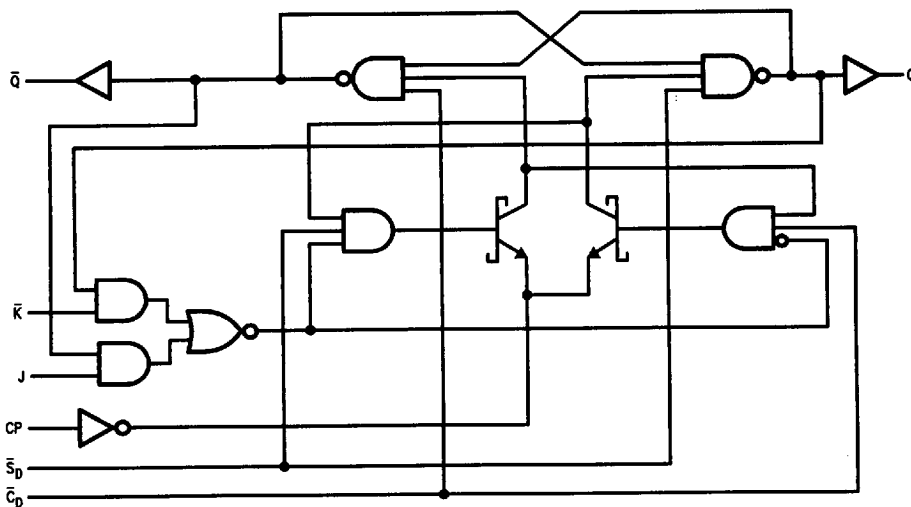
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$J_1, J_2, \bar{K}_1, \bar{K}_2$	Data Inputs	1.0/1.0	20 μA / -0.6 mA
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 μA / -0.6 mA
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs (Active LOW)	1.0/3.0	20 μA / -1.8 mA
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/3.0	20 μA / -1.8 mA
$Q_1, Q_2, \bar{Q}_1, \bar{Q}_2$	Outputs	50/33.3	-1 mA/20 mA

Truth Table

Inputs					Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	—	l	l	L	H
H	H	—	h	l	Toggle	
H	H	—	l	h		
H	H	—	h	h	Q_0	$\bar{Q}_0$
H	H	L	X	X	Q_0	$\bar{Q}_0$

H (h) = HIGH Voltage Level
 L (l) = LOW Voltage Level
 — = LOW-to-HIGH Transition
 X = Immaterial

Q_0 ($\bar{Q}_0$) = Before LOW-to-HIGH Transition of Clock
 Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram (One Half Shown)


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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C

V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V

Input Voltage (Note 2) -0.5V to +7.0V

Input Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V_{CC} = 0V)
Standard Output -0.5V to V_{CC}
TRI-STATE® Output -0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature

Military -55°C to +125°C
Commercial 0°C to +70°C

Supply Voltage

Military +4.5V to +5.5V
Commercial +4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.5 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -1.8	mA	Max Max	V _{IN} = 0.5V (J _N , R _N) V _{IN} = 0.5V (C _{DN} , S _{DN})
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		11.7	17.0	mA	Max	CP = 0V



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AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

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查询"54F109FMQB"供应商		74F			54F		74F		Units	Fig. No.
Symbol	Parameter	$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125		70		90		MHz	2-1
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\bar{Q}_n$	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	9.0 10.5	3.8 4.4	8.0 9.2	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q_n or $\bar{Q}_n$	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	9.0 11.5	3.2 3.5	8.0 10.5	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW J_n or $\bar{K}_n$ to CP_n	3.0 3.0		3.0 4.0		3.0 3.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW J_n or $\bar{K}_n$ to CP_n	1.0 1.0		1.0 1.0		1.0 1.0			
$t_w(\text{H})$ $t_w(\text{L})$	CP_n Pulse Width HIGH or LOW	4.0 5.0		4.0 5.0		4.0 5.0		ns	2-4
$t_w(\text{L})$	$\bar{\text{C}}_{\text{Dn}}$ or $\bar{\text{S}}_{\text{Dn}}$ Pulse Width, LOW	4.0		4.0		4.0		ns	2-4
t_{rec}	Recovery Time $\bar{\text{C}}_{\text{Dn}}$ or $\bar{\text{S}}_{\text{Dn}}$ to CP	2.0		2.0		2.0		ns	2-6