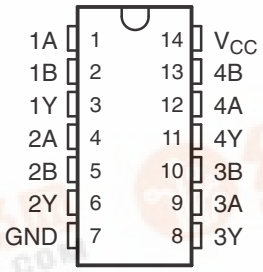
# RAD-TOLERANT CLASS V, QUADRUPLE 2-INPUT POSITIVE-NAND GATE

## FEATURES

- **2-V to 6-V $V_{CC}$ Operation**
- **Inputs Accept Voltages to 6 V**
- **Max $t_{pd}$ of 7 ns at 5 V**
- **Rad-Tolerant: 50 KRad(Si) TID** (1)
  - **TID Dose Rate < 2 mRad/sec**
- **QML-V Qualified, SMD 5962-87549**

(1) Radiation tolerance is a typical value based upon initial device qualification. Radiation Lot Acceptance Testing is available - contact factory for details.

**J OR W PACKAGE**
**(TOP VIEW)**




## DESCRIPTION/ORDERING INFORMATION

The SN54AC00 device contains four independent 2-input NAND gates. Each gate performs the Boolean function of $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

### ORDERING INFORMATION

| $T_A$ | PACKAGE(1)(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55°C to 125°C | CDIP – J | Tube | 5962-8754903VCA | 5962-8754903VCA |
| | CFP – W | Tube | 5962-8754903VDA | 5962-8754903VDA |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

### FUNCTION TABLE
### (Each Gate)

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

### LOGIC DIAGRAM (POSITIVE LOGIC)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## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 or $V_I$ > $V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±200 | mA |
| $\theta_{JA}$ | Package thermal impedance(3) | J package | | | °C/W |
| | | W package | | | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 2.1 | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | | 0.9 | V |
| | | $V_{CC}$ = 4.5 V | | 1.35 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3 V | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | 24 | |
| | | $V_{CC}$ = 5.5 V | | 24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3 V | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | 24 | |
| | | $V_{CC}$ = 5.5 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | | 8 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 3 V | 2.9 | | | 2.9 | | V |
| | | 4.5 V | 4.4 | | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | |
| | $I_{OH}$ = –12 mA | 3 V | 2.56 | | | 2.4 | | |
| | $I_{OH}$ = –24 mA | 4.5 V | 3.86 | | | 3.7 | | |
| | | 5.5 V | 4.86 | | | 4.7 | | |
| | $I_{OH}$ = –50 mA (1) | 5.5 V | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 3 V | | | 0.1 | | 0.1 | V |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | | 5.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 12 mA | 3 V | | | 0.36 | | 0.5 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | |
| | | 5.5 V | | | 0.36 | | 0.5 | |
| | $I_{OL}$ = 50 mA (1) | 5.5 V | | | | | 1.65 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.6 | | | | pF |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | 2 | 7 | 9.5 | 1 | 11 | ns |
| $t_{PHL}$ | | | 1.5 | 5.5 | 8 | 1 | 9 | |

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | 1.5 | 6 | 8 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | 1.5 | 4.5 | 6.5 | 1 | 7 | |

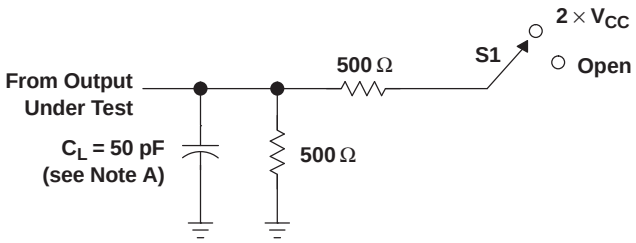
## OPERATING CHARACTERISTICS

$V_{CC}$ = 5 V, $T_A$ = 25°C

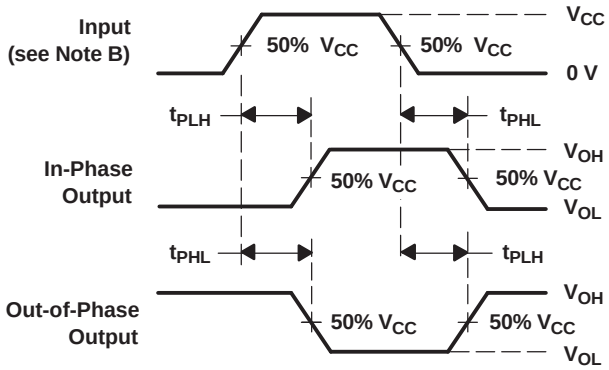
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 1 MHz | 40 | pF |

## PARAMETER MEASUREMENT INFORMATION

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |




LOAD CIRCUIT



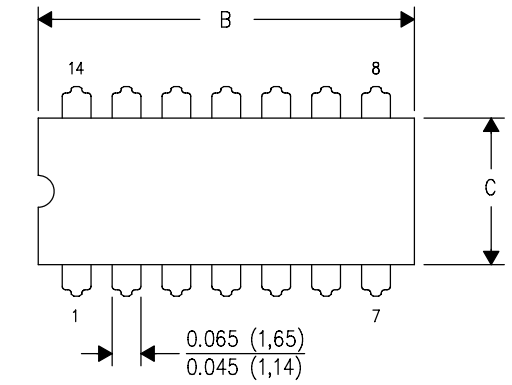

VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

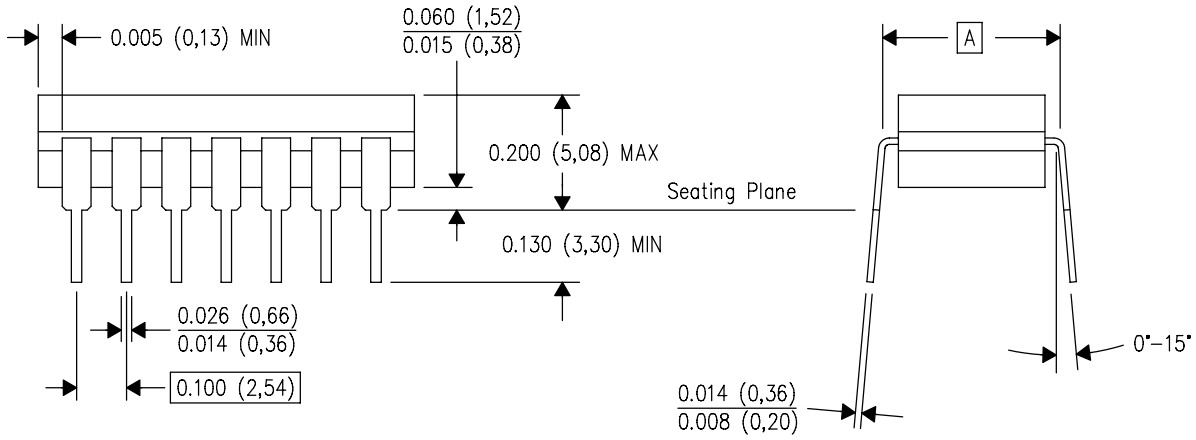
**Figure 1. Load Circuit and Voltage Waveforms**

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

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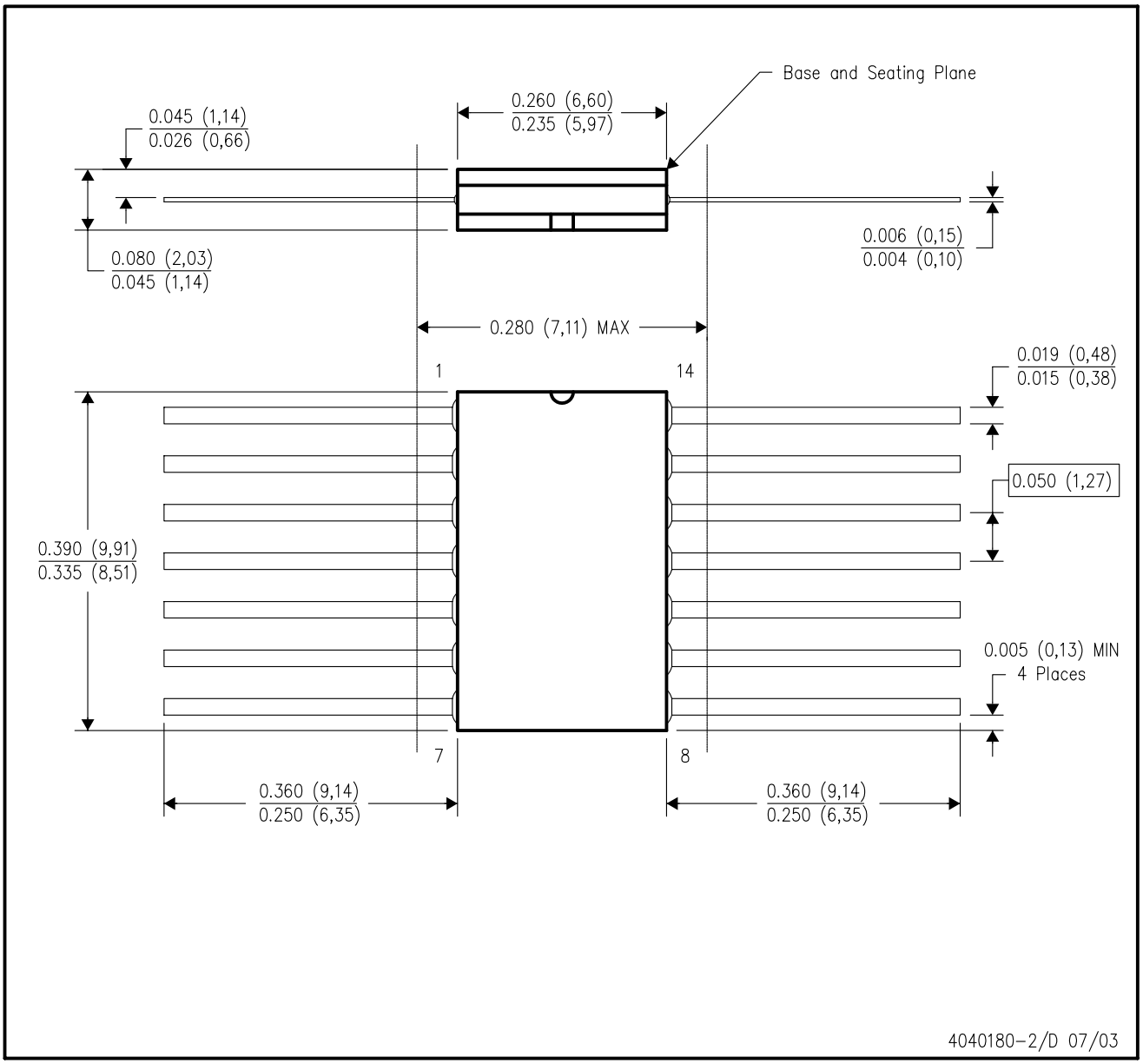
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

## W (R–GDFP–F14) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

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