REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added vendor CAGE number 6Y440 and 65786 to the drawing as approved sources of supply. Removed vendor CAGE number 0BK02 from the drawing. Also deleted ESDS from the drawing. Editorial changes throughout.	1989 SEP 28	M. A. Frye
B	Changes in accordance with NOR 5962-R349-92.	1992 OCT 29	M. A. Frye
C	Added device types 05 and 06. Updated drawing to include new verbage from standard boilerplate. Figure 1 Terminal connections, for case outline Y, changed DQ to I/O, $\overline{W}$ to $\overline{WE}$, and $\overline{C}$ to $\overline{CE}$. Removed CAGE numbers 61772, 6Y440, and 66301. Added CAGE numbers 0EU86. ksr	1997 AUG 19	RAYMOND MONNIN

REV																				
SHEET																				
REV	C																			
SHEET	15																			

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
27 JULY 1988

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 64K X 4 SRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88681**

SHEET 1 OF 15

DESC FORM 2233
APR 97

5962-E243-97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0030257 T58

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88681	01	L	X
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
Drawing number	Device type (see 1.2.1)	Case outline (see 1:2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(See 6.6)	64K X 4 CMOS SRAM	35 ns
02	(See 6.6)	64K X 4 CMOS SRAM	45 ns
03	(See 6.6)	64K X 4 CMOS SRAM	55 ns
04	(See 6.6)	64K X 4 CMOS SRAM	70 ns
05	(See 6.6)	64K X 4 CMOS SRAM	25 ns
06	(See 6.6)	64K X 4 CMOS SRAM	20 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package
X	CQCC3-N28	28	rectangular chip carrier package
Y	CDFP4-28	28	flat package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage on any input relative to V_{SS} range	-0.5 V dc to +7.0 V dc
Voltage applied to outputs range	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases L and X	See MIL-STD-1835
Junction temperature (T_J)	+150°C 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage range (V_{SS})	0 V dc
Input high voltage range (V_{IH})	2.2 V dc to V_{CC} +0.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to + 0.8 V dc 2/
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
2/ V_{IL} minimum = -3.0 V dc for pulse width less than 20 ns.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}/ C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 15 devices with no failures and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Operating supply current 1/	I_{CC1}	$t_{AVAV} = t_{AVAV}$ (minimum), V_{CC} = 5.5 V, $\overline{CE} = V_{IL}$	1, 2, 3	01 - 04		120	mA
				05		140	
				06		150	
Standby power supply current TTL 1/	I_{CC2}	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = 5.5 V, f = 0 MHz		01 - 04		25	
				05		40	
				06		45	
Standby power supply current CMOS 1/	I_{CC3}	$\overline{CE} \ge (V_{CC} - 0.2\ V)$, f = 0 Mhz, V_{CC} = 5.5 V, all other inputs ≤ 0.2 V or $> (V_{CC} - 0.2\ V)$		All		20	
Input leakage current any input	I_{ILK}	V_{CC} = 5.5 V, V_{IN} = 0 V to 5.5 V				±10	µA
Off state output leakage current	I_{OLK}	V_{CC} = 5.5 V, V_{IN} = 0 V to 5.5 V				±10	
Output high voltage	V_{OH}	I_{OUT} = -4.0 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.2 V			2.4		V
Output low voltage	V_{OL}	I_{OUT} = 8.0 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.2 V				0.4	
Input capacitance	C_{IN}	VIN = 0V,				10.0	pF
Output capacitance	C_{OUT}	f = 1.0 Mhz, TA = +25°C, See 4.3.1c	4			12.0	
Functional Testing		See 4.3.1d	7, 8A, 8B				

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Chip enable access time	t_{ELQV}	See figure 4	9, 10, 11	01		35	ns
				02		45	
				03		55	
				04		70	
				05		25	
				06		20	
Read cycle time	t_{AVAV}	See figure 4 3/		01	35		
				02	45		
				03	55		
				04	70		
				05	25		
				06	20		
Address access time	t_{AVQV}	See figure 4 4/		01		35	
				02		45	
				03		55	
				04		70	
				05		25	
				06		20	
Output hold after address change	t_{AVQX}	See figure 4		All	3.0		
Chip enable to output active	t_{ELQX}	See figure 4 5/ 6/		All	3.0		
Chip disable to output inactive	t_{EHQZ}			01, 02	0	20	
				03	0	25	
				04	0	30	
				05, 06	0	10	
Chip enable to power up	t_{ELPU}	See figure 4 5/		All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Chip enable to power down	t_{EHPD}	See figure 4 5/	9, 10, 11	01		35	ns
				02		45	
				03		55	
				04		70	
				05		25	
				06		20	
Input rise and fall times	t_T	5/ 7/		All		50	
Write cycle time	t_{AVAV}	See figure 5		01	35		
				02	45		
				03	55		
				04	70		
				05	25		
				06	20		
Write pulse width	t_{WLWH}			01	30		
				02	40		
				03	50		
				04	55		
				05	17		
				06	15		
Chip enable to end of write	t_{ELEH}			01	30		
				02	40		
				03	50		
				04	55		
				05	18		
				06	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Data setup to end of write	t_{DVWH}	See figure 5	9, 10, 11	01, 02	20		ns
				03, 04	25		
				05	12		
				06	10		
Data hold after end of write	t_{WHDX}			All	0		
Address setup to end of write	t_{AVWH}			01	30		
				02	40		
				03	50		
				04	55		
				05	18		
				06	15		
Address setup to beginning of write	t_{AVWL}	See figure 5 (write cycle number 1)		All	0		
	t_{AVEL}	See figure 5 (write cycle number 2)			0		
Address hold after end of write	t_{WHAV}	See figure 5		01 - 04	5.0		
				05, 06	2.0		
Write enable to output disable	t_{WLQZ}	See figure 5 5/ 6/		01, 02	0	20	
				03	0	25	
				04	0	30	
				05	0	11	
				06	0	10	
Output active after end of write	t_{WHQX}	See figure 5 5/ 6/ 8/		All	0		

1/ I_{CC} is dependent upon output loading and cycle rate. The specified values apply with output(s) unloaded.
2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance. Output timing reference is 1.5 V. See figure 3.
3/ For read cycles 1 and 2, $\overline{WE}$ is high for entire cycle.
4/ Device is continuously selected, $\overline{CE}$ low.
5/ Parameter if not tested, shall be guaranteed to the limits specified in table I.
6/ Measured ±500 mV from steady-state output voltage. Load capacitance is 5.0 pF.
7/ Measured between V_{IL} maximum and V_{IH} minimum.
8/ If $\overline{WE}$ is low when $\overline{CE}$ goes low, the output remains in the high impedance state.

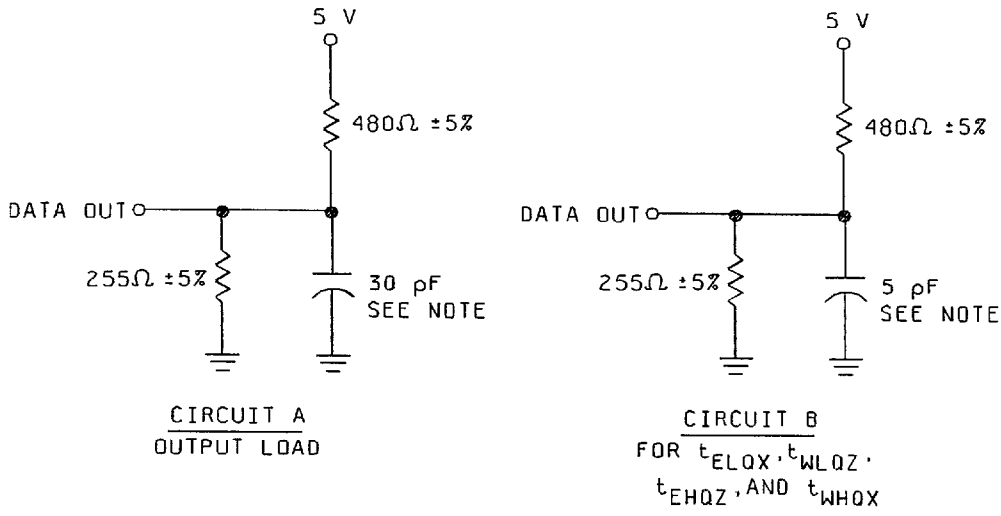
Device types	01, 02, 03, 04, 05, 06		
Case outlines	L	X	Y
Terminal number	Terminal symbol		
1	A_6	NC	NC
2	A_7	A_6	A_0
3	A_8	A_7	A_1
4	A_9	A_8	A_2
5	A_{10}	A_9	A_3
6	A_{11}	A_{10}	A_4
7	A_{12}	A_{11}	A_5
8	A_{13}	A_{12}	A_6
9	A_{14}	A_{13}	A_7
10	A_{15}	A_{14}	A_8
11	$\overline{CE}$	A_{15}	A_9
12	V_{SS}	$\overline{CE}$	$\overline{CE}$
13	$\overline{WE}$	NC	NC
14	I/O_4	V_{SS}	V_{SS}
15	I/O_3	NC	$\overline{WE}$
16	I/O_2	$\overline{WE}$	I/O_0
17	I/O_1	I/O_4	I/O_1
18	A_0	I/O_3	I/O_2
19	A_1	I/O_2	I/O_3
20	A_2	I/O_1	NC
21	A_3	A_0	NC
22	A_4	A_1	A_{10}
23	A_5	A_2	A_{11}
24	V_{CC}	A_3	A_{12}
25	---	A_4	A_{13}
26	---	A_5	A_{14}
27	---	NC	A_{15}
28	---	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

$\overline{CE}$	$\overline{WE}$	Mode	I/O	Power
X	X	Not selected	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

H = Logic "1" state
L = Logic "0" state
X = Don't care

FIGURE 2. Truth table.

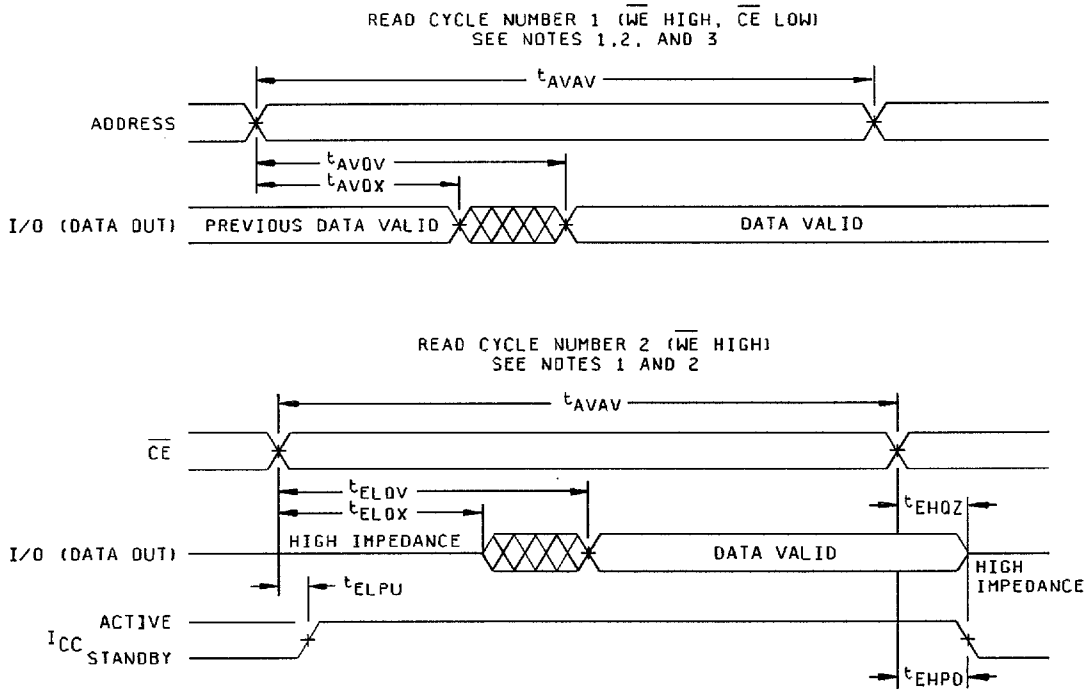


NOTE: Including scope and jig (minimum values).

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuits.



Notes:
1. $\overline{WE}$ is high for entire cycle.
2. $\overline{CE}$ and $\overline{WE}$ must meet transition between VIH (min) to VIL (max) or VIL (max) to VIH (min) in a monotonic fashion.
3. Device is continuosly selected, $\overline{CE}$ low.

FIGURE 4. Read cycle timing diagrams.

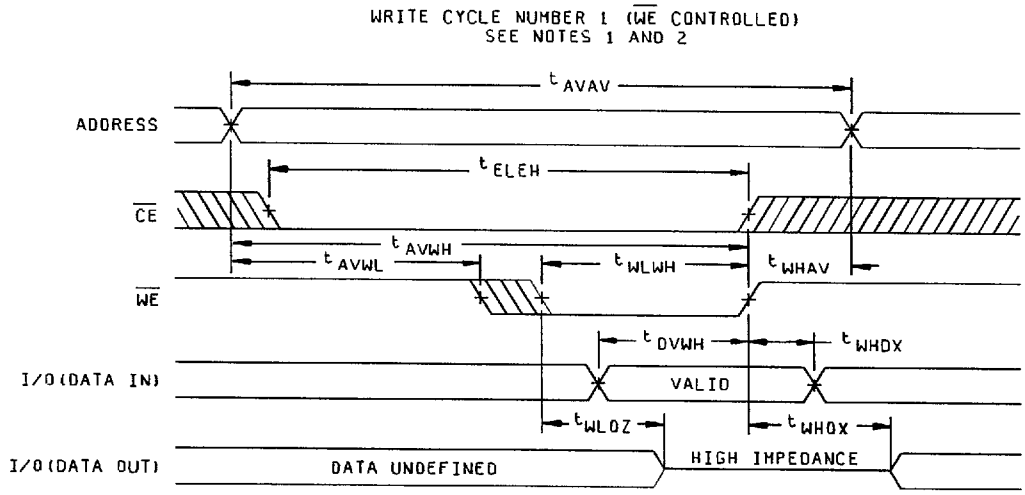
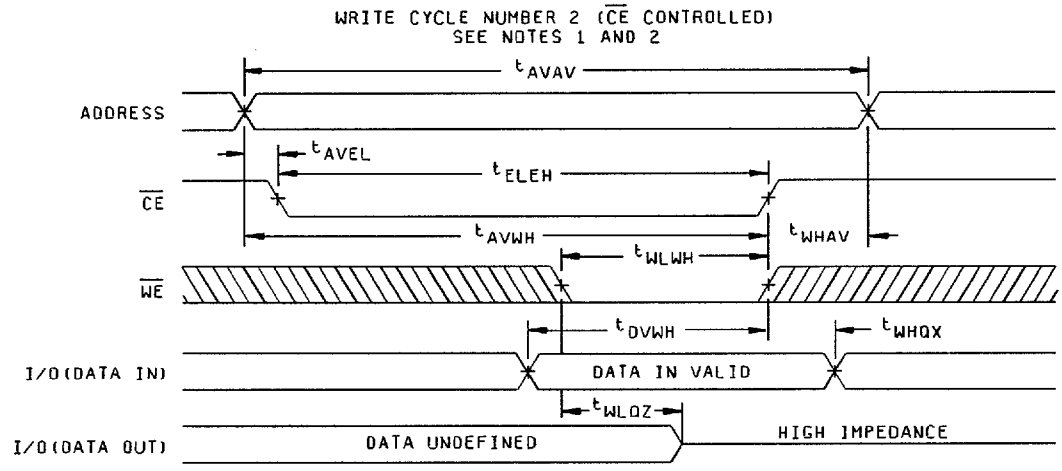


FIGURE 5. Write cycle timing diagrams.



Notes:
1. $\overline{CE}$ and $\overline{WE}$ must meet transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
2. $\overline{CE}$ and $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

FIGURE 5. Write cycle timing diagrams - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroup 1 and 7.
** See 4.3.1c

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 1997 AUG 19

Approved sources of supply for SMD 5962-97524 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 as applicable during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8868101LA	65786 0EU86 0HGZ7 65896 3/ 3/	CY7C194-35DMB MT5C2564C-35883C HM1-65798K/883 L7C194CMB35 IDT71258S35CB EDI8465C35QB
5962-8868101XA	3/ 0EU86 65896 3/	CY7C194-35LMB MT5C2564EC-35883C L7C194KMB35 EDI8465C35LB
5962-8868101YA	3/	EDI8465C35B
5962-8868102LA	65786 0EU86 0HGZ7 65896 3/ 3/	CY7C194-45DMB MT5C2564C-45883C HM1-65798M/883 L7C194CMB35 IDT71258S45CB EDI8465C45QB
5962-8868102XA	3/ 0EU86 65896 3/	CY7C194-45LMB MT5C2564EC-45883C L7C194KMB35 EDI8465C35LB
5962-8868102YA	3/	EDI8465C45B
5962-8868103LA	0EU86 0HGZ7 65896 3/ 3/	MT5C2564C-55883C HM1-65798N/883 L7C194CMB55 IDT71258S55CB EDI8465C55QB
5962-8868103XA	0EU86 65896 3/	MT5C2564EC-55883C L7C194KMB55 EDI8465C55LB
5962-8868103YA	3/	EDI8465C55B

See notes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8868104LA	0EU86 0HGZ7 65896 3/ 3/	MT5C2564C-70883C HM1-65798N/883 L7C194CMB55 IDT71258S70CB EDI8465C70QB
5962-8868104XA	0EU86 65896 3/	MT5C2564EC-70883C L7C194KMB55 EDI8465C70LB
5962-8868104YA	3/	EDI8465C70B
5962-8868105LA	0EU86	MT5C2564C-25883C
5962-8868105XA	0EU86	MT5C2564EC-25883C
5962-8868106LA	0EU86	MT5C2564C-20883C
5962-8868106XA	0EU86	MT5C2564EC-20883C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor Inc. 8701 Cross Park Dr. Austin, TX 78754
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134
65896	Logic Device Inc. 628 East Evelyn Ave. Sunnyvale, CA 94086-6489
0HGZ7	Matra-Harris Semiconductor 2895 Northwestern Pky. Santa Clara, CA 94086-6489

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