

5V ECL Triple 2:1 Multiplexer

Description

The MC100EL59 is a triple 2:1 multiplexer with differential outputs. The output data of the multiplexers can be controlled individually via the select inputs or as a group via the common select input. The flexible selection scheme makes the device useful for both data path and random logic applications.

The 100 Series Contains Temperature Compensation

Features

- Individual or Common Select Controls
- 500 ps Typical Propagation Delays
- PECL Mode Operating Range: $V_{CC} = 4.2\text{ V}$ to 5.7 V with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -4.2\text{ V}$ to -5.7 V
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Internal Input Pulldown Resistors
- ESD Protection: Human Body Model; $> 2\text{ kV}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level:
 - Pb = 1
 - Pb-Free = 3

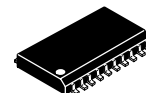
For Additional Information, see Application Note AND8003/D

- Flammability Rating: UL 94 V-0 @ 1.125 in, Oxygen Index: 28 to 34
- Transistor Count = 182 devices
- Pb-Free Package is Available*



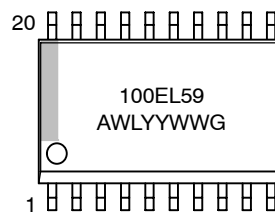
ON Semiconductor®

<http://onsemi.com>



SO-20
WB SUFFIX
CASE 751D

MARKING DIAGRAM*



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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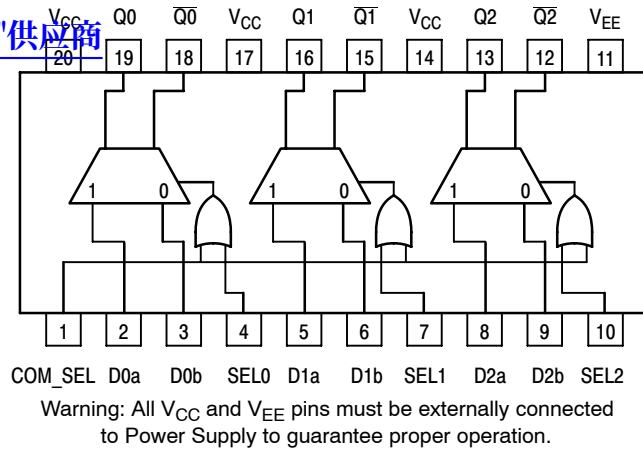


Figure 1. Logic Diagram and Pinout: 20-Lead SOIC (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0a–D2a	ECL Input Data a*
D0b–D2b	ECL Input Data b*
SEL0–SEL2	ECL Individual Select Input*
COM_SEL	ECL Common Select Input*
Q0–Q2; $\overline{Q0}$ – $\overline{Q2}$	ECL Differential Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

*Pins will default LOW when left open.

Table 2. TRUTH TABLE

SEL*	DATA
H	a
L	b

*Pins will default LOW when left open.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8 to 0	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 lfpm 500 lfpm	SOIC–20 SOIC–20	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	Standard Board	SOIC–20	30 to 35	°C/W
T_{sol}	Wave Solder Pb Pb–Free			265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 4. PECL DC CHARACTERISTICS $V_{CC} = 5.0 \text{ V}$; $V_{EE} = 0.0 \text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		130	156		130	156		130	156	mA
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0 \text{ V}$.

Table 5. NECL DC CHARACTERISTICS $V_{CC} = 0.0 \text{ V}$; $V_{EE} = -5.0 \text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 4)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 4)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.
4. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0 \text{ V}$.

Table 6. AC CHARACTERISTICS $V_{CC} = 5.0 \text{ V}$; $V_{EE} = 0.0 \text{ V}$ or $V_{CC} = 0.0 \text{ V}$; $V_{EE} = -5.0 \text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay DATA to Q/ $\bar{Q}$ SEL to Q/ $\bar{Q}$ COM_SEL to Q/ $\bar{Q}$	340 340 340		690 690 690	340 340 340		690 690 690	340 340 340		690 690 690	ps
t_{skew}	Output-Output Skew Any D_n , D_m to Q			100			100			100	ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% - 80%)	200		540	200		540	200		540	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. V_{EE} can vary +0.8 V / -0.5 V.

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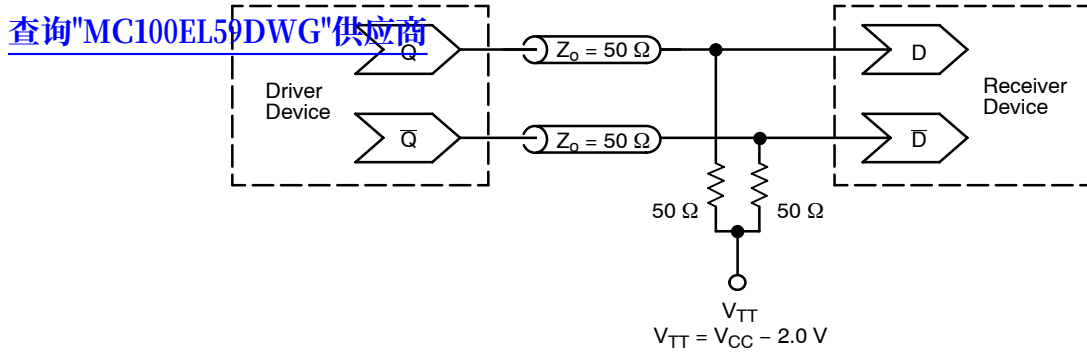


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100EL59DW	SOIC–20	38 Units / Rail
MC100EL59DWG	SOIC–20 (Pb–Free)	38 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

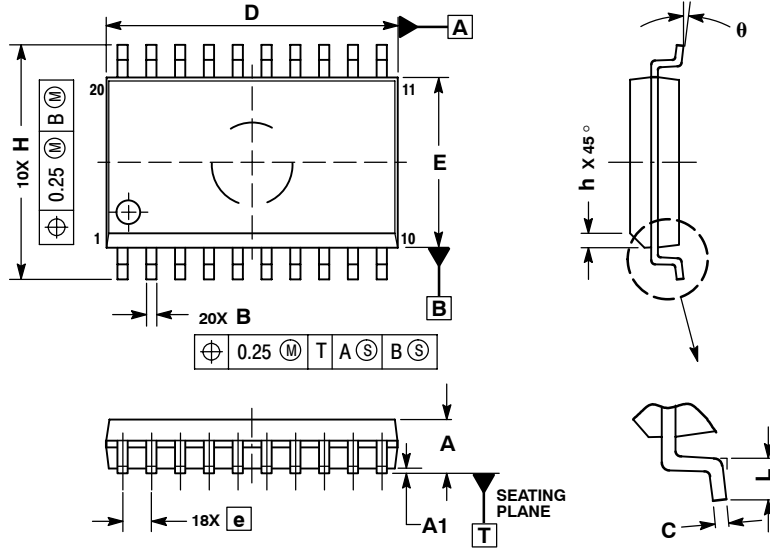
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

SO-20 WB
CASE 751D-05
ISSUE G



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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