December 1, 2008

DS90LV049Q
Automotive LVDS Dual Line Driver and Receiver Pair

General Description

The DS90LV049Q is a dual CMOS flow-through differential line driver-receiver pair designed for applications requiring ultra low power dissipation, exceptional noise immunity, and high data throughput. The device is designed to support data rates in excess of 400 Mbps utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV049Q drivers accept LVTTL/LVCMOS signals and translate them to LVDS signals. The receivers accept LVDS signals and translate them to 3 V CMOS signals. The LVDS input buffers have internal failsafe biasing that places the outputs to a known H (high) state for floating receiver inputs. In addition, the DS90LV049Q supports a TRI-STATE function for a low idle power state when the device is not in use.

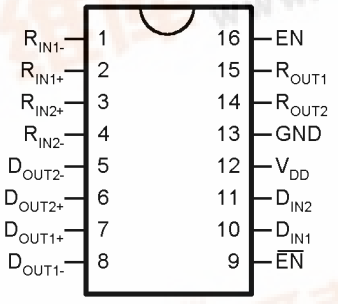
The EN and $\overline{EN}$ inputs are ANDed together and control the TRI-STATE outputs. The enables are common to all four gates.

Features

- AECQ-100 Grade 1
- Up to 400 Mbps switching rates
- Flow-through pinout simplifies PCB layout
- 50 ps typical driver channel-to-channel skew
- 50 ps typical receiver channel-to-channel skew
- 3.3 V single power supply design
- TRI-STATE output control
- Internal fail-safe biasing of receiver inputs
- Low power dissipation (70 mW at 3.3 V static)
- High impedance on LVDS outputs on power down
- Conforms to TIA/EIA-644-A LVDS Standard
- Available in low profile 16 pin TSSOP package

Connection Diagram

Dual-In-Line



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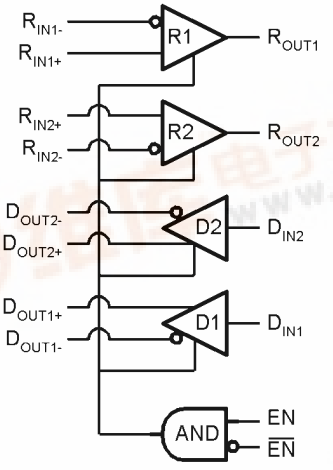
Order Number DS90LV049QMT
Order Number DS90LV049QMTX (Tape and Reel)
See NS Package Number MTC16

Functional Diagram



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Truth Table

EN	$\overline{EN}$	LVDS Out	LVCMOS Out
L or Open	L or Open	OFF	OFF
H	L or Open	ON	ON
L or Open	H	OFF	OFF
H	H	OFF	OFF

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3 V to +4 V
LVCMOS Input Voltage (D_{IN})	−0.3 V to (V_{DD} + 0.3 V)
LVDS Input Voltage (R_{IN+}, R_{IN-})	−0.3 V to +3.9 V
Enable Input Voltage (EN, $\overline{EN}$)	−0.3 V to (V_{DD} + 0.3 V)
LVCMOS Output Voltage (R_{OUT})	−0.3 V to (V_{DD} + 0.3 V)
LVDS Output Voltage (D_{OUT+}, D_{OUT-})	−0.3 V to +3.9 V
LVCMOS Output Short Circuit Current (R_{OUT})	100 mA
LVDS Output Short Circuit Current (D_{OUT+}, D_{OUT-})	24 mA
LVDS Output Short Circuit Current Duration(D_{OUT+}, D_{OUT-})	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+135°C
Maximum Package Power Dissipation @ +25°C	
MT Package	1146 mW
Derate MT Package	10.4 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	96.0°C/W
θ_{JC}	30.0°C/W
ESD Rating	
HBM (Note 1)	≥ 8 kV
MM (Note 2)	≥ 250 V
CDM (Note 3)	≥ 1250 V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.0	+3.3	+3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+125	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Notes 5, 7, 9)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
LVCMOS Input DC Specifications (Driver Inputs, ENABLE Pins)							
V_{IH}	Input High Voltage		D_{IN} EN $\overline{EN}$	2.0		V_{DD}	V
V_{IL}	Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{DD}$		−10	1	+10	µA
I_{IL}	Input Low Current	V_{IN} = GND		−10	−0.1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.6		V
LVDS Output DC Specifications (Driver Outputs)							
$\lvert V_{OD} \rvert$	Differential Output Voltage	R_L = 100 Ω (*Figure 1*)	D_{OUT-} D_{OUT+}	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States				1	35	mV
V_{OS}	Offset Voltage			1.125	1.23	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				1	25	mV
I_{OS}	Output Short Circuit Current (Note 17)	ENABLED, $D_{IN} = V_{DD}$, D_{OUT+} = 0 V or D_{IN} = GND, D_{OUT-} = 0 V			−5.8	−9.0	mA
I_{OSD}	Differential Output Short Circuit Current (Note 17)	ENABLED, V_{OD} = 0 V			−5.8	−9.0	mA
I_{OFF}	Power-off Leakage	V_{OUT} = 0 V or 3.6 V, V_{DD} = 0 V or Open		−20	±1	+20	µA
I_{OZ}	Output TRI-STATE Current	EN = 0 V and $\overline{EN}$ = V_{DD}, V_{OUT} = 0 V or V_{DD}		−10	±1	+10	µA

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
LVDS Input DC Specifications (Receiver Inputs)							
V_{TH}	Differential Input High Threshold	V_{CM} = 1.2 V, 0.05 V, 2.35 V	R_{IN+} R_{IN-}		−15	35	mV
V_{TL}	Differential Input Low Threshold			-100	−15		mV
V_{CMR}	Common-Mode Voltage Range	V_{ID} = 100 mV, V_{DD}=3.3 V		0.05		3	V
I_{IN}	Input Current	V_{DD}=3.6 V V_{IN} =0 V or 2.8 V		−12	±4	+12	µA
		V_{DD}=0 V V_{IN} =0 V or 2.8 V or 3.6 V		−10	±1	+10	µA
LVCMOS Output DC Specifications (Receiver Outputs)							
V_{OH}	Output High Voltage	I_{OH} = -0.4 mA, V_{ID}= 200 mV	R_{OUT}	2.7	3.3		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = 200 mV			0.05	0.25	V
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} =0 V or V_{DD}		-10	±1	+10	µA
General DC Specifications							
I_{DD}	Power Supply Current (Note 6)	EN = 3.3 V	V_{DD}		21	35	mA
I_{DDZ}	TRI-State Supply Current	EN = 0 V			15	25	mA

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Notes 7, 16)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS Outputs (Driver Outputs)						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100 Ω (*Figure 2* and *Figure 3*)		0.7	2	ns
t_{PLHD}	Differential Propagation Delay Low to High			0.7	2	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Notes 8, 10)		0	0.05	0.4	ns
t_{SKD2}	Differential Channel-to-Channel Skew (Notes 8, 11)		0	0.05	0.5	ns
t_{SKD3}	Differential Part-to-Part Skew (Notes 8, 12)		0		1.0	ns
t_{TLH}	Rise Time (Note 8)		0.2	0.4	1	ns
t_{THL}	Fall Time (Note 8)		0.2	0.4	1	ns
t_{PHZ}	Disable Time High to Z	R_L = 100 Ω (*Figure 4* and *Figure 5*)		1.5	3	ns
t_{PLZ}	Disable Time Low to Z			1.5	3	ns
t_{PZH}	Enable Time Z to High		1	3	6	ns
t_{PZL}	Enable Time Z to Low		1	3	6	ns
f_{MAX}	Maximum Operating Frequency (Note 19)			250		MHz
LVCMOS Outputs (Receiver Outputs)						
t_{PHL}	Propagation Delay High to Low	(*Figure 6* and *Figure 7*)	0.5	2	3.5	ns
t_{PLH}	Propagation Delay Low to High		0.5	2	3.5	ns
t_{SK1}	Pulse Skew $\|t_{PHL} - t_{PLH}\|$ (Note 13)		0	0.05	0.4	ns
t_{SK2}	Channel-to-Channel Skew (Note 14)		0	0.05	0.5	ns
t_{SK3}	Part-to-Part Skew (Note 15)		0		1.0	ns
t_{TLH}	Rise Time(Note 8)		0.3	0.9	1.4	ns
t_{THL}	Fall Time(Note 8)		0.3	0.75	1.4	ns
t_{PHZ}	Disable Time High to Z	(*Figure 8* and *Figure 9*)	3	5.6	8	ns
t_{PLZ}	Disable Time Low to Z		3	5.4	8	ns
t_{PZH}	Enable Time Z to High		2.5	4.6	7	ns
t_{PZL}	Enable Time Z to Low		2.5	4.6	7	ns
f_{MAX}	Maximum Operating Frequency (Note 20)			250		MHz

Note 4: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Note 5: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{TH}, V_{TL}, V_{ID} and ΔV_{OD}.

Note 6: Both, driver and receiver inputs are static. All LVDS outputs have 100 Ω load. All LVCMOS outputs are floating. None of the outputs have any lumped capacitive load.

Note 7: All typical values are given for: V_{DD} = +3.3 V, T_A = +25°C.

Note 8: These parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.

Note 9: The DS90LV049Q drivers are current mode devices and only function within datasheet specifications when a resistive load is applied to their outputs. The typical range of the resistor values is 90 Ω to 110 Ω.

Note 10: t_{SKD1} or differential pulse skew is defined as $|t_{PHLD} - t_{PLHD}|$. It is the magnitude difference in the differential propagation delays between the positive going edge and the negative going edge of the same driver channel.

Note 11: t_{SKD2} or differential channel-to-channel skew is defined as the magnitude difference in the differential propagation delays between two driver channels on the same device.

Note 12: t_{SKD3} or differential part-to-part skew is defined as $|t_{PLHD\ Max} - t_{PLHD\ Min}|$ or $|t_{PHLD\ Max} - t_{PHLD\ Min}|$. It is the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.

Note 13: t_{SK1} or pulse skew is defined as $|t_{PHL} - t_{PLH}|$. It is the magnitude difference in the propagation delays between the positive going edge and the negative going edge of the same receiver channel.

Note 14: t_{SK2} or channel-to-channel skew is defined as the magnitude difference in the propagation delays between two receiver channels on the same device.

Note 15: t_{SK3} or part-to-part skew is defined as $|t_{PLH\ Max} - t_{PLH\ Min}|$ or $|t_{PHL\ Max} - t_{PHL\ Min}|$. It is the difference between the minimum and maximum specified propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.

Note 16: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, $t_r \leq$ 1 ns, and $t_f \leq$ 1 ns.

Note 17: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 18: All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.

Note 19: f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output Criteria: duty cycle = 45%/55%, $V_{OD} > 250$ mV, all channels switching.

Note 20: f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, V_{ID} = 200 mV, V_{CM} = 1.2 V . Output Criteria: duty cycle = 45%/55%, $V_{OH} >$ 2.7 V, $V_{OL} <$ 0.25 V, all channels switching.

Parameter Measurement Information

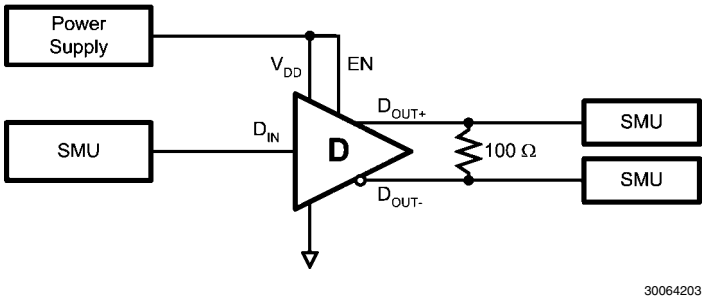


FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit

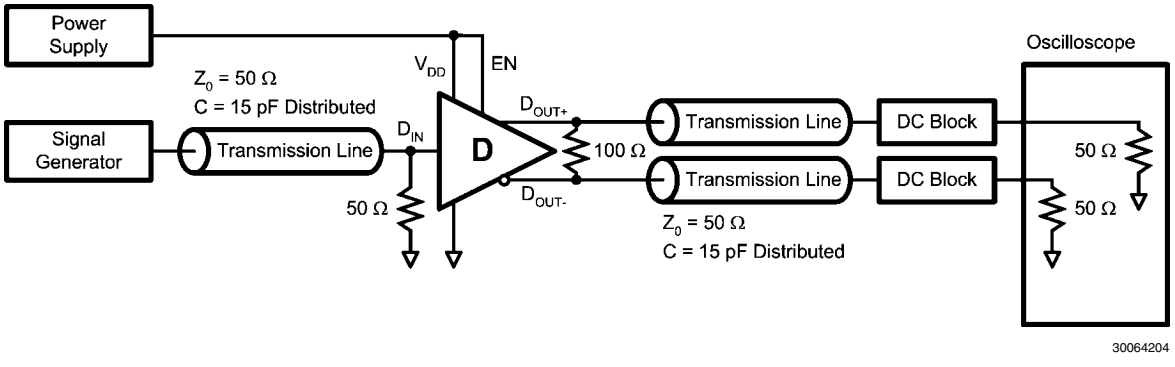


FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit

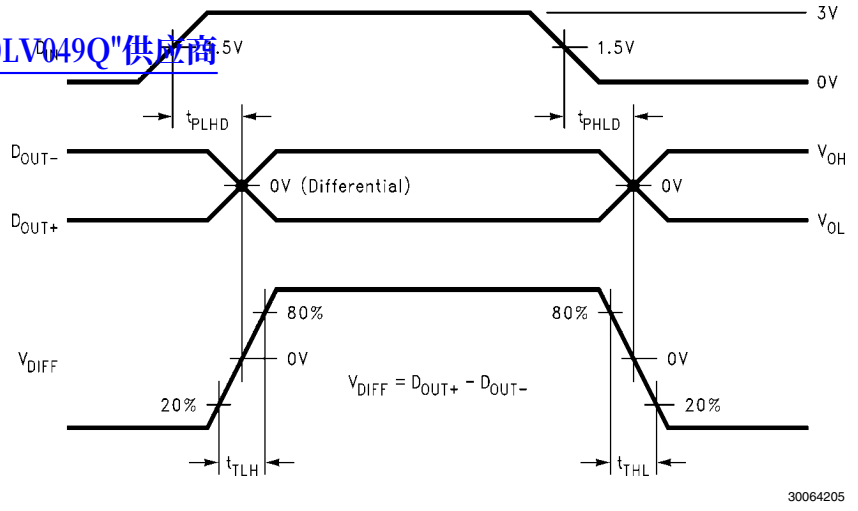


FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

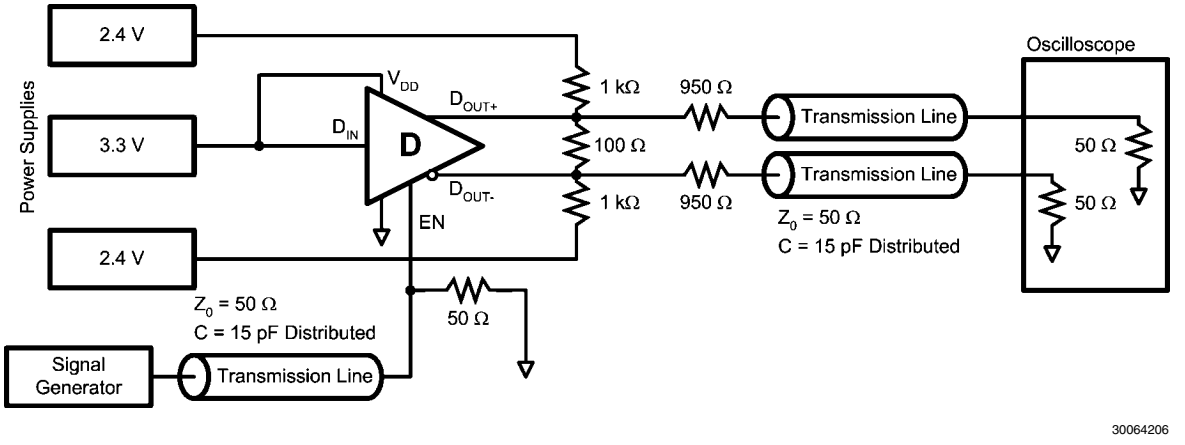


FIGURE 4. Driver TRI-STATE Delay Test Circuit

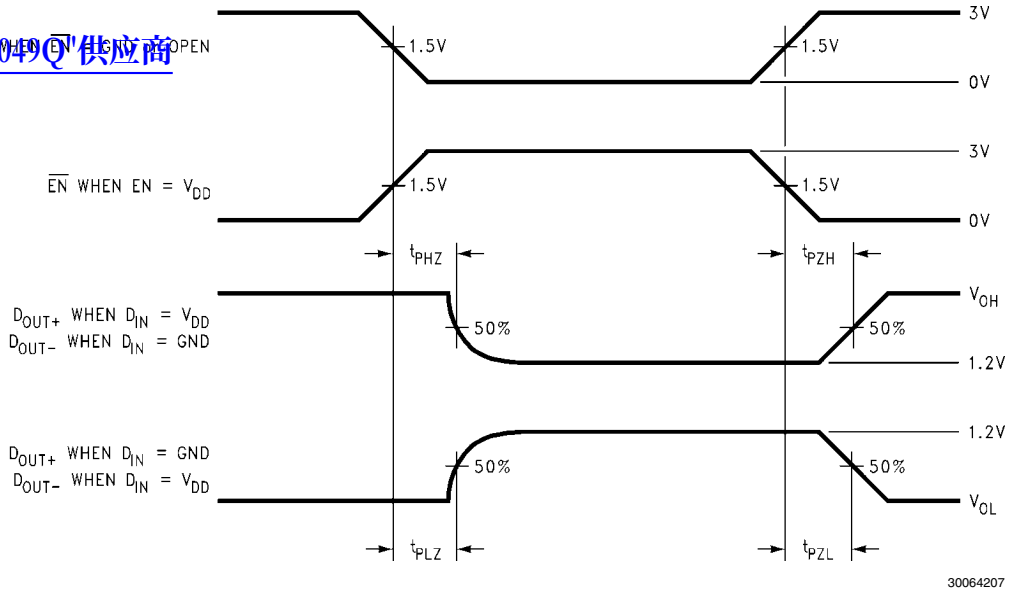


FIGURE 5. Driver TRI-STATE Delay Waveform

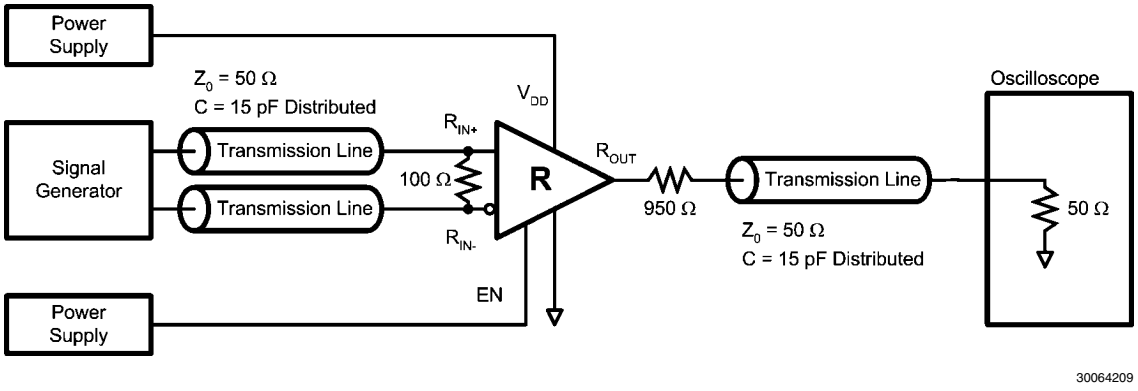


FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit

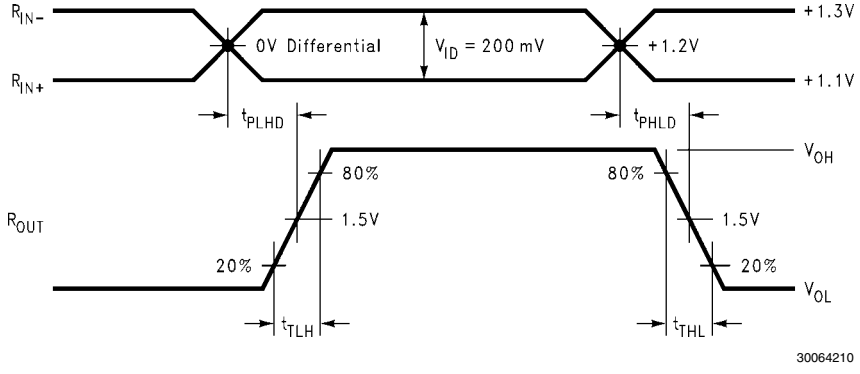


FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms

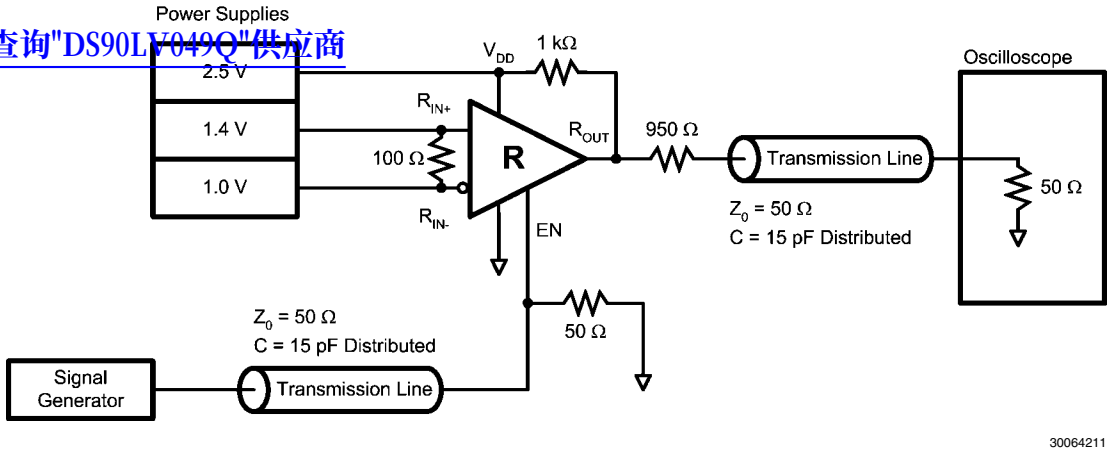


FIGURE 8. Receiver TRI-STATE Delay Test Circuit

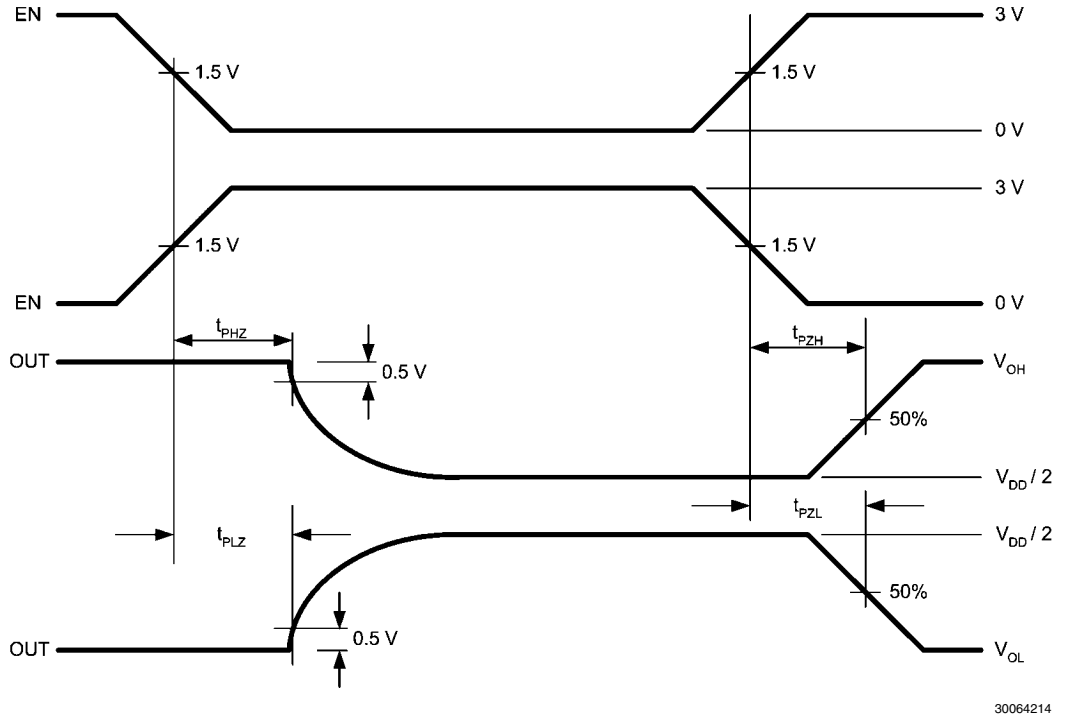


FIGURE 9. Receiver TRI-STATE Delay Waveforms

Typical Application

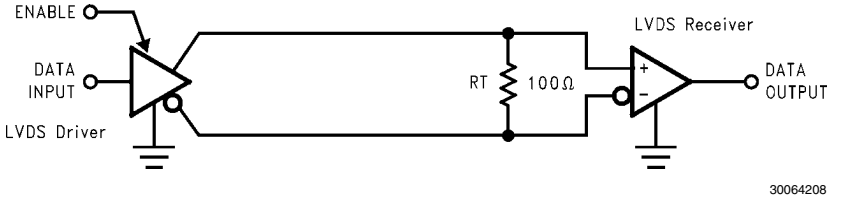


FIGURE 10. Point-to-Point Application

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-003), AN-805, AN-808, AN-903, AN-916, AN-971, AN-977.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 10*. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω (selected to match the media), and is located as close to the receiver input pins as possible. The termination resistor converts the driver output current (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The TRI-STATE function allows the device outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The DS90LV049Q has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1 µF and 0.001 µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10 µF (35 V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC BOARD CONSIDERATIONS

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (i.e. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10 mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number or vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10 mm (12 mm MAX).

PROBING LVDS TRANSMISSION LINES

Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100 Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

FAIL-SAFE FEATURE

An LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20 mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating receiver inputs.

The DS90LV049Q has two receivers, and if an application requires a single receiver, the unused receiver inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down current sources to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5 kΩ to 15 kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry.

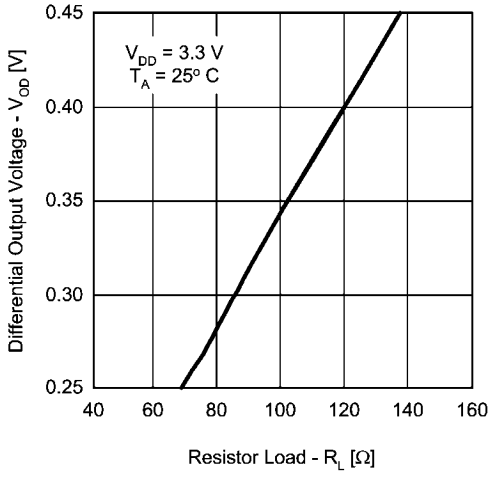
For more information on failsfe biasing of LVDS interfaces please refer to AN-1194.

Pin Descriptions

Pin No.	Name	Description
10, 11	D_{IN}	Driver input pins, LVCMOS levels. There is a pull-down current source present.
6, 7	D_{OUT+}	Non-inverting driver output pins, LVDS levels.
5, 8	D_{OUT-}	Inverting driver output pins, LVDS levels.
2, 3	R_{IN+}	Non-inverting receiver input pins, LVDS levels. There is a pull-up current source present.
1, 4	R_{IN-}	Inverting receiver input pins, LVDS levels. There is a pull-down current source present.
14, 15	R_{OUT}	Receiver output pins, LVCMOS levels.
9, 16	EN, $\overline{EN}$	Enable and Disable pins. There are pull-down current sources present at both pins.
12	V_{DD}	Power supply pin.
13	GND	Ground pin.

Typical Performance Curves

Differential Output Voltage vs Load Resistor



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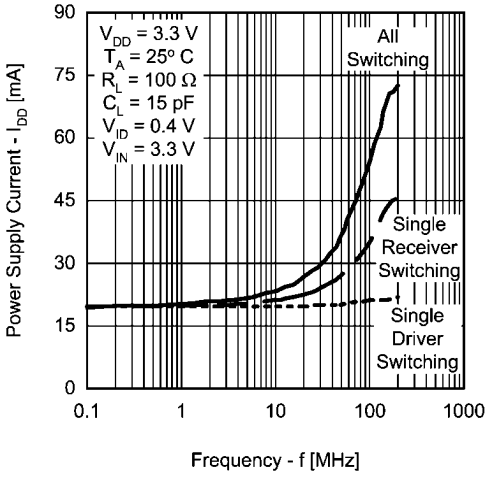
Power Supply Current vs Frequency



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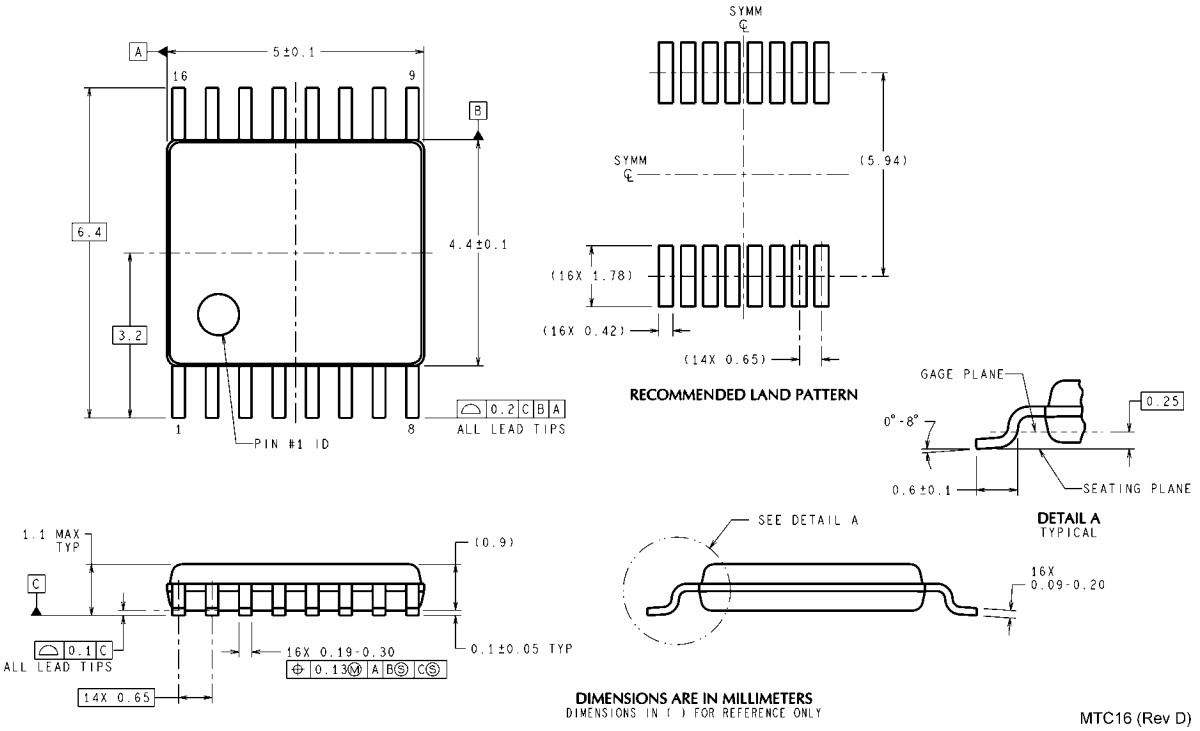
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead (0.100″ Wide) Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90LV049QMT
Order Number DS90LV049QMTX (Tape and Reel)
NS Package Number MTC16

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
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Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

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