查询"NCS2530ADG"供应商

NCS2530, NCS2530A

Triple 1.1 mA 200 MHz Current Feedback Op Amp with Enable Feature

NCS2530 is a triple 1.1 mA 200 MHz current feedback monolithic operational amplifier featuring high slew rate and low differential gain and phase error. The current feedback architecture allows for a superior bandwidth and low power consumption. This device features an enable pin.

Features

- −3.0 dB Small Signal BW (A_V = +2.0, V_O = 0.5 V_{p-p}) 200 MHz Typ
- Slew Rate 450 V/μs
- Supply Current 1.1 mA per amplifier
- Input Referred Voltage Noise 4.0 nV/$\sqrt{Hz}$
- THD −55 dB (f = 5.0 MHz, V_O = 2.0 V_{p-p})
- Output Current 100 mA
- Enable Pin Available
- These are Pb−Free Devices

Applications

- Portable Video
- Line Drivers
- Radar/Communication Receivers
- Set Top Box
- NTSC/PAL/HDTV

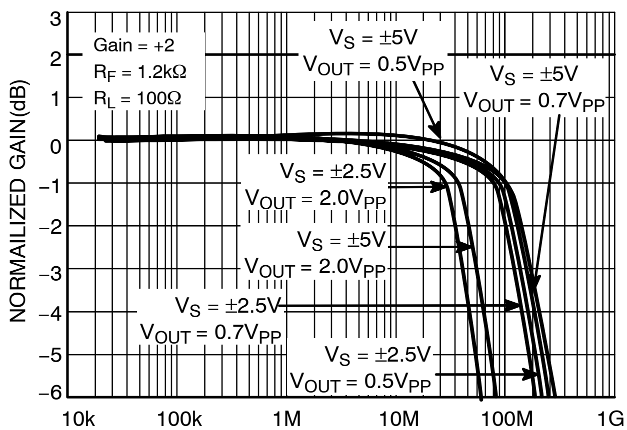

Figure 1. Frequency Response: Gain (dB) vs. Frequency Av = +2.0, R_L = 100 Ω

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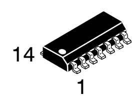
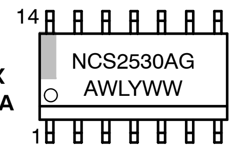
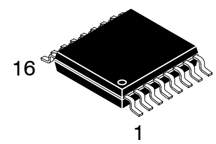
MARKING DIAGRAM

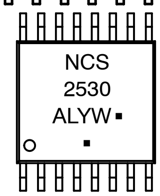


SOIC−14 D SUFFIX CASE 751A





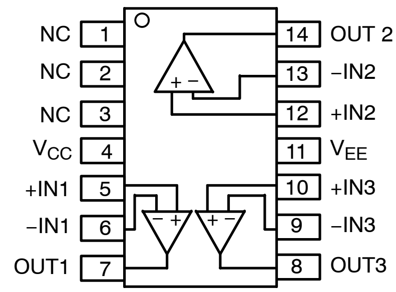
TSSOP−16 DT SUFFIX CASE 948F



A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

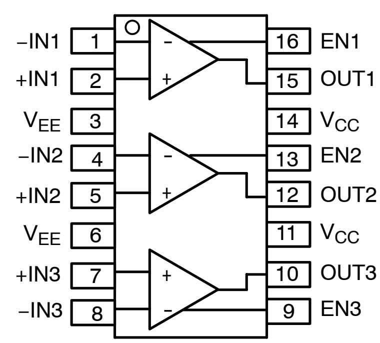
(Note: Microdot may be in either location)

SOIC−14 PINOUT (NCS2530A ONLY)



NC = NO CONNECT
(Top View)

TSSOP−16 PINOUT (NCS2530 ONLY)



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

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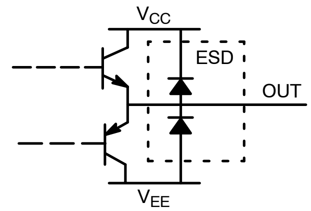
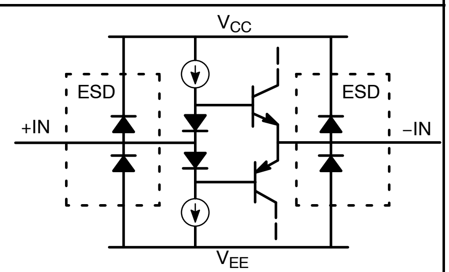
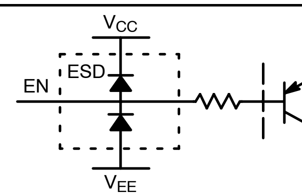
PIN FUNCTION DESCRIPTION

SOIC−14 (NCS2530A Only)	TSSOP−16 (NCS2530 Only)	Symbol	Function	Equivalent Circuit
7, 8, 14	10, 12, 15	OUTx	Output	
11	3, 6	V_{EE}	Negative Power Supply	
5, 10, 12	2, 5, 7	+INx	Non−inverted Input	
6, 9, 13	1, 4, 8	−INx	Inverted Input	See Above
4	11, 14	V_{CC}	Positive Power Supply	
N/A	9, 13, 16	EN	Enable	

ENABLE PIN TRUTH TABLE (NCS2530 Only)

	High*	Low
Enable	Enabled	Disabled

*Default open state

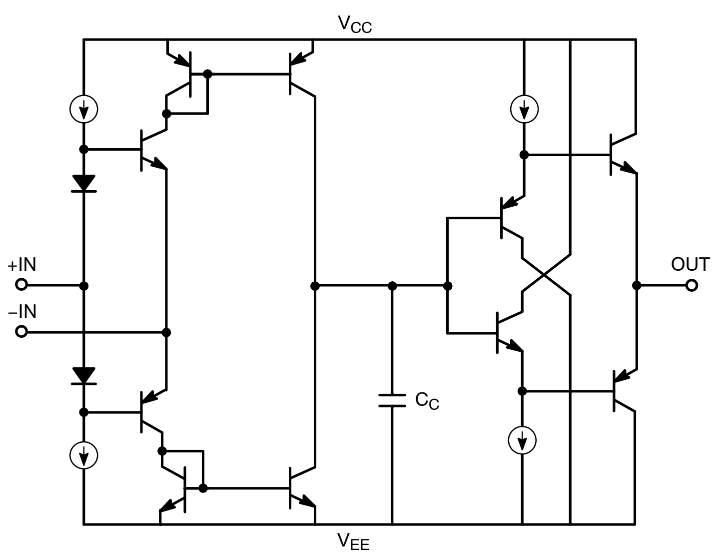


Figure 2. Simplified Device Schematic

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ATTRIBUTES

Characteristics		Value
ESD Human Body Model Machine Model Charged Device Model		 2.0 kV (Note 1) 200 V 1.0 kV
Moisture Sensitivity (Note 2)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in

1. 0.8 kV between the input pairs +IN and −IN pins only. All other pins are 2.0 kV.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Power Supply Voltage		V_S	11	V_{DC}
Input Voltage Range		V_I	$\leq V_S$	V_{DC}
Input Differential Voltage Range		V_{ID}	$\leq V_S$	V_{DC}
Output Current		I_O	100	mA
Maximum Junction Temperature (Note 3)		T_J	150	°C
Operating Ambient Temperature		T_A	−40 to +85	°C
Storage Temperature Range		T_{stg}	−60 to +150	°C
Power Dissipation		P_D	(See Graph)	mW
Thermal Resistance, Junction−to−Air	TSSOP−16 SOIC−14	$R_{\theta JA}$	178 156	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the “overheated” condition for an extended period can result in device damage.

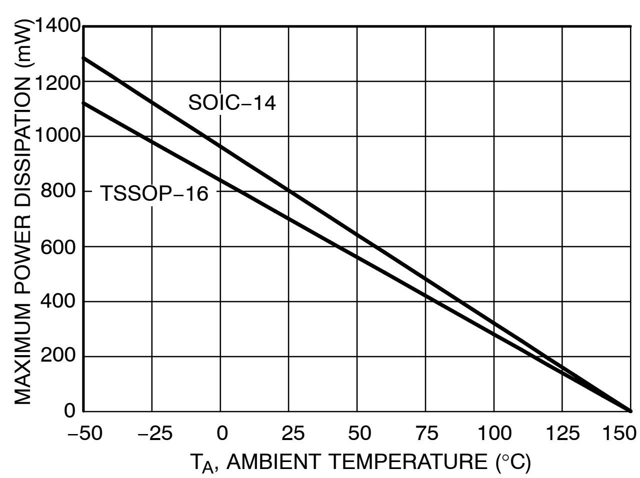

Figure 3. Power Dissipation vs. Temperature

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 100 Ω to GND, R_F = 1.2 kΩ, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 2.0 V_{p-p}		 200 140		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		30		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.02		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.1		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 2.0 V		450		V/μs
t_s	Settling Time 0.01% 0.1%	 A_V = +2.0, V_{step} = 2.0 V A_V = +2.0, V_{step} = 2.0 V		 35 18		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 2.0 V		5		ns
t_{ON}	Turn−on Time (Note 4)			900		ns
t_{OFF}	Turn−off Time (Note 4)			500		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}, R_L = 150 Ω		−55		dBc
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−67		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−57		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 2.0 V_{p-p}		35		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 2.0 V_{p-p}		58		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		4		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz, Inverting f = 1.0 MHz, Non−Inverting		15 15		$pA/\sqrt{Hz}$

4. Applies to NCS2530 device only.

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DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 100 Ω to GND, R_F = 1.2 kΩ, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage		−4.0	±0.7	+4.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		µV/°C
I_{IB}	Input Bias Current	+Input (Non−Inverting), V_O = 0 V −Input (Inverting), V_O = 0 V (Note 5)	−5.0 −5.0	±2.0 ±0.4	+5.0 +5.0	µA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	+Input (Non−Inverting), V_O = 0 V −Input (Inverting), V_O = 0 V		±40 ±10		nA/°C
V_{IH}	Input High Voltage (Enable) (Note 5 and 6)		V_{CC} − 1.5 V			V
V_{IL}	Input Low Voltage (Enable) (Note 5 and 6)				V_{CC} − 3.5 V	V
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range (Note 5)		±3.0	±4.0		V
CMRR	Common Mode Rejection Ratio	(See Graph)	50	55		dB
R_{IN}	Input Resistance	+Input (Non−Inverting) −Input (Inverting)		4.0 350		MΩ Ω
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	Closed Loop Open Loop		0.02 12		Ω
V_O	Output Voltage Swing		±3.0	±3.5		V
I_O	Output Current		±60	±100		mA
POWER SUPPLY						
V_S	Operating Voltage Supply			10		V
$I_{S,ON}$	Power Supply Current − Enabled (per amplifier)	V_O = 0 V	0.6	1.1	2.0	mA
$I_{S,OFF}$	Power Supply Current − Disabled (per amplifier) (Note 6)	V_O = 0 V		0.35	0.5	mA
	Crosstalk	Channel to Channel, f = 5.0 MHz		60		dB
PSRR	Power Supply Rejection Ratio	(See Graph)	50	60		dB

5. Guaranteed by design and/or characterization.
6. Applies to NCS2530 device only.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 100 Ω to GND, R_F = 1.2 kΩ, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 1.0 V_{p-p}		 180 130		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		15		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.02		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.1		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 1.0 V		350		V/μs
t_s	Settling Time 0.01% 0.1%	 A_V = +2.0, V_{step} = 1.0 V A_V = +2.0, V_{step} = 1.0 V		 40 18		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 1.0 V		8.0		ns
t_{ON}	Turn−on Time (Note 7)			900		ns
t_{OFF}	Turn−off Time (Note 7)			500		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}, R_L = 150 Ω		−55		dBc
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−67		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−57		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 1.0 V_{p-p}		35		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 1.0 V_{p-p}		58		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		4.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz, Inverting f = 1.0 MHz, Non−Inverting		15 15		$pA/\sqrt{Hz}$

7. Applies to NCS2530 device only.

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DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 100 Ω to GND, R_F = 1.2 kΩ, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage		−4.0	±0.5	+4.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	+Input (Non−Inverting), V_O = 0 V −Input (Inverting), V_O = 0 V (Note 8)	−5.0 −5.0	±2.0 ±0.4	+5.0 +5.0	μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	+Input (Non−Inverting), V_O = 0 V −Input (Inverting), V_O = 0 V		±40 ±10		nA/°C
V_{IH}	Input High Voltage (Enable) (Note 8 and 9)		V_{CC} − 1.5 V			V
V_{IL}	Input Low Voltage (Enable) (Note 8 and 9)				V_{CC} − 3.5 V	V
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range (Note 8)		±1.3	±1.5		V
CMRR	Common Mode Rejection Ratio	(See Graph)	50	55		dB
R_{IN}	Input Resistance	+Input (Non−Inverting) −Input (Inverting)		4.0 350		MΩ Ω
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	Closed Loop Open Loop		0.02 12		Ω
V_O	Output Voltage Swing		±1.0	±1.4		V
I_O	Output Current		±40	±80		mA
POWER SUPPLY						
V_S	Operating Voltage Supply			5.0		V
$I_{S,ON}$	Power Supply Current – Enabled (per amplifier)	V_O = 0 V	0.5	0.9	1.9	mA
$I_{S,OFF}$	Power Supply Current – Disabled (per amplifier) (Note 9)	V_O = 0 V		0.15	0.35	mA
	Crosstalk	Channel to Channel, f = 5.0 MHz		60		mA
PSRR	Power Supply Rejection Ratio	(See Graph)	50	60		dB

8. Guaranteed by design and/or characterization.
9. Applies to NCS2530 device only.

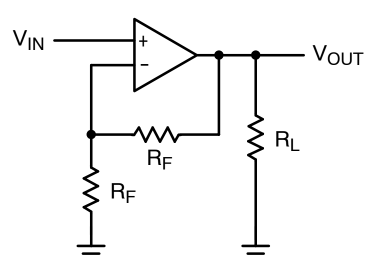

Figure 4. Typical Test Setup
(A_V = +2.0, R_F = 1.8 kΩ or 1.2 kΩ or 1.0 kΩ, R_L = 100 Ω)

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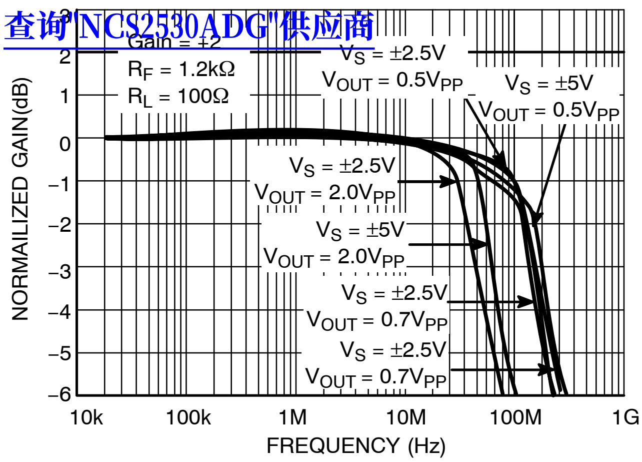

Figure 5. Frequency Response: Gain (dB) vs. Frequency Av = +2.0

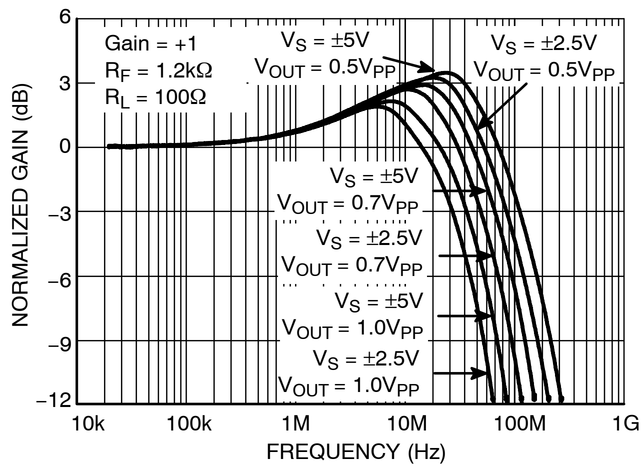

Figure 6. Frequency Response: Gain (dB) vs. Frequency Av = +1.0

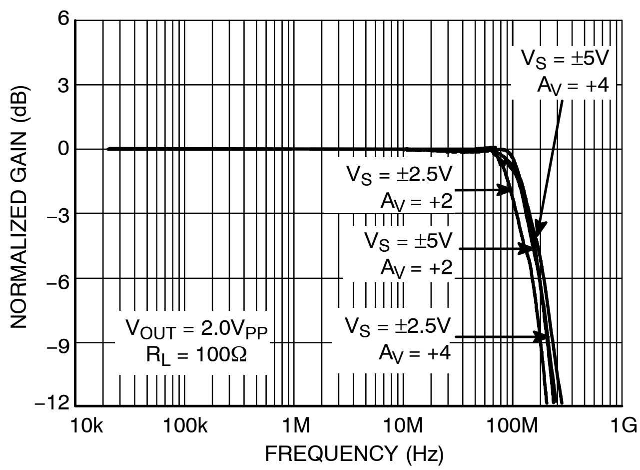

Figure 7. Large Signal Frequency Response Gain (dB) vs. Frequency

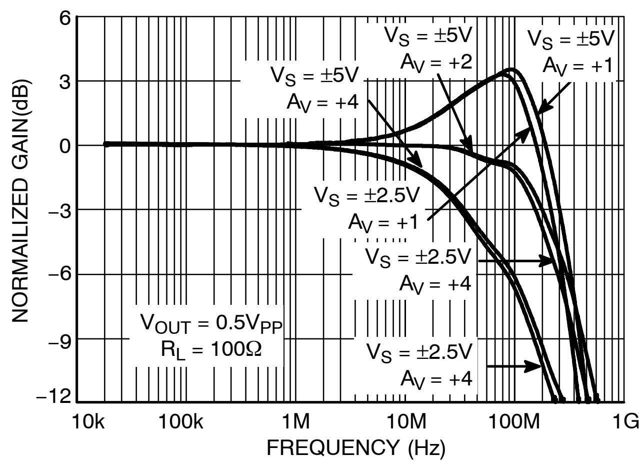

Figure 8. Small Signal Frequency Response Gain (dB) vs. Frequency

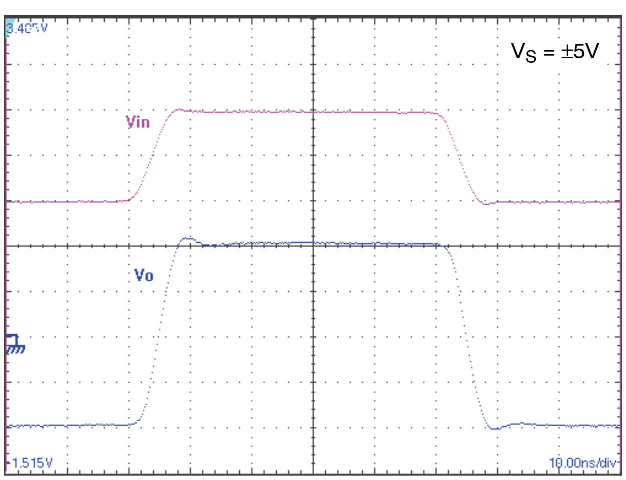

Figure 9. Small Signal Step Response
Vertical: 500 mV/div
Horizontal: 10 ns/div

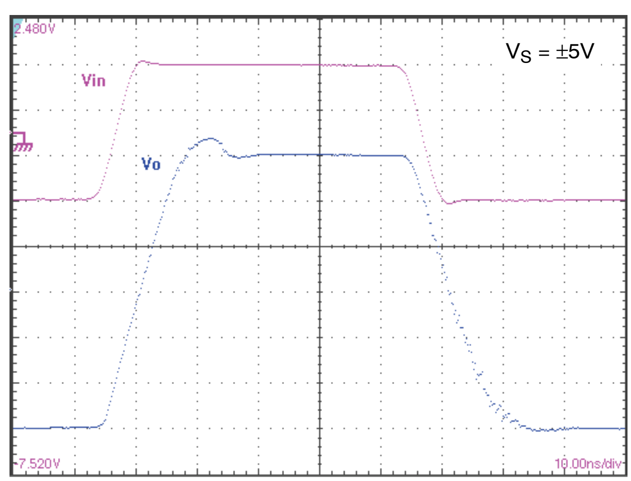

Figure 10. Large Signal Step Response
Vertical: 500 mV/div
Horizontal: 10 ns/div

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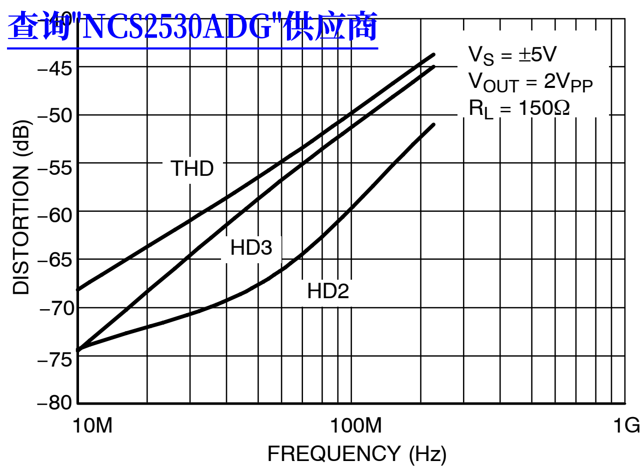

Figure 11. THD, HD2, HD3 vs. Frequency

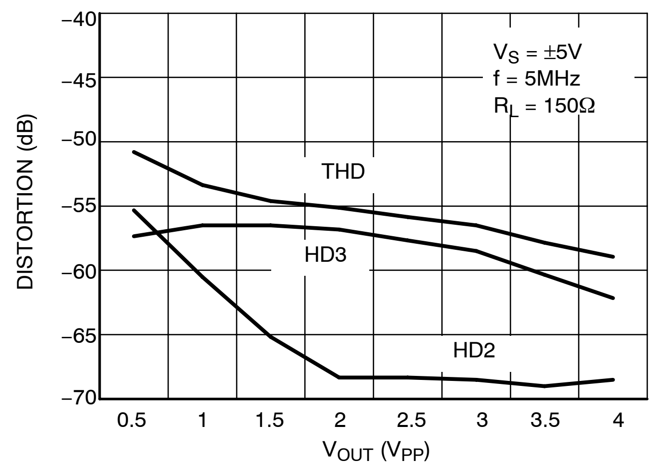

Figure 12. THD, HD2, HD3 vs. Output Voltage

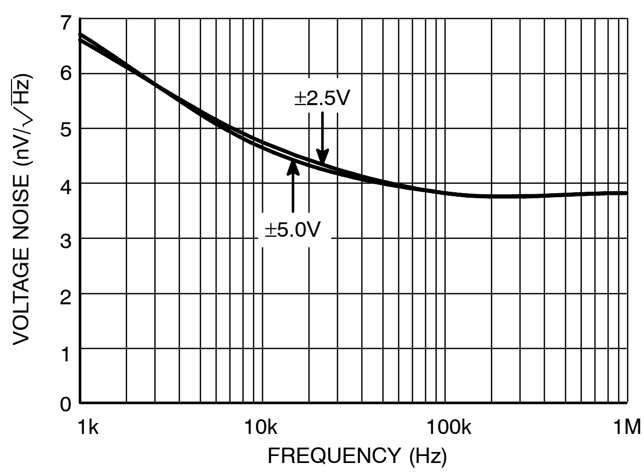

Figure 13. Input Referred Noise vs. Frequency

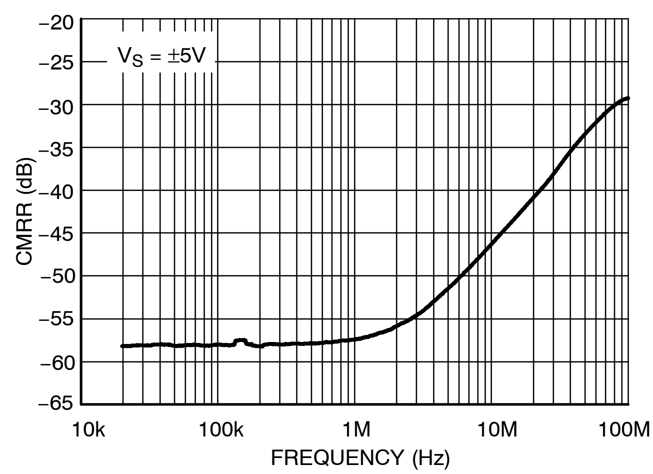

Figure 14. CMRR vs. Frequency

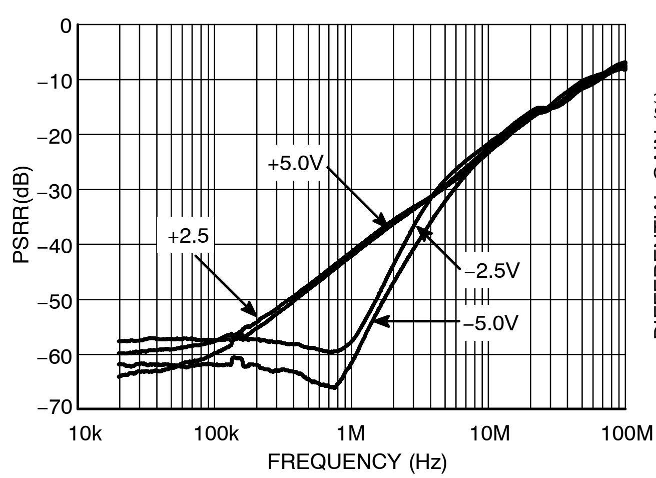

Figure 15. PSRR vs. Frequency

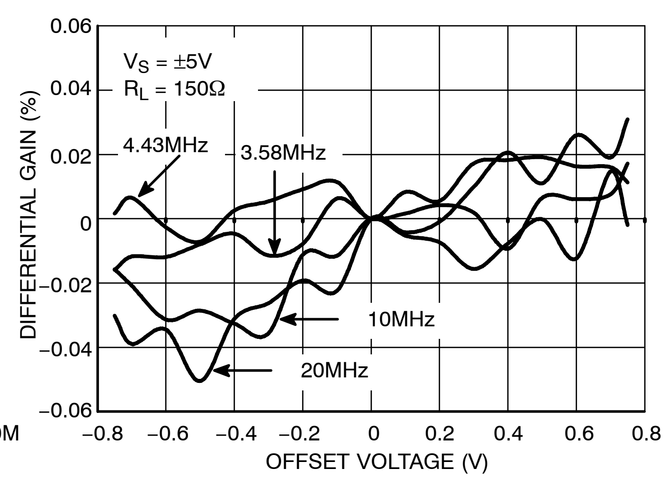

Figure 16. Differential Gain

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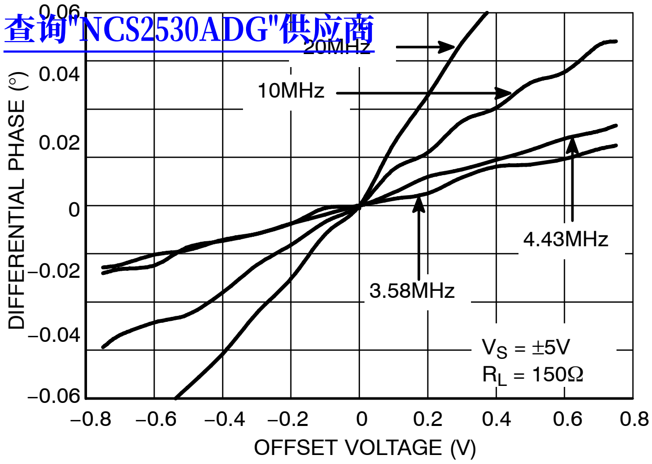

Figure 17. Differential Phase

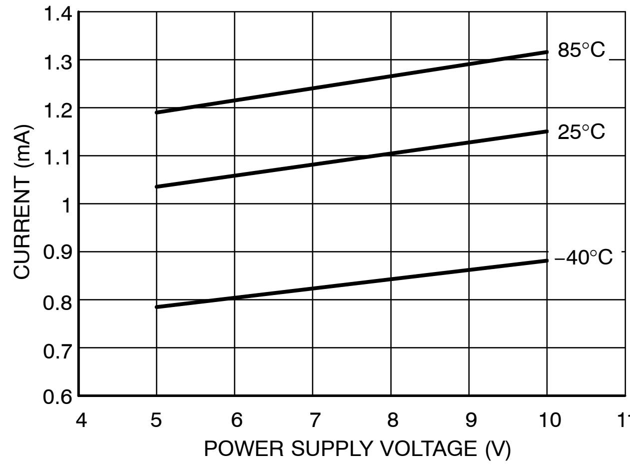

Figure 18. Supply Current per Amplifier vs. Power Supply vs. Temperature (Enabled)

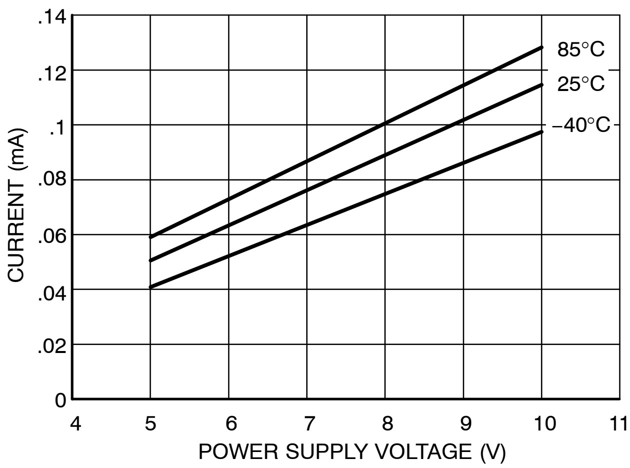

Figure 19. Supply Current per Amplifier vs. Power Supply vs. Temperature (Disabled) (NCS2530 Only)

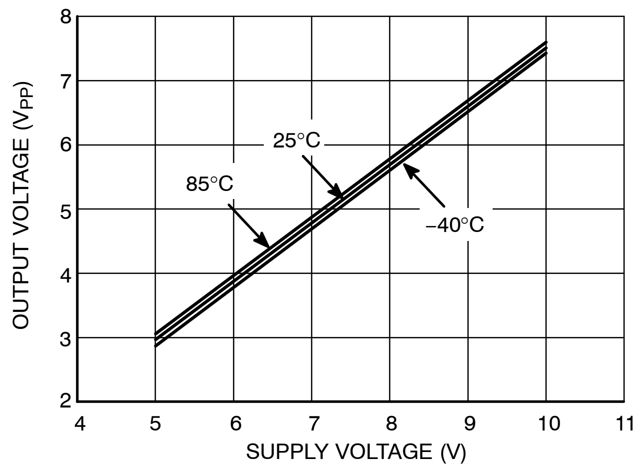

Figure 20. Output Voltage Swing vs. Supply Voltage

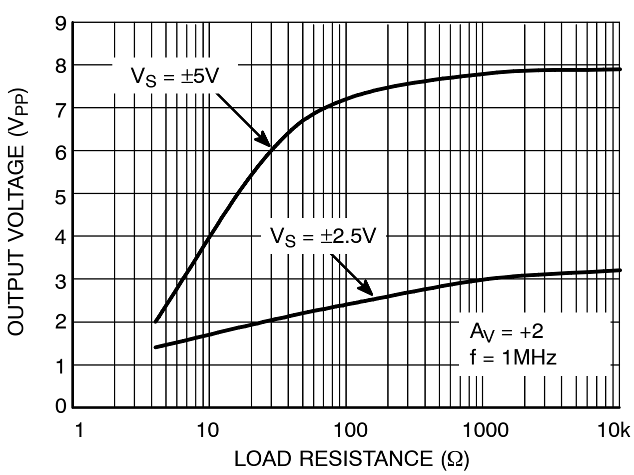

Figure 21. Output Voltage Swing vs. Load Resistance

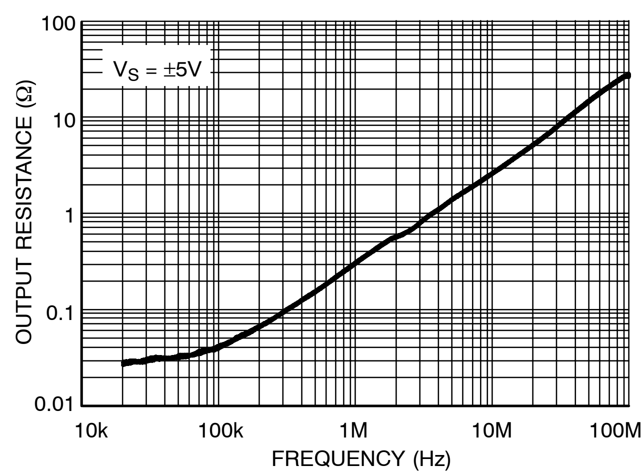

Figure 22. Output Impedance vs. Frequency

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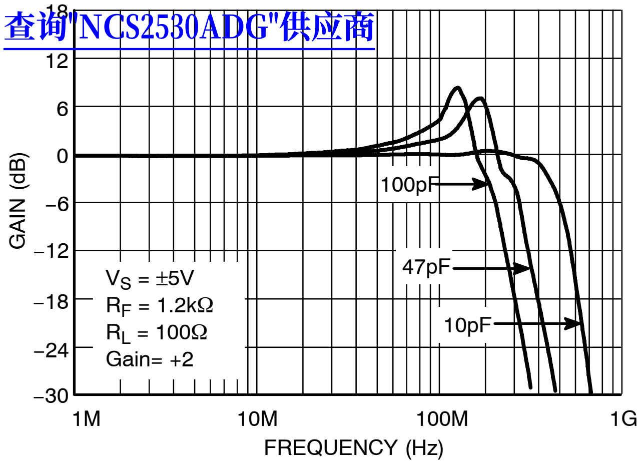

Figure 23. Frequency Response vs. Capacitive Load

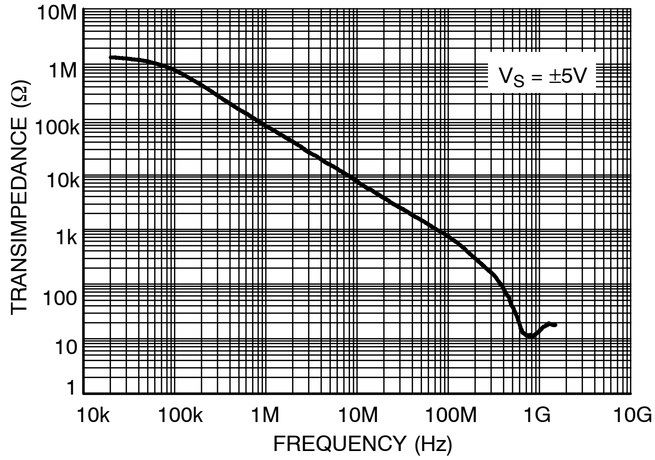

Figure 24. Transimpedance (ROL) vs. Frequency

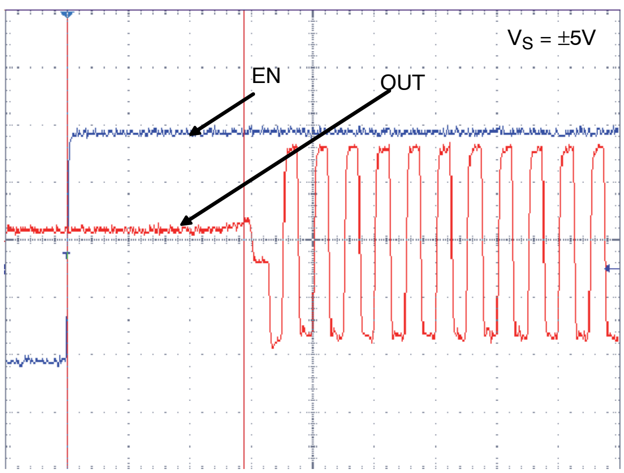

Figure 25. Turn ON Time Delay
Vertical: 10 mV/Div, Horizontal: 4 ns/Div
(Output Signal: Square Wave, 10 MHz, 2 V_{pp})
(NCS2530 Only)

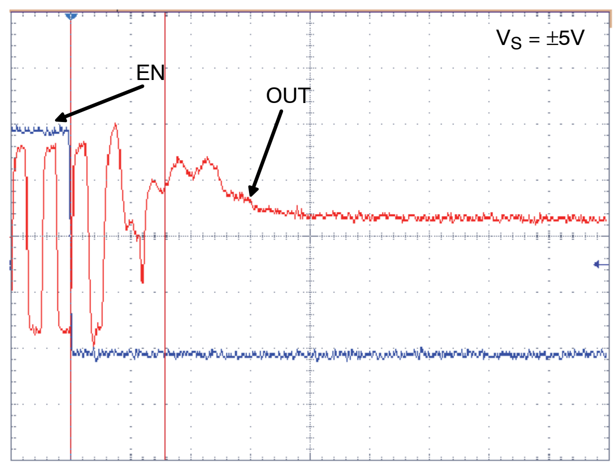

Figure 26. Turn OFF Time Delay
Vertical: 10 mV/Div, Horizontal: 4 ns/Div
(Output Signal: Square Wave, 10 MHz, 2 V_{pp})
(NCS2530 Only)

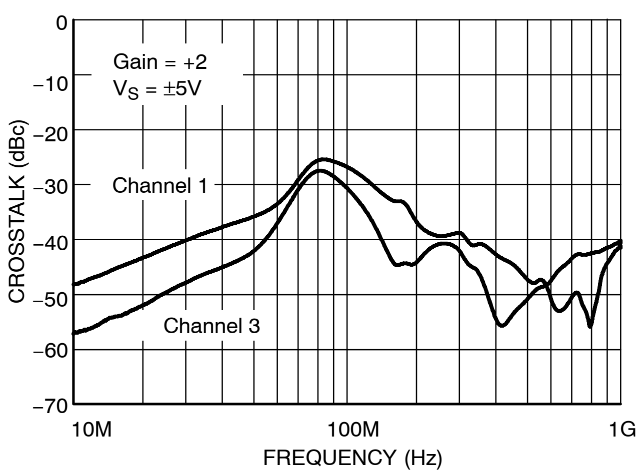

Figure 27. Crosstalk (dBc) vs. Frequency (Crosstalk measured on Channel 2 with input signal on Channel 1 and 3)

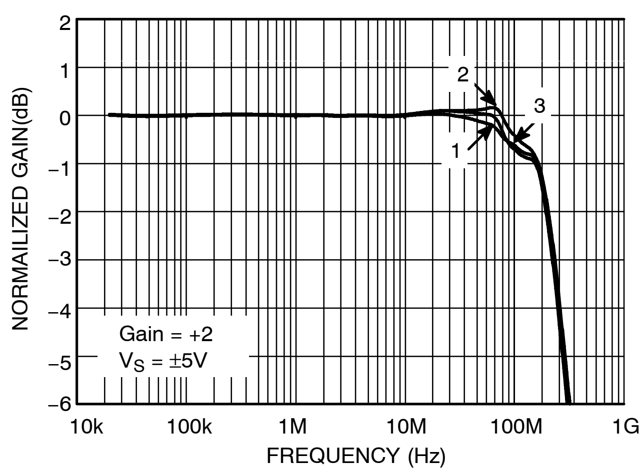

Figure 28. Channel Matching Gain (dB) vs. Frequency

General Design Considerations

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The current feedback amplifier is optimized for use in high performance video and data acquisition systems. For current feedback architecture, its closed−loop bandwidth depends on the value of the feedback resistor. The closed−loop bandwidth is not a strong function of gain, as is for a voltage feedback amplifier, as shown in Figure 29.

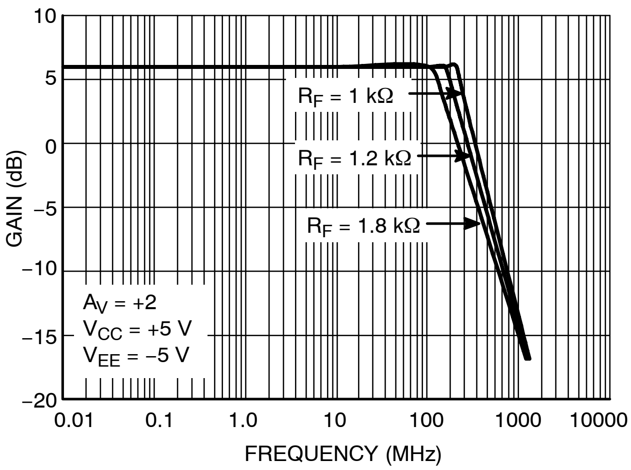

Figure 29. Frequency Response vs. R_F

The −3.0 dB bandwidth is, to some extent, dependent on the power supply voltages. By using lower power supplies, the bandwidth is reduced, because the internal capacitance increases. Smaller values of feedback resistor can be used at lower supply voltages, to compensate for this affect.

Feedback and Gain Resistor Selection for Optimum Frequency Response

A current feedback operational amplifier's key advantage is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor. To obtain a very flat gain response, the feedback resistor tolerance should be considered as well. Resistor tolerance of 1% should be used for optimum flatness. Normally, lowering RF resistor from its recommended value will peak the frequency response and extend the bandwidth while increasing the value of RF resistor will cause the frequency response to roll off faster. Reducing the value of RF resistor too far below its recommended value will cause overshoot, ringing, and eventually oscillation.

Since each application is slightly different, it is worth some experimentation to find the optimal RF for a given circuit. A value of the feedback resistor that produces ∼0.1 dB of peaking is the best compromise between stability and maximal bandwidth. It is not recommended to use a current feedback amplifier with the output shorted directly to the inverting input.

Printed Circuit Board Layout Techniques

Proper high speed PCB design rules should be used for all wideband amplifiers as the PCB parasitics can affect the overall performance. Most important are stray capacitances at the output and inverting input nodes as it can effect peaking and bandwidth. A space (3/16″ is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4″ are recommended.

Video Performance

This device designed to provide good performance with NTSC, PAL, and HDTV video signals. Best performance is obtained with back terminated loads as performance is degraded as the load is increased. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

Video Line Driver

NCS2530 can be used in video line driver applications. Figure 30 shows a typical schematic for a video driver. In some applications, two or more video loads have to be driven simultaneously as shown in Figure 31. Figure 32 shows the typical performance of the op amp with single and triple video load.

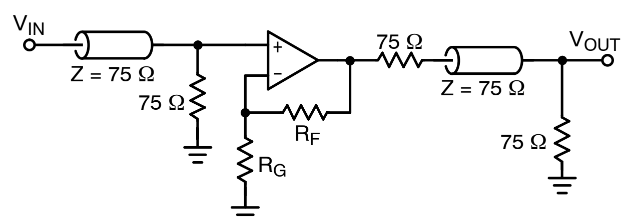

Figure 30. Video Driver Schematic

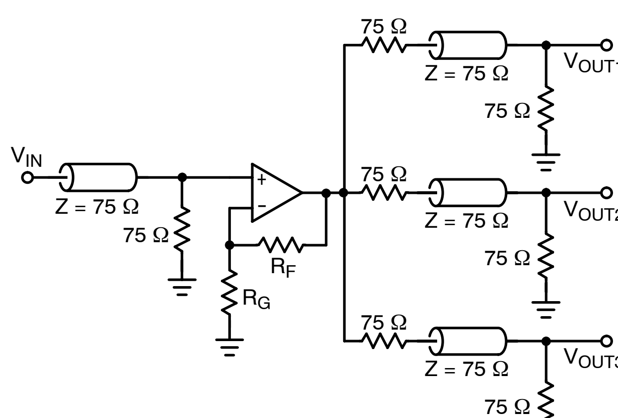

Figure 31. Video Driver Schematic for Three Video Loads

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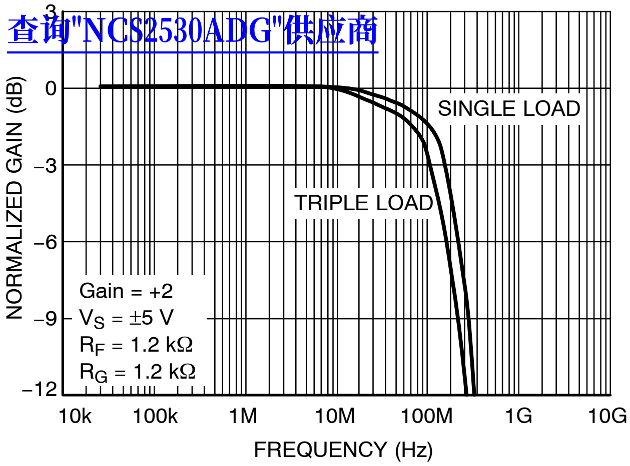

Figure 32. Frequency Response with Various Loads

ESD Protection

All device pins have limited ESD protection using internal diodes to power supplies as specified in the attributes table (See Figure 33). These diodes provide moderate protection to input overdrive voltages above the supplies. The ESD diodes can support high input currents with current limiting series resistors. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Under closed−loop operation, the ESD diodes have no effect on circuit performance. However, under certain conditions the ESD diodes will be evident. If the device is driven into a slewing condition, the ESD diodes will clamp large differential voltages until the feedback loop restores closed−loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

Note: Human Body Model for +IN and –IN pins are rated at 0.8 kV while all other pins are rated at 2.0 kV.

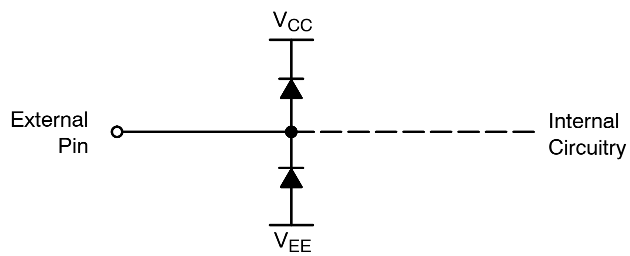

Figure 33. Internal ESD Protection

ORDERING INFORMATION

Device	Package	Shipping†
NCS2530ADG	SOIC−14 (Pb−Free)	55 Units / Rail
NCS2530ADR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
NCS2530DTBG	TSSOP−16*	96 Units / Rail
NCS2530DTBR2G	TSSOP−16*	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

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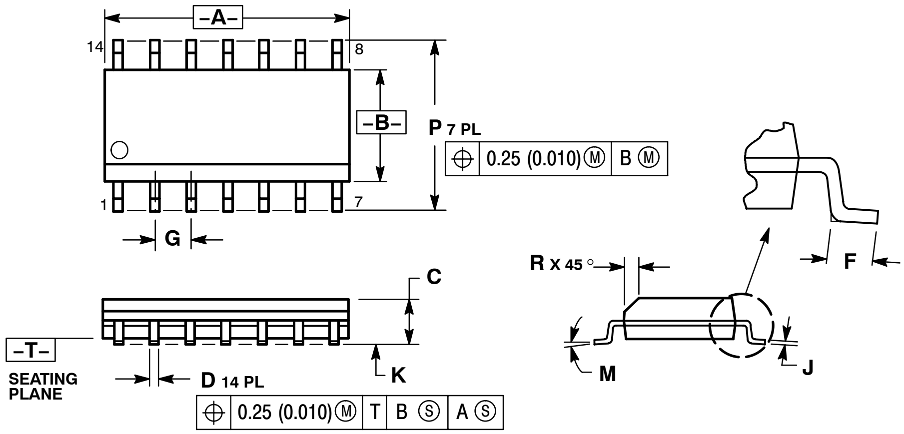
PACKAGE DIMENSIONS

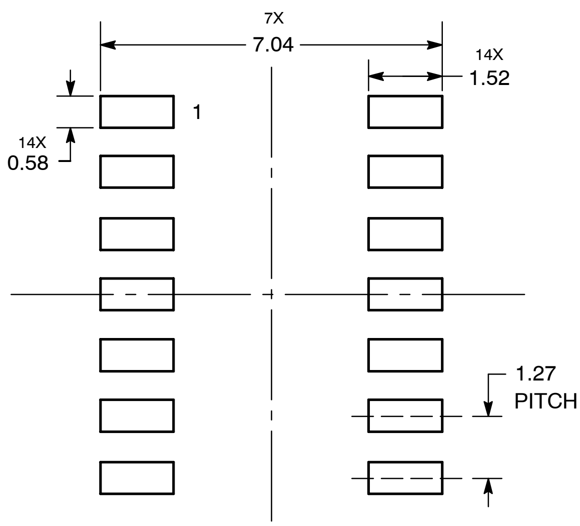
SOIC−14
CASE 751A−03
ISSUE H

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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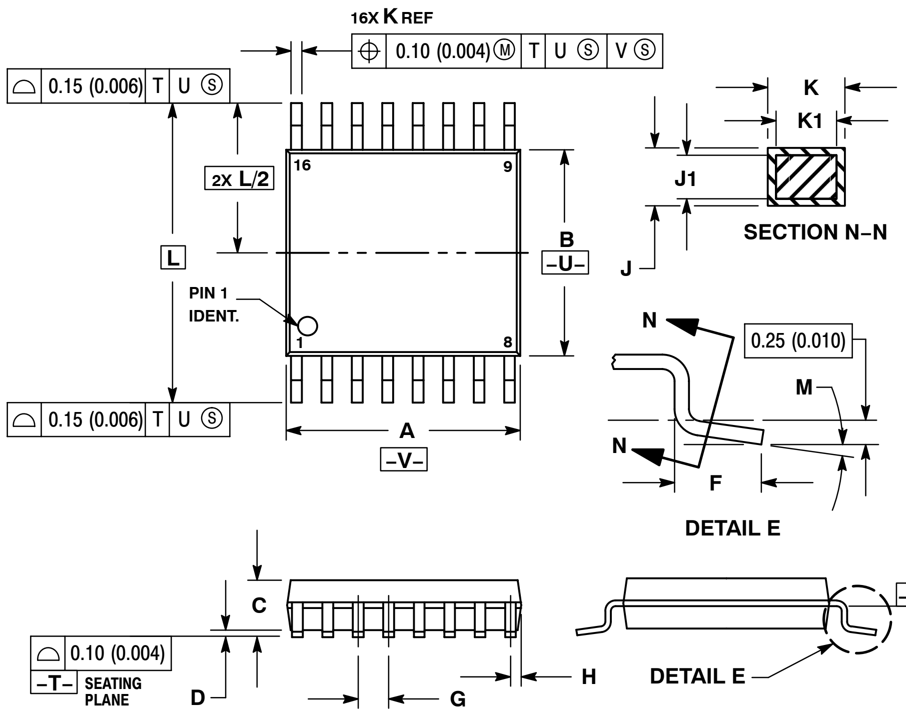
PACKAGE DIMENSIONS

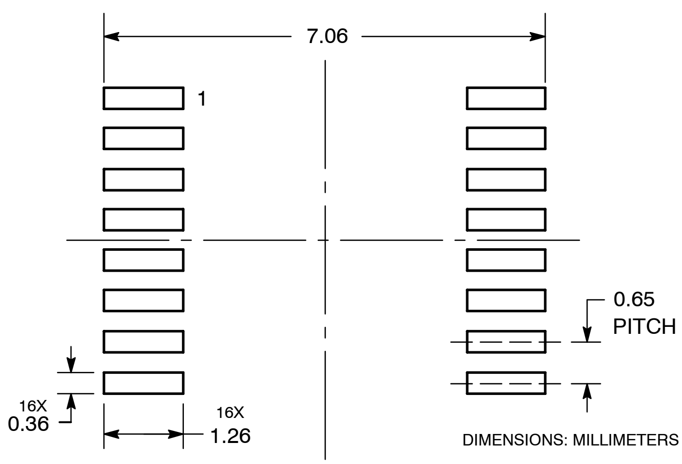
TSSOP−16
CASE 948F−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



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