REVISIONS			
	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R051-94.	93-11-30	K. A. Cottongim
B	Add device types 09 through 24.	95-01-19	K. A. Cottongim
C	Changes in accordance with NOR 5962-R121-95.	95-04-27	K. A. Cottongim
D	Changes in accordance with NOR 5962-R014-96.	95-12-15	K. A. Cottongim
E	Add device types 25 and 26. Add case outlines T and U.	98-06-11	K. A. Cottongim
F	Correct figure 1, case outline Z, pin 1 index.	98-09-11	K. A. Cottongim

REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F	F	F	F	F							
SHEET	15	16	17	18	18	20	21	22	23	24	25	26	27							

REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Steve Duncan

CHECKED BY
Michael C. Jones

APPROVED BY
Kendall A. Cottongim

DRAWING APPROVAL DATE
93-09-17

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, LINEAR, MIL-STD-1553, BC/RTU/MT, MULTIPLEXED TERMINAL

SIZE	CAGE CODE	
A	**67268**	**5962-93065**

SHEET 1 OF 27

DSCC FORM 2233
APR 97

5962-E516-98

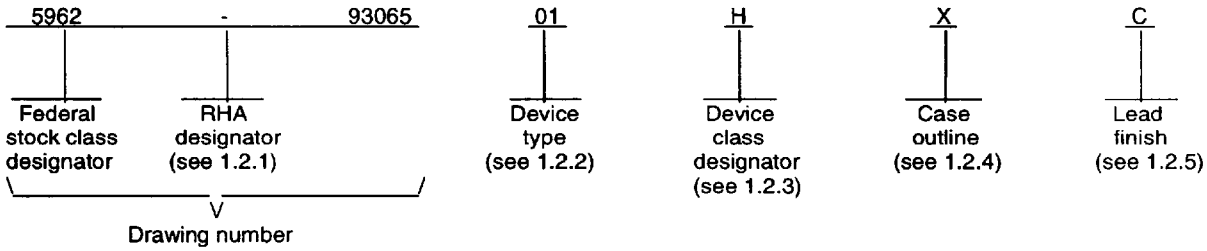
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0039168 078

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	BU-65170X1	MIL-STD-1553, RT, 4K RAM, +5/-15 V transceiver
02	BU-65170X2	MIL-STD-1553, RT, 4K RAM, +5/-12 V transceiver
03	BU-61580X1	MIL-STD-1553, BC/RT/MT, 4K RAM, +5/-15 V transceiver
04	BU-61580X2	MIL-STD-1553, BC/RT/MT, 4K RAM, +5/-12 V transceiver
05	BU-65171X1	MIL-STD-1553, RT, 4K RAM, +5/-15 V transceiver, RT address latch
06	BU-65171X2	MIL-STD-1553, RT, 4K RAM, +5/-12 V transceiver, RT address latch
07	BU-61581X1	MIL-STD-1553, BC/RT/MT, 4K RAM, +5/-15 V transceiver, RT address latch
08	BU-61581X2	MIL-STD-1553, BC/RT/MT, 4K RAM, +5/-12 V transceiver, RT address latch
09	BU-65170X3	MIL-STD-1553, RT, 4K RAM, +5 V transceiver
10	BU-65170X6	MIL-STD-1553, RT, 4K RAM, +5 V transceiver
11	BU-61580X3	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver
12	BU-61580X6	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver
13	BU-65171X3	MIL-STD-1553, RT, 4K RAM, +5 V transceiver, RT address latch
14	BU-65171X6	MIL-STD-1553, RT, 4K RAM, +5 V transceiver, RT address latch
15	BU-61581X3	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver, RT address latch
16	BU-61581X6	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver, RT address latch
17	BU-61585X1	MIL-STD-1553, BC/RT/MT, 12K RAM, +5/-15 V transceiver
18	BU-61585X2	MIL-STD-1553, BC/RT/MT, 12K RAM, +5/-12 V transceiver
19	BU-61586X1	MIL-STD-1553, BC/RT/MT, 12K RAM, +5/-15 V transceiver, RT address latch
20	BU-61586X2	MIL-STD-1553, BC/RT/MT, 12K RAM, +5/-12 V transceiver, RT address latch
21	BU-61585X3	MIL-STD-1553, BC/RT/MT, 12K RAM, +5 V transceiver
22	BU-61585X6	MIL-STD-1553, BC/RT/MT, 12K RAM, +5 V transceiver
23	BU-61586X3	MIL-STD-1553, BC/RT/MT, 12K RAM, +5 V transceiver, RT address latch
24	BU-61586X6	MIL-STD-1553, BC/RT/MT, 12K RAM, +5 V transceiver, RT address latch
25	BU-61588X3	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver
26	BU-65178X3	MIL-STD-1553, RT, 4K RAM, +5 V transceiver

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	72	Quad flat package with tie bars
U	See figure 1	81	Pin grid array
X	See figure 1	70	Dual-in-line
Y	See figure 1	70	Flat package
Z	See figure 1	70	Dual-in-line, J-lead

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Positive supply voltage range (+5VA, +5VB)	-0.3 V dc to +7.0 V dc
Negative supply voltage range (-VA, -VB)	+0.3 V dc to -18 V dc
Logic supply voltage range (+5 V logic)	-0.3 V dc to +6.0 V dc
Power dissipation (P_D): 2/ 3/ 4/	
Device types 01, 03, 05, 07, 17, and 19	2.23 W
Device types 02, 04, 06, 08, 18, and 20	2.16 W
Device types 09 through 16 and 21 through 24	2.85 W
Device types 25 and 26	1.97 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC})	6.99°C/W 3/

1.4 Recommended operating conditions.

Positive supply voltage range (+5VA, +5VB):	
Device types 01 through 08 and 17 through 20	+4.5 V dc to +5.5 V dc
Device types 09 through 16 and 21 through 26	+4.75 V dc to +5.25 V dc
Negative supply voltage range (-VA, -VB):	
Device types 01, 03, 05, 07, 17, and 19	-14.25 V dc to -15.75 V dc
Device types 02, 04, 06, 08, 18, and 20	-11.40 V dc to -12.60 V dc
Logic supply voltage range (+5V logic)	+4.5 V dc to +5.5 V dc
Minimum logic high input voltage (V_{IH})	2.0 V dc
Maximum logic low input voltage (V_{IL})	0.8 V dc
Operating frequency (F_{OP})	12 MHz or 16 MHz
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Applies up to T_C = +125°C.
3/ Hottest die.
4/ Assumes 100 percent transmitter duty cycle on one channel and 0 percent duty cycle on the other channel.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1553 - Aircraft Internal Time Division Command/Response Multiplex Data Bus.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Pin functions. The pin functions shall be as specified in table III.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
+5 volt supply current, idle 1/	I_{CC1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V	1, 2, 3	01-08	5	190	mA
				09-16, 25, 26	5	200	
				17-20	5	250	
				21-24	5	260	
+5 volt supply current, channel A = 25% duty cycle, channel B = idle 1/	I_{CC2}		1, 2, 3	01-08	5	190	mA
				09-16, 25, 26	5	350	
				17-20	5	250	
				21-24	5	398	
+5 volt supply current, channel A = idle, channel B = 25% duty cycle 1/	I_{CC3}		1, 2, 3	01-08	5	190	mA
				09-16, 25, 26	5	350	
				17-20	5	250	
				21-24	5	398	
Negative supply 2/ current	I_{EE1}	$-V_A$ = -12 V for device types 02, 04, 06, 08, 18, and 20.	1, 2, 3	01-08, 17-20	5	60	mA
Negative supply current, channel A = 25% duty cycle, channel B = idle 2/	I_{EE2}	$-V_A$ = -15 V for device types 01, 03, 05, 07, 17, and 19.	1, 2, 3	01,03,05, 07,17,19	25	108	mA
				02,04,06, 08,18,20	25	120	
Negative supply current, channel B = 25% duty cycle, channel A = idle 2/	I_{EE3}		1, 2, 3	01,03,05, 07,17,19	25	108	mA
				02,04,06, 08,18,20	25	120	
Low level input 3/ current	I_{IL1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, V_{IN} = 0 V	1, 2, 3	All	-397	-50	µA
Low level input 4/ current	I_{IL2}				-794	-100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input 3/ current	I_{IH1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, V_{IN} = 2.4 V	1, 2, 3	All	-346	-42	µA
High level input 4/ current	I_{IH2}				-692	-84	
Output voltage low 5/	V_{OL1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, I_{OL} = -6.4 mA	1, 2, 3	All		0.4	V
Output voltage low 6/	V_{OL2}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, I_{OL} = -3.2 mA	1, 2, 3	All		0.4	V
Output voltage high 5/	V_{OH1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, I_{OH} = 6.4 mA	1, 2, 3	All	2.4		V
Output voltage high 6/	V_{OH2}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, I_{OH} = 3.2 mA	1, 2, 3	All	2.4		V
$\overline{IOEN}$ low pulse width (memory read)	t_{PW1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V	9, 10, 11	All	475	625	ns
$\overline{READYD}$ low pulse width (memory read)	t_{PW2}				225	375	ns
$\overline{MEMOE}$ low pulse width (memory read)	t_{PW3}				350	500	ns
$\overline{MEMWR}$ low pulse width (memory write)	t_{PW4}				37	87	ns
$\overline{MEMENA\text{-}OUT}$ low pulse width (memory read)	t_{PW5}				412	562	ns
$\overline{MEMENA\text{-}OUT}$ low pulse width (memory write)	t_{PW6}				435	695	ns
$\overline{INCMD}$ low pulse width (receive command)	t_{PW7}				45.5	47.5	µs
$\overline{INCMD}$ low pulse width (transmit command)	t_{PW8}				45.5	47.5	µs
$\overline{INT}$ low pulse width	t_{PW9}				450	550	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{DTREQ}}$ low pulse width	t_{PW10}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V	9, 10, 11	All	2.07	2.19	µs
$\overline{\text{DTACK}}$ low pulse width	t_{PW11}				2.0	2.23	µs
Functional tests		+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, see 4.3.1b	7, 8	All			Pass/ fail
Receiver threshold	V_{TH}	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, transformer coupled into a 70 Ω resistive load	4, 5, 6	All	500	700	mVp-p
Transmitter differential output voltage 7/	V_O	+5V logic = +5.5 V, +5VA = +5VB = +5.5 V, transformer coupled into a 70 Ω resistive load	4, 5, 6	All	18	27	Vp-p
Transmitter output rise time	t_R			All	100	300	ns
Transmitter output fall time	t_F			All	100	300	ns
Transmitter output offset voltage 8/	V_{OS}			All	-250	+250	mVp-p

1/ Measured at the following pins: Case outline T: pins 20, 37, and 72. Case outline U: pins A9, D3, and J3. Case outlines X, Y, and Z: pins 38, 54, and 68.
2/ Measured at the following pins: Case outlines X, Y, and Z: pins 36 and 70.
3/ Measured at the following pins: Device types 01 - 08, 10, 12, 14, 16 - 20, 22, and 24: pins 3-17, 19-26, 29-33, 39-44, 46-53, and 55-64. Device types 09, 11, 13, 15, 21, and 23: pins 3-17, 19-26, 29-33, 36, 39-44, 46-53, 55-64, and 70. Device types 25 and 26, case outline T: pins 1-4, 6, 8-12, 14, 15, 21-24, 27-31, 33-36, 38-55, 59-64, 66, and 68-71. Device types 25 and 26, case outline U: pins A1, A2, A5, A6, B1-B5, B7, B9, C2-C7, C9, D2, D7-D9, E1-E3, E7-E9, F1-F3, F7-F9, G2-G9, H5-H9, J1, J2, J4-J7, and J9.
4/ Measured at the following pin. Case outline T: pin 32. Case outline U: pin H2. Case outlines X, Y, and Z: pin 27.
5/ Measured at the following pins: Case outline T: pins 3, 4, 6, 8-12, 14, 15, 22-24, 27, 29, 36, 38, 39, 42-54, 66, and 68-71. Case outline U: pins A1, A2, B1-B3, B9, C2-C5, D2, D7-D9, E1-E3, E7-E9, F1-F3, F7-F9, G2-G6, H5, H9, J1, J2, and J4, J6. Case outlines X, Y, and Z: pins 8-17, 20-25, 29-32, 46-53, and 55-62.
6/ Measured at the following pins: Case outline T: pins 56, 57, and 58. Case outline U: pins A3, B8, and C8. Case outline X, Y, and Z: pins 28, 45, and 65-67.
7/ For device types 01, 03, 05, 17, 19:
In case outline X, the limits are 20 Vp-p minimum and 27 Vp-p maximum.
In case outlines Y and Z, the limits are 18 Vp-p minimum and 27 Vp-p maximum.
8/ Parameter shall be tested as part of the initial characterization of these devices and after design and process changes. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.

Case outline T.

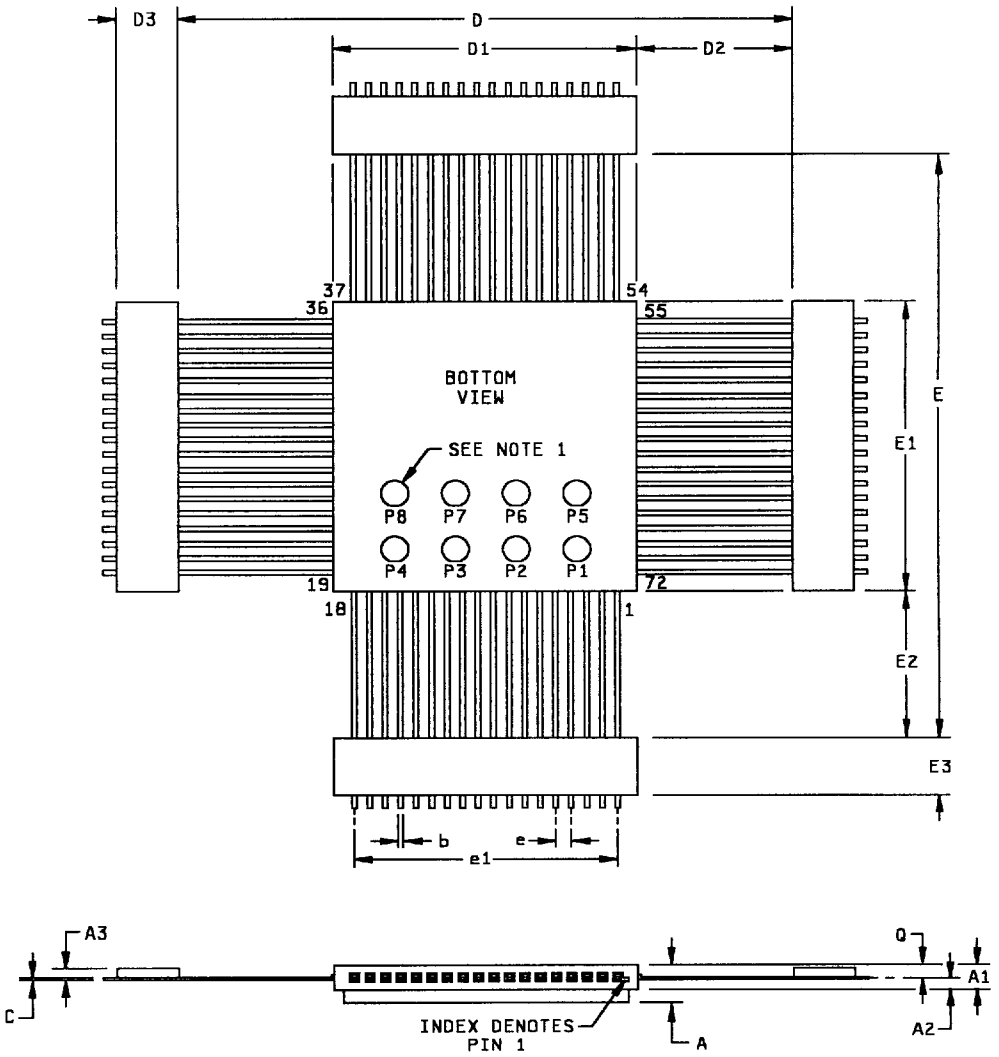


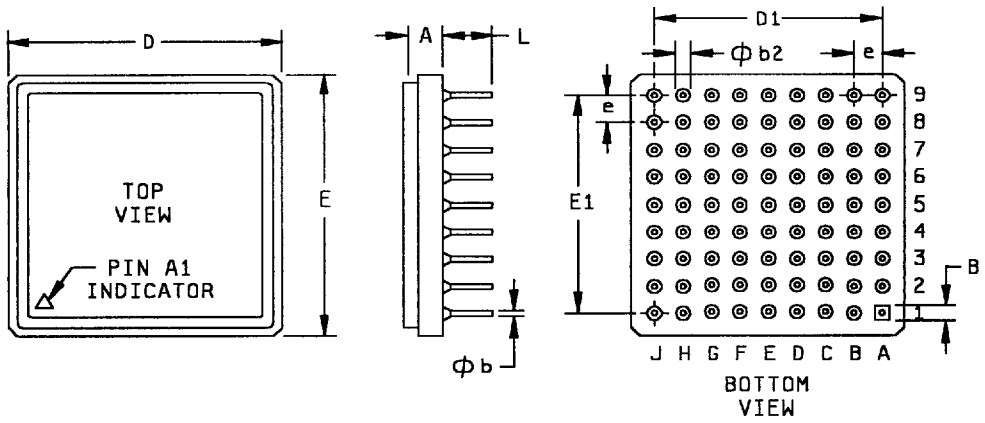
FIGURE 1. Case outline(s).

Symbol	Millimeter		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	3.94	---	0.155
A1	2.03	2.54	0.080	0.100
A2	1.14	1.40	0.045	0.055
A3	0.76	1.02	0.030	0.040
b	0.41	0.51	0.016	0.020
c	0.20	0.30	0.008	0.012
e	1.14	1.40	0.045	0.055
e1	18.35	25.40	0.842	0.858
D/E	50.42	51.18	1.985	2.015
D1/E1	25.15	25.65	0.990	1.010
D2/E2	12.19	13.21	0.480	0.520
D3/E3	4.95	5.21	0.195	0.205

NOTES:
1. There are eight test pads located on the bottom of the package. Each pad measures 0.100 inch (2.54 mm) in diameter. These pads are recessed so as to not interfere when mounting the package.
2. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. Package material is Alumina (AL_2O_3).

FIGURE 1. Case outline(s) - Continued.

Case outline U.



Symbol	Millimeter		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	3.94	---	0.155
B	1.61	1.91	0.065	0.075
øb	0.41	0.51	0.016	0.020
øb2	1.61	1.91	0.065	0.075
D/E	25.15	25.65	0.990	1.010
D1/E1	20.19	20.48	0.795	0.805
e	2.41	2.67	0.095	0.105
L	4.37	4.78	0.172	0.188

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Package material is Alumina (AL_2O_3).

FIGURE 1. Case outline(s) - Continued.

Case outline X.

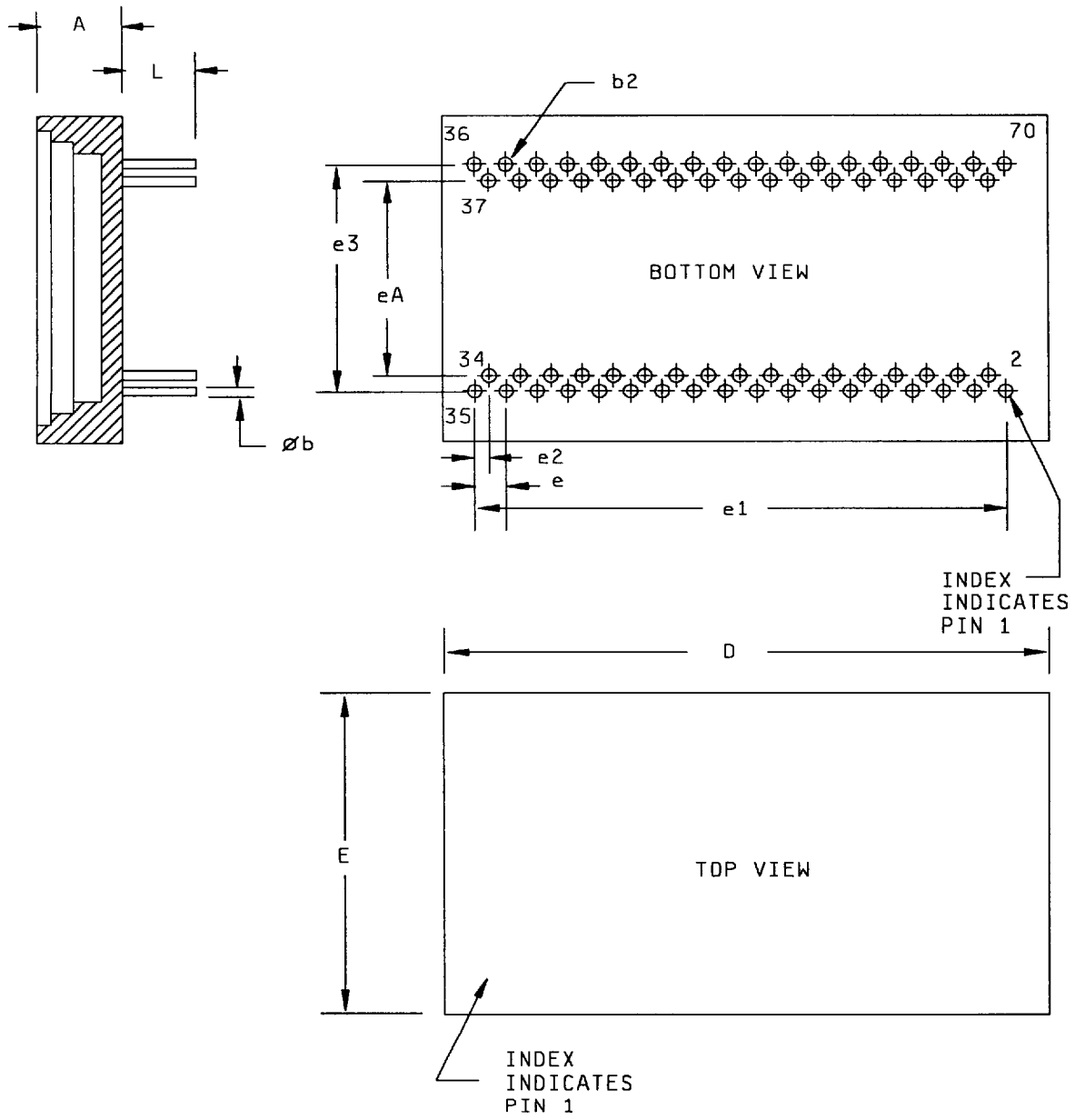


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeter		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	5.46	---	0.215
⌀b	0.406	0.508	0.016	0.020
b2	1.65	1.91	0.065	0.075
D	---	48.26	---	1.900
e	2.41	2.67	0.095	0.105
eA	10.03	10.29	0.395	0.405
e1	43.05	43.31	1.695	1.705
e2	1.14	1.40	0.045	0.055
e3	15.11	15.37	0.595	0.605
E	---	25.40	---	1.000
L	4.32	4.83	0.170	0.190

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline Y.

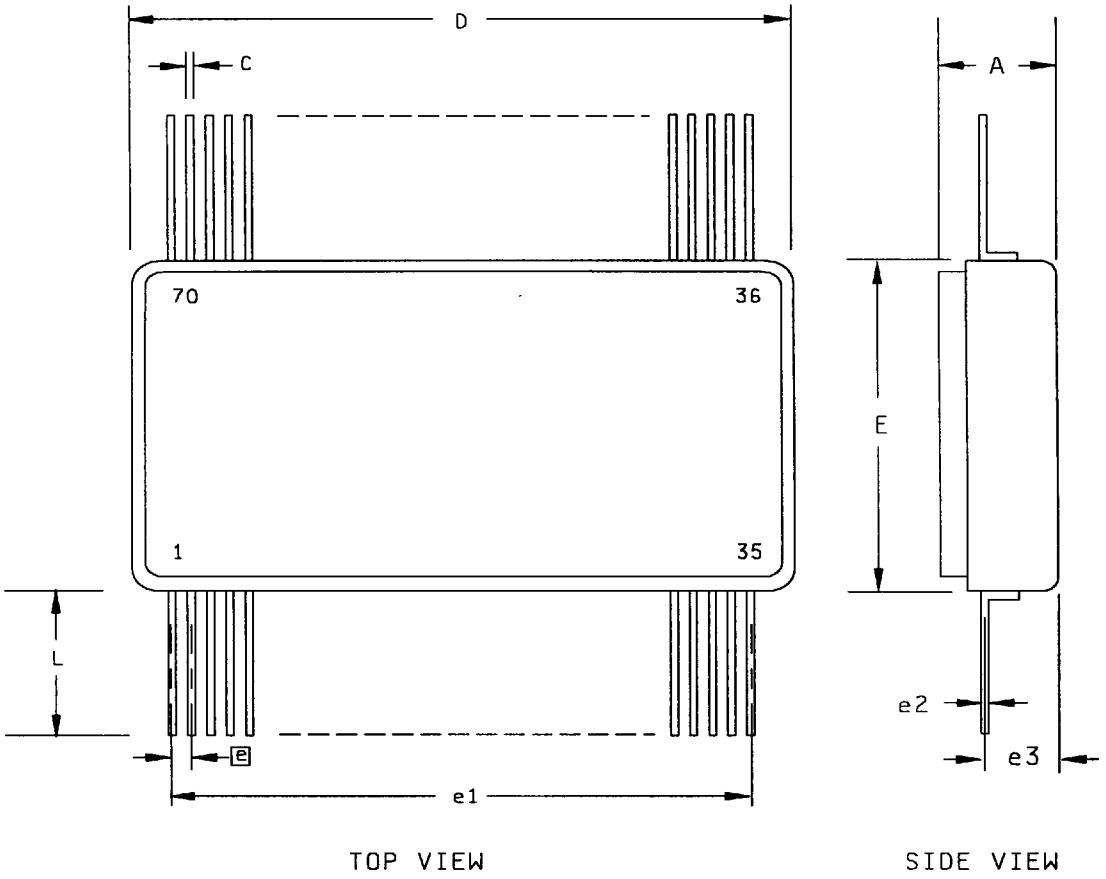


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeter		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	5.46	---	0.215
C	0.330	0.432	0.013	0.017
D	---	48.26	---	1.900
e	1.14	1.40	0.045	0.055
e1	43.05	43.31	1.695	1.705
e2	0.20	0.30	0.008	0.012
e3	1.52	2.03	0.060	0.080
E	---	25.40	---	1.000
L	10.16	---	0.400	---

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Case outline Z.

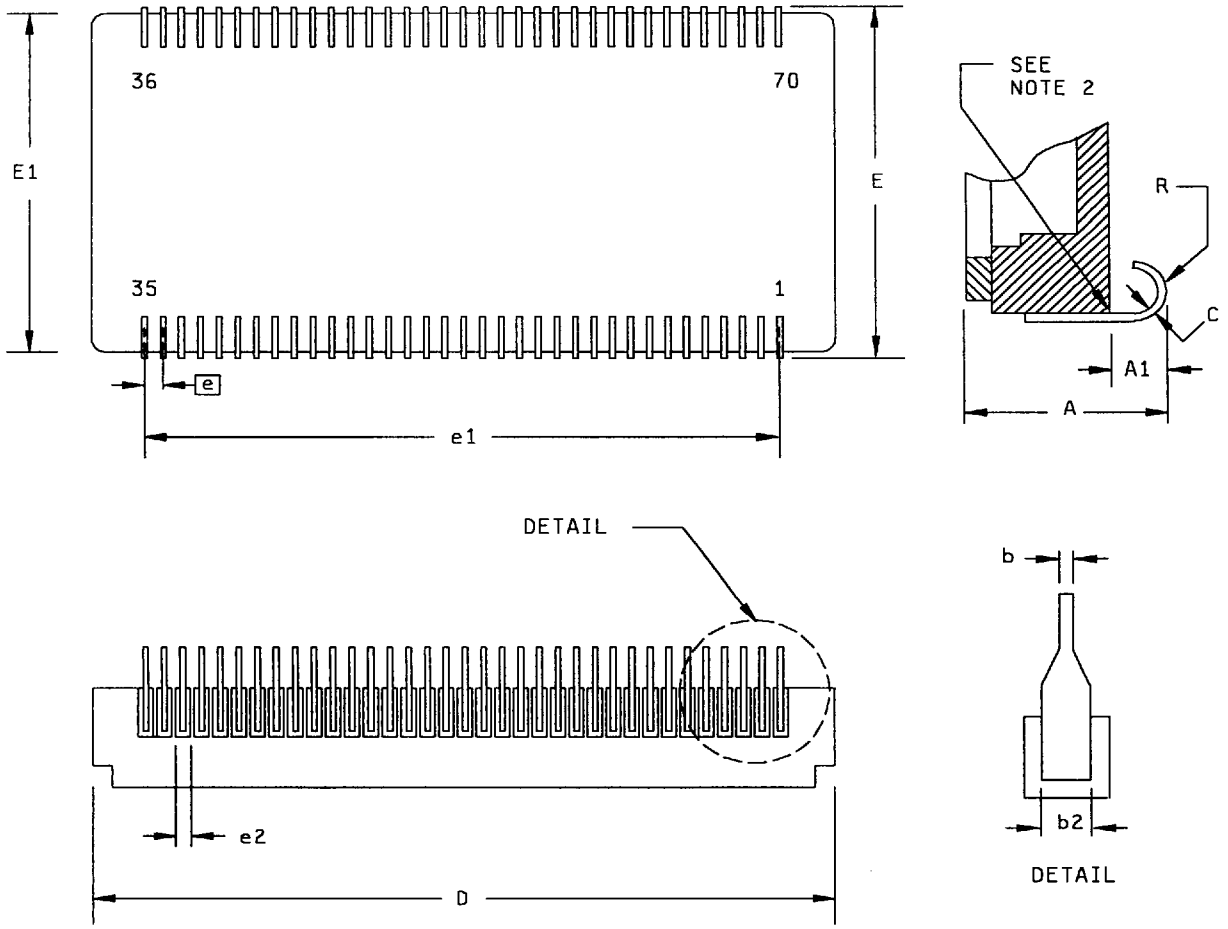


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeter		Inches	
	Minimum	Maximum	Minimum	Maximum
A	6.05	7.06	0.238	0.278
A1	1.52	1.93	0.060	0.076
b	0.38	0.48	0.015	0.019
b2	0.58	0.69	0.023	0.027
C	0.15	0.25	0.006	0.010
D	---	48.26	---	1.900
e	1.27 BSC		0.050 BSC	
e1	43.05	43.31	1.695	1.705
e2	0.84	1.09	0.033	0.043
E	---	25.98	---	1.023
E1	---	25.40	---	1.000
R	0.635	0.889	0.025	0.035

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Braze fillet shall be concave and is .020 ±.005 inches, (.508 ±.127 mm) at an angle of 45 degrees.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Device types	25 and 26		
Case outline	T		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	MEM/REG	37	+5 V LOGIC
2	MSTCLR	38	D01
3	A11	39	D04
4	A10	40	RTADP
5	TX/RX-A	41	RTADI
6	A08	42	D00
7	TX/RX-A	43	D02
8	A14	44	D03
9	A04	45	D05
10	A03	46	D08
11	A07	47	D07
12	A02	48	D13
13	TX/RX-B	49	D12
14	MEMOE/ADDR_LAT	50	D14
15	A00	51	D09
16	TX/RX-B	52	D11
17	LOGIC GND	53	D15
18	LOGIC GND	54	D10
19	LOGIC GND	55	TRANSPARENT/BUFFERED
20	+5 V LOGIC	56	READYD
21	RTAD2	57	INT
22	A06	58	IOEN
23	MEMWR/ZERO_WAIT	59	TX_INH_A
		60	TX_INH_B
24	DTREQ/16/8		
25	Test output (RX_B)	61	SELECT
		62	STRBD
26	Test output (RX_B)	63	RD/WR
27	A01	64	DTGRT/MSB/LSB
28	MENENA_IN/TRIGGER_SEL	65	Test output (RX-A)
29	DTACK/POLARITY_SEL	66	A15
30	CLOCK_IN	67	Test output (RX-A)
31	RT_AD_LAT	68	A05
		69	A09
32	SSFLAG/EXT_TRIG	70	A12
33	RTAD0	71	A13
34	TRAD3	72	+5 V LOGIC
35	RTAD4		
36	D06		

FIGURE 2. Terminal connections.

Device type	25 and 26		
Case outline	U		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	D10	E6	Test output (AB_Tstck)
A2	D11	E7	D08
A3	IOEN	E8	D06
A4	Test output (RX-A)	E9	D07
A5	RD/WR	F1	A06
A6	STRBD	F2	A03
A7	LOGIC GND	F3	A02
A8	LOGIC GND	F4	Test output(AB_Test2)
A9	+5 V LOGIC	F5	Test output(AB_Test3)
B1	A13	F6	Test output(B_Test1)
B2	D12	F7	D03
B3	A12	F8	D01
B4	MEM/REG	F9	D02
B5	MSTCLR	G1	TX/RX-B
B6	Test output (RX-A)	G2	A01
B7	TX_INH_A	G3	A00
		G4	MEMOE/ADDR_LAT
B8	READYD	G5	D05
B9	D09	G6	D04
C1	TX/RX-A	G7	RT_AD_LAT
C2	A11	G8	RTAD3
C3	A10	G9	RTADP
C4	A14	H1	TX/RX-B
C5	A15	H2	SSFLAG/EXT_TRIG
		H3	Test output (RX-B)
C6	SELECT	H4	Test output (RX-B)
C7	TX_INH_B	H5	DTREQ/16//8
		H6	CLOCK_IN
C8	INT	H7	RTAD0
C9	TRANPARENT/BUFFERED	H8	RTAD4
D1	TX/RX-A	H9	D00
D2	A08	J1	DTGRT/MSB/LSB
D3	+5 V LOGIC	J2	MEMWR/ZERO_WAIT
D4	Test output (A_RExt)	J3	+5 V LOGIC
D5	Test output (A_Test1)	J4	A09
D6	Test output (AB_Test4)	J5	MEMNA_IN/TRIGGER_SEL
D7	D13	J6	DTACK/POLARITY_SEL
D8	D15	J7	RTAD2
D9	D14	J8	LOGIC GND
E1	A07	J9	RTAD1
E2	A05		
E3	A04		
E4	Test output(B_RExt)		
E5	No connect		

FIGURE 2. Ternimal connections- Continued.

Device types	01 through 24		
Case outlines	X, Y, and Z		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	TX/RX-A	36	-VB (see note 1)
2	TX/RX-A	37	GNDB
3	SELECT	38	+5VB
4	STRBD	39	RTAD0
5	MEM/REG	40	RTAD1
6	RD/WR	41	RTAD2
7	MSTCLR	42	RTAD3
8	A15	43	RTAD4
9	A14	44	RTADP
10	A13	45	INCMD
11	A12	46	D00
12	A11	47	D01
13	A10	48	D02
14	A09	49	D03
15	A08	50	D04
16	A07	51	D05
17	A06	52	D06
18	LOGIC GND	53	D07
19	CLOCK_IN	54	+5 V LOGIC
20	A05	55	D08
21	A04	56	D09
22	A03	57	D10
23	A02	58	D11
24	A01	59	D12
25	A00	60	D13
26	DTGRT/MSB/LSB	61	D14
27	SSFLAG/EXT_TRIG	62	D15
28	MEMENA_OUT	63	TAG_CLK
29	MEMOE/ADDR_LAT	64	TRANSPARENT/BUFFERED
30	MEMWR/ZERO_WAIT	65	INT
31	DTREQ/16/8	66	READYD
32	DTACK/POLARITY_SEL	67	IOEN
33	MEMENA_IN/TRIGGER_SEL	68	+5VA
34	TX/RX-B	69	GNDA
35	TX/RX-B	70	-VA (see note 1)

NOTE:
1. For device types 01, 03, 05, 07, 17, and 19; pin 36 and pin 70 are -15 V.
   For device types 02, 04, 06, 08, 18, and 20; pin 36 and pin 70 are -12 V.
   For device types 09, 11, 13, 15, 21, and 23; pin 36 and pin 70 are no connects.
   For device types 10, 12, 14, 16, 22, and 24: pin 36 and pin 70 are TX_INH_B and TX_INH_A, respectively.

FIGURE 2. Terminal connections - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,2,3,4,5,6,7,8,9,10,11
Final electrical parameters	1*,2,3,4,5,6,7,8,9,10,11
Group A test requirements	1,2,3,4,5,6,7,8,9,10,11
Group C end-point electrical parameters	1,2,3,4,5,6,7,8,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendors test tape and shall be maintained and available from the aprroved source of supply.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

TABLE III. Pin functions.

Terminal symbol	I/O	Description
D00	I/O	Data bus bit 0 (LSB).
D02	I/O	Data bus bit 2.
D04	I/O	Data bus bit 4.
D06	I/O	Data bus bit 6.
D08	I/O	Data bus bit 8.
D10	I/O	Data bus bit 10.
D12	I/O	Data bus bit 12.
D14	I/O	Data bus bit 14.
RTAD1	I	Remote terminal address bit 1.
RTAD0	I	Remote terminal address bit 0 (LSB).
RTAD4	I	Remote terminal address bit 4 (MSB).
+5 V LOGIC or +5 V VCC	I	+5 V supply input for digital logic section.
TAG CLK	I	External Time Tag Clock Input, for BC/RT modes.
-VB	I	Input power supply connection for the B channel transceiver. -15 V for device types 01, 03, 05, and 07, -12 V for device types 02, 04, 06, and 08.
GNDB	-	Ground B. Power supply return connection for the B channel transceiver.
TX/RX-B	I/O	Transmit/receive transceiver-B. Input/output to the coupling transformer that connects to the B channel of the 1553 bus.
LOGIC GND	-	Logic ground. Power supply return for the digital logic section.
A01	I/O	Address bit 1.
A03	I/O	Address bit 3.
A05	I/O	Address bit 5.
A07	I/O	Address bit 7.
A09	I/O	Address bit 9.
A11	I/O	Address bit 11.
A13	I/O	Address bit 13.
A15	I/O	Address bit 15.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{MEMOE}}$/ADDR_LAT	O/I	Memory Output Enable/Address Latch. In transparent mode, used to enable data outputs for external RAM. In buffered mode, input used to configure the internal address buffers.
$\overline{\text{MEMENA-OUT}}$ 1/	O	Memory enable out. Logic 0 output enables external RAM. Used with $\overline{\text{MEMOE}}$ to read data or with MEMWR to write data into external RAM.
CLOCK IN	I	Clock input. 16 MHz TTL clock.
MEM/$\overline{\text{REG}}$	I	Memory/register. Input from CPU to select memory or register data transfer.
$\overline{\text{STRBD}}$	I	Strobe data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate a data transfer cycle to/from CPU.
TRANSPARENT/ BUFFERED	I	Used to select between the transparent and buffered modes for the host processor interface.
D11	I/O	Data bus bit 11.
D13	I/O	Data bus bit 13.
D15	I/O	Data bus bit 15 (MSB).
RTAD3	I	Remote terminal address bit 3.
RTAD2	I	Remote terminal address bit 2.
RTADP	I	Remote terminal address parity input.
RD/$\overline{\text{WR}}$	I	Read/write. Input from the CPU which defines the data bus transfer as a read or write operation.
GNDA	-	Ground A. Power supply return connection for the A channel transceiver.
-VA	I	Input power supply connection for the A channel transceiver. -15 V for device types 01, 03, 05, and 07, -12 V for device types 02, 04, 06, and 08.
TX/RX-A	I/O	Transmit receive transceiver-A. Input/output to the coupling transformer that connects to the A channel of the 1553 bus.
D01	I/O	Data bus bit 1.
D03	I/O	Data bus bit 3.
D05	I/O	Data bus bit 5.
D07	I/O	Data bus bit 7.
D09	I/O	Data bus bit 9.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
+5 VB	I	+5 V power supply connection for the B channel transceiver.
$\overline{\text{TX/RX-B}}$	I/O	Transmit/receive transceiver-B. Inverted I/O to coupling transformer that connects to channel B of the 1553 bus.
A00	I/O	Address bit 0 (LSB).
A02	I/O	Address bit 2.
A04	I/O	Address bit 4.
A06	I/O	Address bit 6.
A08	I/O	Address bit 8.
A10	I/O	Address bit 10.
A12	I/O	Address bit 12.
A14	I/O	Address bit 14.
$\overline{\text{MEMWR}}$/ZERO $\overline{\text{WAIT}}$	O/I	Memory write. Output pulse to write data into memory.
$\overline{\text{MEMENA-IN}}$/ TRIGGER SEL	I	Memory enable in. Enables internal RAM only; connect directly to MEMENA-OUT.
$\overline{\text{INCMD}}$ 1/	O	In command. Indicates BC to RTU currently in message transfer sequence.
$\overline{\text{MSTRCLR}}$	I	Master clear. Power-on reset from CPU.
$\overline{\text{INT}}$	O	Interrupt. Interrupt pulse line to CPU.
$\overline{\text{IOEN}}$	O	Input/output enable. Output to enable external buffers/latches connecting the hybrid to the address/data bus.
$\overline{\text{SELECT}}$	I	Select. Input from the CPU. When active selects device for operation.
$\overline{\text{READYD}}$	O	Ready data. When active indicates data has been received from, or is available to, the CPU.
+5 VA or +5 V VCC2	I	+5 V input power supply connection for the channel A transceiver.
$\overline{\text{TX/RX-A}}$	I/O	Transmit/receive transceiver-A. Inverted I/O to the coupling transformer that connects to channel A of the 1553 bus.
$\overline{\text{DTREQ}}$/16/$\overline{8}$	O/I	Data Transfer Request or 16 Bit/8 Bit Transfer Mode Select. In transparent mode,active low output signal used to request access to the ram interface bus (address,data, and control buses). In buffered mode, input signal used to select between the 16 bit data transfer mode (16/8 = Logic 1) and the 8 bit data transfer mode (16/8 = Logic 0).

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{SSFLAG}}$/EXT_TRIG	I	Sub System Flag/External Trigger Input. In the Remote Terminal mode, if this input is asserted low, the subsystem flag bit will be set in the device's RT Status Word. In the Bus Controller mode if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the Monitor mode if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a monitor trigger. This input has no effect in RT mode.
$\overline{\text{DTGRT}}$/MSB/LSB	I	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In $\overline{\text{DTGRT}}$ transparent mode, active low input signal asserted, in response to the $\overline{\text{DTREQ}}$ output, to indicate thatcontrol of the RAM interface bus has been granted to the BU-65170/61580. In buffered mode, input signal used to indicate which byte is currently begin transfered (MSB orLSB). The logic sense of MSB/LSB is controlled by the POLARITY SEL input. MSB/LSB is only used in the 8-bit buffered mode.
$\overline{\text{DTACK}}$/POLARITY_SEL	O/I	Data Transfer Acknowledge or Polarity Select. In transparent mode, active low output signal used to indicate acceptance of the ram interface bus in response to a data transfer grant ($\overline{\text{DTGRT}}$). In 16-bit buffered mode (TRANSPARENT/$\overline{\text{BUFFERED}}$ = LOGIC 0 AND 16/8 = LOGIC 1), input signal used to control the logic sense of the RD/$\overline{\text{WR}}$ signal. If POLARITY SEL is connected to logic 1, RD/$\overline{\text{WR}}$ should be asserted high (logic 1) for a read operation and low (logic 0) for a write operation. If POLARITY SEL is connected to logic 0, RD/$\overline{\text{WR}}$ should be asserted low (logic 0) for a read operation and high (logic 1) for a write operation. In 8-bit buffered mode (TRANSPARENT/$\overline{\text{BUFFERED}}$ = LOGIC 0 AND 16/8 = LOGIC 0), input signal used to control the logic sense of the MSB/LSB signal. If POLARITY SEL is is connected to logic 0, MSB/LSB should be asserted low (logic 0) to indicate the transfer of the least significant byte and high (logic 1) to indicate the transfer of the most significant byte. If POLARITY SEL is connected to logic 1, MSB/LSB should be asserted high (logic 1) to indicate the transfer of the least significant byte and low (logic 0) to indicate the transfer of the most significant byte.
$\overline{\text{MEMENA-IN}}$/ TRIGGER_SEL	I	Memory Enable Input or Trigger Select. In transparent mode, active low Chip Select ($\overline{\text{CS}}$) input to the 4K X 16 of internal shared RAM. If only internal RAM is used connect directly to $\overline{\text{MEMENA-OUT}}$. In buffered mode, input signal used to indicate the order in which byte pairs are transfered to or from the BU-65170/61580 by the host processor. This signal has no operation in the 16-bit buffered mode. In the 8-bit buffered mode, TRIGGER SEL should be asserted high (logic 1) if the byte oder for both read operations and write operations is MSB followed LSB. TRIGGER SEL should be asserted low (logic 0) if the byte oder for both read operations and write operations is LSB followed MSB.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{MEMWR}}$/ZERO_$\overline{\text{WAIT}}$	O/I	Memory Write or Zero Wait State. In transparent mode, active low output signal asserted low during memory write transfers to strobe data into internal or external RAM (normally connected to the WR signal on external ram chips). In buffered mode, input signal used to select between the zero wait state mode (ZEROWAIT = logic 0) and the non-zero wait state mode (ZEROWAIT = logic 1).
RT_AD_LATCH 2/	I	RT Address Latch. Input signal used to control the ACE internal RT Address Latch. A logic 0 configures the ACE to have a hardwired (transparent) RT address. A logic 1 configures the ACE to for the latched RT address mode. The value presented on the RTAD4, RTAD0, RTADP inputs is latched on the rising edge of RT_AD_LAT.
TX_INH_A, TX_INH_B 3/	I	The 1553 Channel A and /or Channel B transmitters may be inhibited by asserting the respective TX_INH input(s) high. Note that the ACE will fail its BC off self-test if the respective TX_INH input is logic 1.

1/ Not applicable to device types 25 and 26.
2/ Applicable to device types 25 and 26.
3/ Applicable to device types 10, 12, 14, 16, 22, 24, 25, and 26.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-09-11

Approved sources of supply for SMD 5962-93065 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9306501HXA	19645	BU-65170SI-140
5962-9306501HXC	19645	BU-65170SI-110
5962-9306501HYA	19645	BU-65170VI-140
5962-9306501HYC	19645	BU-65170VI-110
5962-9306501HZA	19645	BU-65170JI-140
5962-9306501HZC	19645	BU-65170JI-110
5962-9306502HXA	19645	BU-65170S2-140
5962-9306502HXC	19645	BU-65170S2-110
5962-9306502HYA	19645	BU-65170V2-140
5962-9306502HYC	19645	BU-65170V2-110
5962-9306502HZA	19645	BU-65170J2-140
5962-9306502HZC	19645	BU-65170J2-110
5962-9306503HXA	19645	BU-61580SI-140
5962-9306503HXC	19645	BU-61580SI-110
5962-9306503HYA	19645	BU-61580VI-140
5962-9306503HYC	19645	BU-61580VI-110
5962-9306503HZA	19645	BU-61580JI-140
5962-9306503HZC	19645	BU-61580JI-110
5962-9306504HXA	19645	BU-61580S2-140
5962-9306504HXC	19645	BU-61580S2-110
5962-9306504HYA	19645	BU-61580V2-140
5962-9306504HYC	19645	BU-61580V2-110
5962-9306504HZA	19645	BU-61580J2-140
5962-9306504HZC	19645	BU-61580J2-110
5962-9306505HXA	19645	BU-65171SI-140
5962-9306505HXC	19645	BU-65171SI-110
5962-9306505HYA	19645	BU-65171VI-140
5962-9306505HYC	19645	BU-65171VI-110
5962-9306505HZA	19645	BU-65171JI-140
5962-9306505HZC	19645	BU-65171JI-110

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9306506HXA	19645	BU-65171S2-140
5962-9306506HXA	19645	BU-65171S2-110
5962-9306506HYA	19645	BU-65171V2-140
5962-9306506HYC	19645	BU-65171V2-110
5962-9306506HZA	19645	BU-65171J2-140
5962-9306506HZC	19645	BU-65171J2-110
5962-9306507HXA	19645	BU-61581SI-140
5962-9306507HXA	19645	BU-61581SI-110
5962-9306507HYA	19645	BU-61581VI-140
5962-9306507HYC	19645	BU-61581VI-110
5962-9306507HZA	19645	BU-61581JI-140
5962-9306507HZC	19645	BU-61581JI-110
5962-9306508HXA	19645	BU-61581S2-140
5962-9306508HXA	19645	BU-61581S2-110
5962-9306508HYA	19645	BU-61581V2-140
5962-9306508HYC	19645	BU-61581V2-110
5962-9306508HZA	19645	BU-61581J2-140
5962-9306508HZC	19645	BU-61581J2-110
5962-9306509HXA	19645	BU-65170S3-140
5962-9306509HXA	19645	BU-65170S3-110
5962-9306509HYA	19645	BU-65170V3-140
5962-9306509HYC	19645	BU-65170V3-110
5962-9306510HXA	19645	BU-65170S6-140
5962-9306510HXA	19645	BU-65170S6-110
5962-9306510HYA	19645	BU-65170V6-140
5962-9306510HYC	19645	BU-65170V6-110
5962-9306511HXA	19645	BU-61580S3-140
5962-9306511HXA	19645	BU-61580S3-110
5962-9306511HYA	19645	BU-61580V3-140
5962-9306511HYC	19645	BU-61580V3-110

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9306512HXA	19645	BU-61580S6-140
5962-9306512HXC	19645	BU-61580S6-110
5962-9306512HYA	19645	BU-61580V6-140
5962-9306512HYC	19645	BU-61580V6-110
5962-9306513HXA	19645	BU-65171S3-140
5962-9306513HXC	19645	BU-65171S3-110
5962-9306513HYA	19645	BU-65171V3-140
5962-9306513HYC	19645	BU-65171V3-110
5962-9306514HXA	19645	BU-65171S6-140
5962-9306514HXC	19645	BU-65171S6-110
5962-9306514HYA	19645	BU-65171V6-140
5962-9306514HYC	19645	BU-65171V6-110
5962-9306515HXA	19645	BU-61581S3-140
5962-9306515HXC	19645	BU-61581S3-110
5962-9306515HYA	19645	BU-61581V3-140
5962-9306515HYC	19645	BU-61581V3-110
5962-9306516HXA	19645	BU-61581S6-140
5962-9306516HXC	19645	BU-61581S6-110
5962-9306516HYA	19645	BU-61581V6-140
5962-9306516HYC	19645	BU-61581V6-110
5962-9306517HXA	19645	BU-61585S1-140
5962-9306517HXC	19645	BU-61585S1-110
5962-9306517HYA	19645	BU-61585V1-140
5962-9306517HYC	19645	BU-61585V1-110
5962-9306518HXA	19645	BU-61585S2-140
5962-9306518HXC	19645	BU-61585S2-110
5962-9306518HYA	19645	BU-61585V2-140
5962-9306518HYC	19645	BU-61585V2-110
5962-9306519HXA	19645	BU-61586S1-140
5962-9306519HXC	19645	BU-61586S1-110
5962-9306519HYA	19645	BU-61586V1-140
5962-9306519HYC	19645	BU-61586V1-110

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9306520HXA	19645	BU-61586S2-140
5962-9306520HXC	19645	BU-61586S2-110
5962-9306520HYA	19645	BU-61586V2-140
5962-9306520HYC	19645	BU-61585V2-110
5962-9306521HXA	19645	BU-61585S3-140
5962-9306521HXC	19645	BU-61585S3-110
5962-9306521HYA	19645	BU-61585V3-140
5962-9306521HYC	19645	BU-61585V3-110
5962-9306522HXA	19645	BU-61585S6-140
5962-9306522HXC	19645	BU-61585S6-110
5962-9306522HYA	19645	BU-61585V6-140
5962-9306522HYC	19645	BU-61585V6-110
5962-9306523HXA	19645	BU-61586S3-140
5962-9306523HXC	19645	BU-61586S3-110
5962-9306523HYA	19645	BU-61586V3-140
5962-9306523HYC	19645	BU-61586V3-110
5962-9306524HXA	19645	BU-61586S6-140
5962-9306524HXC	19645	BU-61586S6-110
5962-9306524HYA	19645	BU-61586V6-140
5962-9306524HYC	19645	BU-61586V6-110
5962-9306525HTA	19645	BU-61588F3-140
5962-9306525HTC	19645	BU-61588F3-110
5962-9306525HUA	19645	BU-61588P3-140
5962-9306525HUC	19645	BU-61588P3-110
5962-9306526HTA	19645	BU-65178F3-140
5962-9306526HTC	19645	BU-65178F3-110
5962-9306526HUA	19645	BU-65178P3-140
5962-9306526HUC	19645	BU-65178P3-110

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
19645	ILC Data Device Corporation 105 Wilbur Place Bohemia, NY 11716-2482

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.