AUTO-SWITCHING POWER MULTIPLEXER

FEATURES

- Qualified for Automotive Applications
- Two-Input One-Output Power Multiplexer With Low $r_{DS(on)}$ Switch...84 mΩ (Typ)
- Reverse and Cross-Conduction Blocking
- Wide Operating Voltage Range...2.8 V to 5.5 V
- Low Standby Current...0.5 μA (Typ)
- Low Operating Current...55 μA (Typ)
- Adjustable Current Limit
- Controlled Output Voltage Transition Times Limit Inrush Current and Minimize Output Voltage Hold-Up Capacitance
- CMOS- and TTL-Compatible Control Inputs
- Manual and Auto-Switching Operating Modes
- Thermal Shutdown
- Available in TSSOP-8 (PW) Package

APPLICATIONS

- PCs
- PDAs
- Digital Cameras
- Modems
- Cell Phones
- Digital Radios
- MP3 Players

PW PACKAGE
(TOP VIEW)

DESCRIPTION/ORDERING INFORMATION

The TPS2115A power multiplexer enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8 V to 5.5 V and delivering up to 1 A. The TPS2115A includes extensive protection circuitry including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

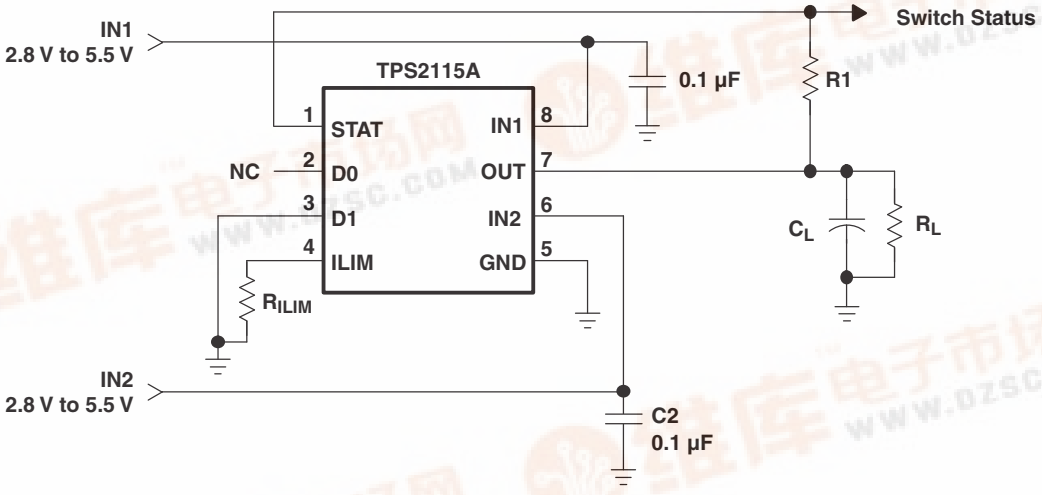


Figure 1. Typical Application

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Reel of 2000	TPS2115AIPWRQ1	2115AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

TRUTH TABLE

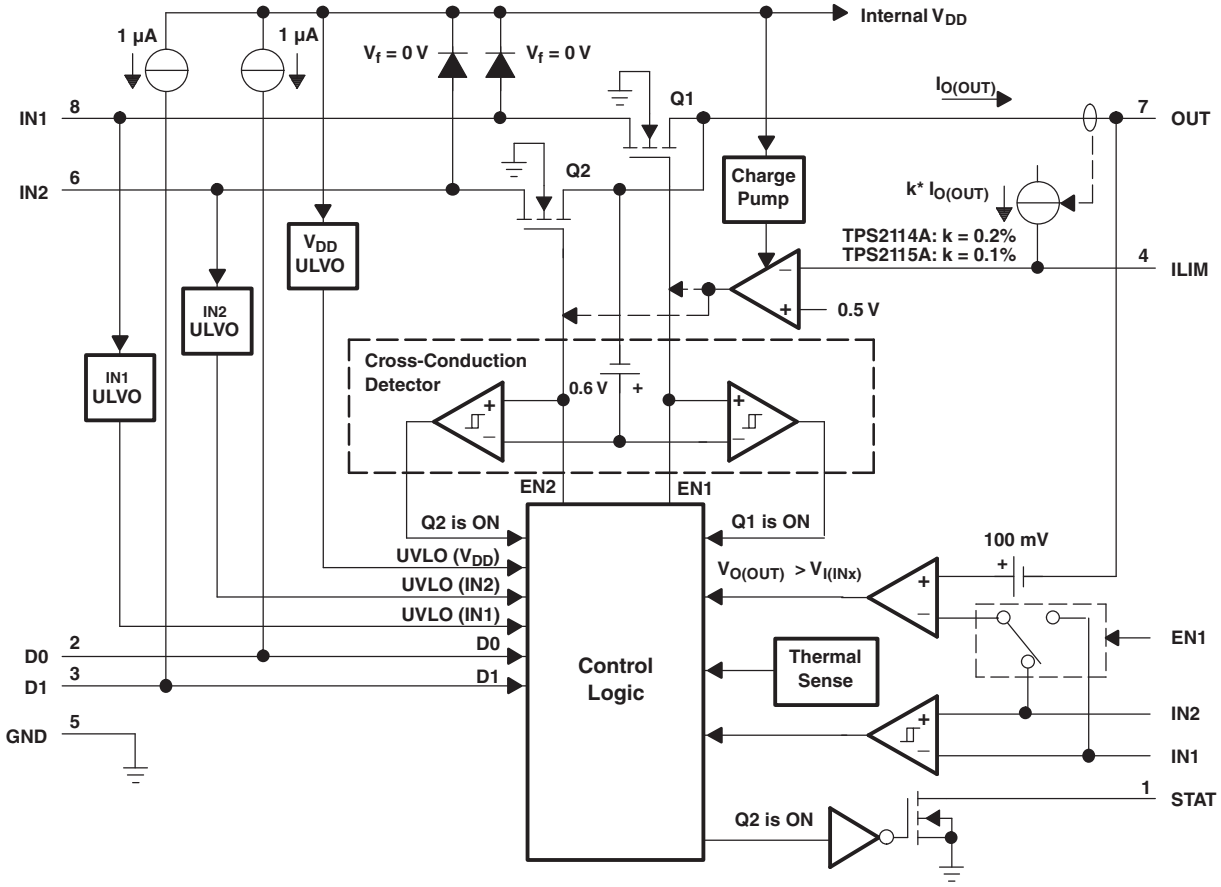
D0	D1	$V_{I(IN2)} > V_{I(IN1)}$(1)	STAT	OUT(2)
0	0	X	Hi-Z	IN2
0	1	No	0	IN1
0	1	Yes	Hi-Z	IN2
1	0	X	0	IN1
1	1	X	0	Hi-Z

(1) X = don't care
(2) The undervoltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal V_{DD} UVLO.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
D0	2	I	TTL- and CMOS-compatible input pins. Each pin has a 1-µA pullup. The *Truth Table* shows the functionality of D0 and D1.
D1	3	I	
GND	5	I	Ground
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
ILIM	4	I	A resistor R_{ILIM} from ILIM to GND sets the current limit I_L to $500/R_{ILIM}$.
OUT	7	O	Power switch output
STAT	1	O	Open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (i.e., EN is equal to logic 0).

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range unless otherwise noted

V_I	Input voltage range	IN1, IN2, D0, D1, ILIM	–0.3 V to 6 V
V_O	Output voltage range	OUT, STAT	–0.3 V to 6 V
$I_{O(sink)}$	Output sink current	STAT	5 mA
I_O	Continuous output current		1.5 mA
P_D	Continuous total power dissipation		See Dissipation Ratings
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating virtual-junction temperature range		–40°C to 125°C
T_{stg}	Storage temperature range		–65°C to 150°C
T_{lead}	Lead temperature soldering	1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

			MAX	UNIT
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	2000	V
		Charged-Device Model (CDM)	500	

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
TSSOP (PW)	3.9 mW/°C	387 mW	213 mW	155 mW

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
V_I	Input voltage	IN1	$V_{I(IN2)} \ge 2.8$ V	1.5	5.5	V
			$V_{I(IN2)} < 2.8$ V	2.8	5.5	
		IN2	$V_{I(IN1)} \ge 2.8$ V	1.5	5.5	
			$V_{I(IN1)} < 2.8$ V	2.8	5.5	
		D0, D1		0	5.5	
V_{IH}	High-level input voltage	D0, D1		2		V
V_{IL}	Low-level input voltage	D0, D1			0.7	V
I_O	Current limit adjustment range	OUT		0.63	1.25	A
T_A	Operating free-air temperature			–40	85	°C
T_J	Operating virtual-junction temperature range			–40	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{I(IN1)}$ = $V_{I(IN2)}$ = 5.5 V, R_{ILIM} = 400 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Switch (1)							
$r_{DS(on)}$	Drain-source on-state resistance (INx to OUT)	T_A = 25°C, I_L = 500 mA	$V_{I(IN1)}$ = $V_{I(IN2)}$ = 5.0 V		84	110	mΩ
			$V_{I(IN1)}$ = $V_{I(IN2)}$ = 3.3 V		84	110	
			$V_{I(IN1)}$ = $V_{I(IN2)}$ = 2.8 V		84	110	
		T_A = 85°C, I_L = 500 mA	$V_{I(IN1)}$ = $V_{I(IN2)}$ = 5.0 V			150	
			$V_{I(IN1)}$ = $V_{I(IN2)}$ = 3.3 V			150	
			$V_{I(IN1)}$ = $V_{I(IN2)}$ = 2.8 V			150	
Logic Inputs (D0 and D1)							
I_I	Input current at D0 or D1	D0 or D1 = high, sink current				1	µA
		D0 or D1 = low, source current		0.5	1.4	5	
Supply and Leakage Currents							
Supply current from IN1 (operating)		D1 = high, D0 = low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A			55	90	µA
		D1 = high, D0 = low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A			1	12	
		D0 = D1 = low (IN2 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A				75	
		D0 = D1 = low (IN2 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A				1	
Supply current from IN2 (operating)		D1 = high, D0 = low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A				1	µA
		D1 = high, D0 = low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A				75	
		D0 = D1 = low (IN2 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A			1	12	
		D0 = D1 = low (IN2 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A			55	90	
Quiescent current from IN1 (standby)		D0 = D1 = high (inactive), $I_{O(OUT)}$ = 0 A	$V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V		0.5	2	µA
			$V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V			1	
Quiescent current from IN2 (standby)		D0 = D1 = high (inactive), $I_{O(OUT)}$ = 0 A	$V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V			1	µA
			$V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V		0.5	2	
Forward leakage current from IN1 (measured from OUT to GND)		D0 = D1 = high (inactive), $V_{I(IN1)}$ = 5.5 V, IN2 open, $V_{O(OUT)}$ = 0 V (shorted), T_A = 25°C			0.1	5	µA
Forward leakage current from IN2 (measured from OUT to GND)		D0 = D1= high (inactive), $V_{I(IN2)}$ = 5.5 V, IN1 open, $V_{O(OUT)}$ = 0 V (shorted), T_A = 25°C			0.1	5	µA
Reverse leakage current to INx (measured from INx to GND)		D0 = D1 = high (inactive), $V_{I(INx)}$ = 0 V, $V_{O(OUT)}$ = 5.5 V, T_A = 25°C			0.3	5	µA
Current Limit Circuit							
	Current limit accuracy	R_{ILIM} = 400 Ω		0.95	1.25	1.56	A
		R_{ILIM} = 700 Ω		0.47	0.71	0.99	
t_d	Current limit settling time	Time for short-circuit output current to settle within 10% of its steady state value			1		ms
I_I	Input current at ILIM	$V_{I(ILIM)}$ = 0 V, $I_{O(OUT)}$ = 0 A		–15		0	µA
UVLO							
IN1 and IN2 UVLO		Falling edge		1.15	1.25		V
		Rising edge			1.30	1.35	
IN1 and IN2 UVLO hysteresis				30	57	65	mV
Internal VDD UVLO (the higher of IN1 and IN2)		Falling edge		2.4	2.53		V
		Rising edge			2.58	2.8	
Internal VDD UVLO hysteresis				30	50	75	mV
UVLO deglitch for IN1, IN2		Falling edge			110		µs
Reverse Conduction Blocking							
$\Delta V_{IO(blk)}$	Minimum input-to-output voltage difference to block switching	D0 = D1 = high, $V_{I(INx)}$ = 3.3 V. Connect OUT to a 5-V supply through a series 1-kΩ resistor. Set D0 = low. Slowly decrease the supply voltage until OUT connects to IN1.		80	100	120	mV

(1) The TPS2115A can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_{I(IN1)}$ = $V_{I(IN2)}$ = 5.5 V, R_{ILIM} = 400 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal Shutdown						
Thermal shutdown threshold		TPS2115A is in current limit.	135			°C
Recovery from thermal shutdown		TPS2115A is in current limit.	125			°C
Hysteresis				10		°C
IN2-IN1 Comparators						
Hysteresis of IN2-IN1 comparator			0.1		0.2	V
Deglitch of IN2-IN1 comparator (both ↑↓)			10	20	50	µs
STAT Output						
I_{leak}	Leakage current	$V_{O(STAT)}$ = 5.5 V		0.01	1	µA
V_{sat}	Saturation voltage	$I_{I(STAT)}$ = 2 mA, IN1 switch is on		0.13	0.4	V
t_d	Deglitch time (falling edge only)			150		µs

SWITCHING CHARACTERISTICS

over operating free-air temperature range, $V_{I(IN1)}$ = $V_{I(IN2)}$ = 5.5 V, R_{ILIM} = 400 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Switch							
t_r	Output rise time from an enable	$V_{I(IN1)}$ = $V_{I(IN2)}$ = 5 V	T_A = 25°C, C_L = 1 µF, I_L = 500 mA, See Figure 2(a)	1	1.8	3	ms
t_f	Output fall time from a disable	$V_{I(IN1)}$ = $V_{I(IN2)}$ = 5 V	T_A = 25°C, C_L = 1 µF, I_L = 500 mA, See Figure 2(a)	0.5	1	2	ms
t_t	Transition time	IN1 to IN2 transition, $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5 V	T_A = 85°C, C_L = 10 µF, I_L = 500 mA [Measure transition time as 10%-90% rise time or from 3.4 V to 4.8 V on $V_{O(OUT)}$], See Figure 2(b)		40	60	µs
		IN2 to IN1 transition, $V_{I(IN1)}$ = 5 V, $V_{I(IN2)}$ = 3.3 V			40	60	
t_{PLH1}	Turn-on propagation delay from enable	$V_{I(IN1)}$ = $V_{I(IN2)}$ = 5 V, Measured from enable to 10% of $V_{O(OUT)}$	T_A = 25°C, C_L = 10 µF, I_L = 500 mA, See Figure 2(a)		1		ms
t_{PHL1}	Turn-off propagation delay from a disable	$V_{I(IN1)}$ = $V_{I(IN2)}$ = 5 V, Measured from disable to 90% of $V_{O(OUT)}$	T_A = 25°C, C_L = 10 µF, I_L = 500 mA, See Figure 2(a)		5		ms
t_{PLH2}	Switch-over rising propagation delay	Logic 1 to Logic 0 transition on D1, $V_{I(IN1)}$ = 1.5 V, $V_{I(IN2)}$ = 5 V, $V_{I(D0)}$ = 0 V, Measured from D1 to 10% of $V_{O(OUT)}$	T_A = 25°C, C_L = 10 µF, I_L = 500 mA, See Figure 2(c)		40	100	µs
t_{PHL2}	Switch-over falling propagation delay	Logic 0 to Logic 1 transition on D1, $V_{I(IN1)}$ = 1.5 V, $V_{I(IN2)}$ = 5 V, $V_{I(D0)}$ = 0 V, Measured from D1 to 90% of $V_{O(OUT)}$	T_A = 25°C, C_L = 10 µF, I_L = 500 mA, See Figure 2(c)	2	5	10	ms

PARAMETER MEASUREMENT INFORMATION

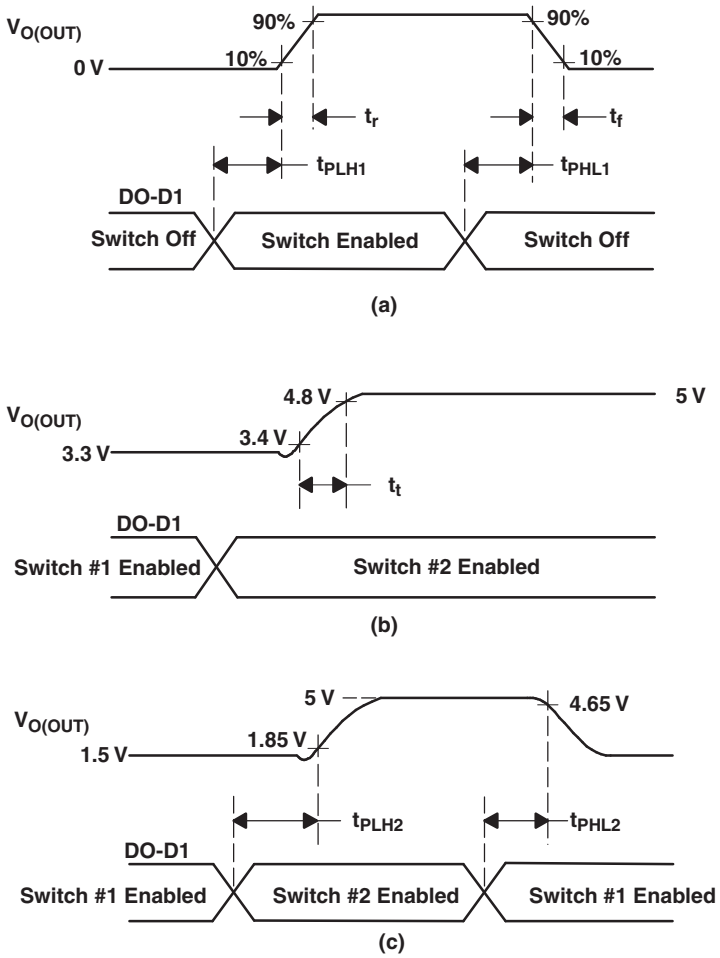
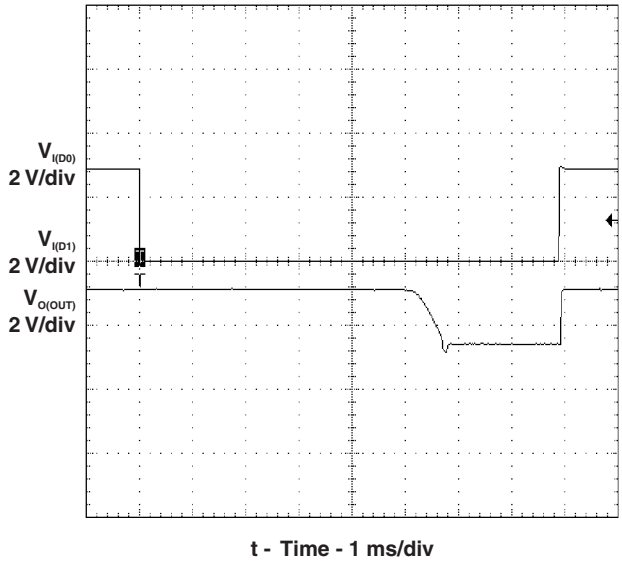
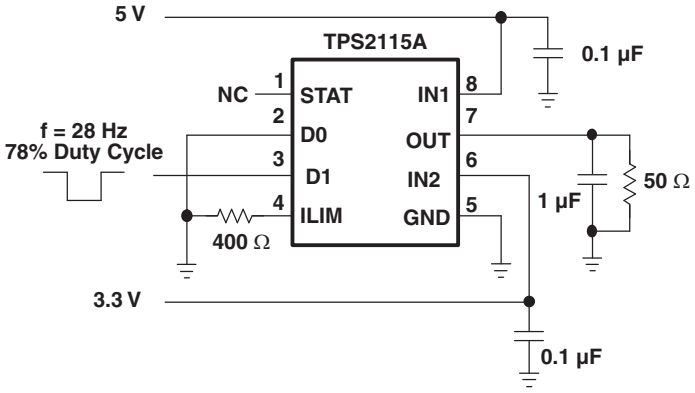


Figure 2. Propagation Delays and Transition Timing Waveforms

TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER RESPONSE

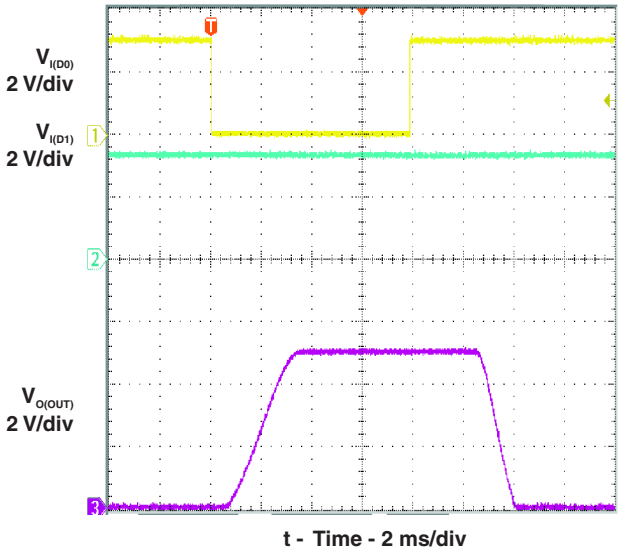


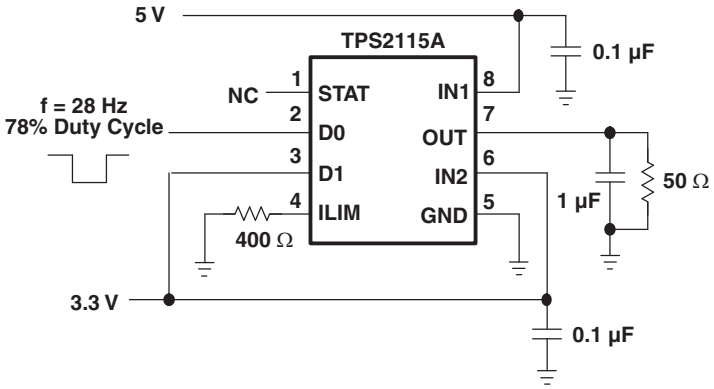


Output Switchover Response Test Circuit

Figure 3.

OUTPUT TURN-ON RESPONSE





Output Turn-On Response Test Circuit

Figure 4.

TYPICAL CHARACTERISTICS (continued)

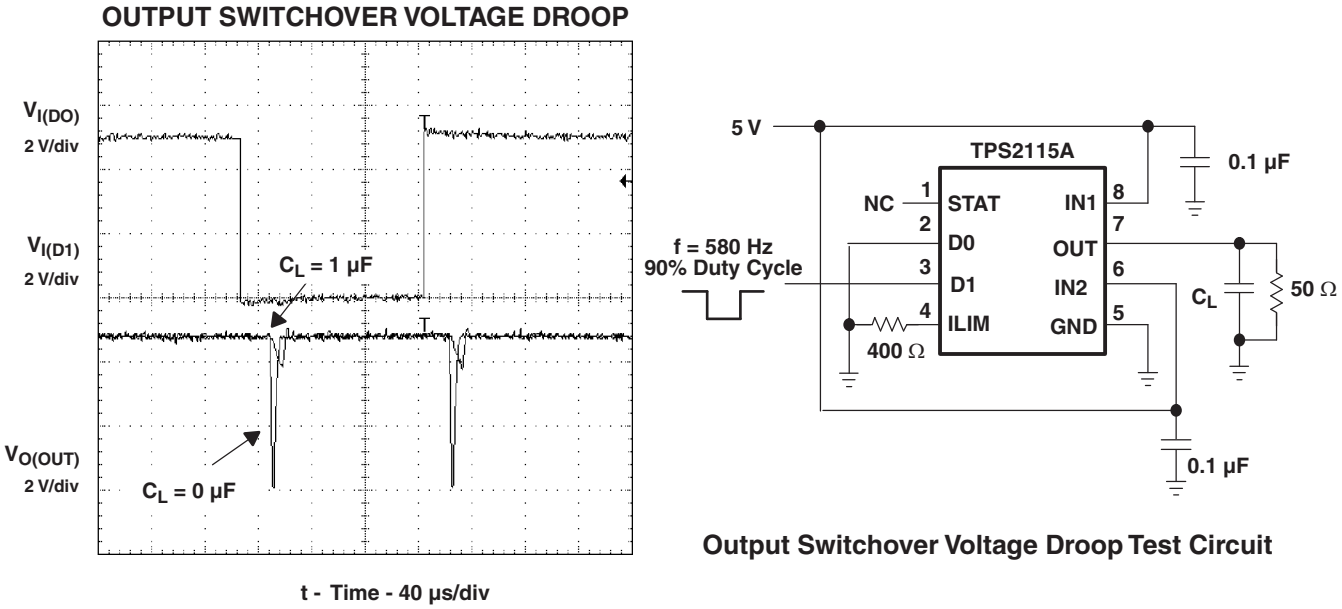
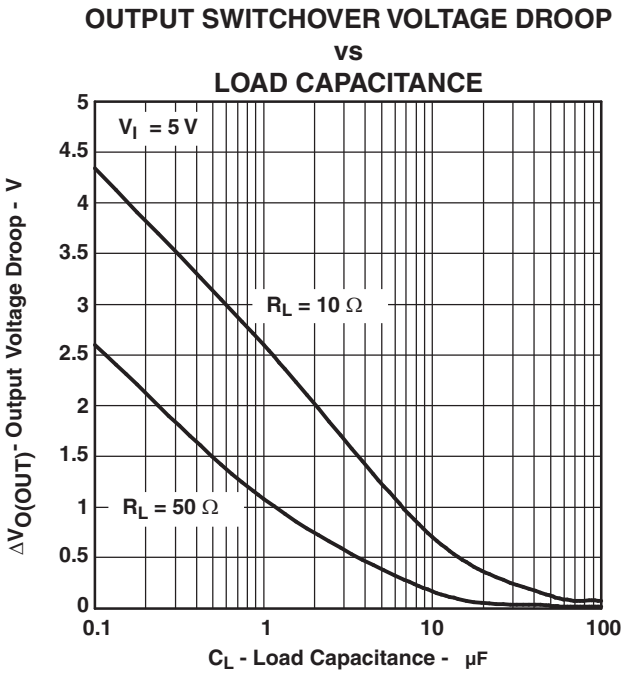
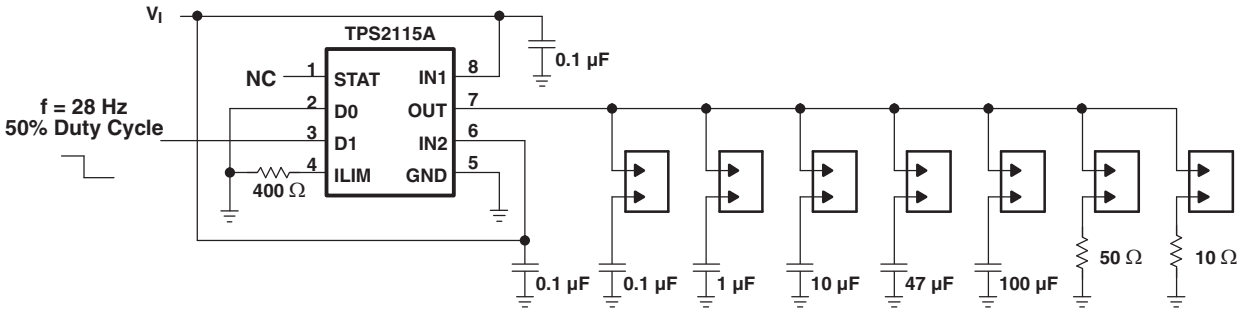


Figure 5.

TYPICAL CHARACTERISTICS (continued)



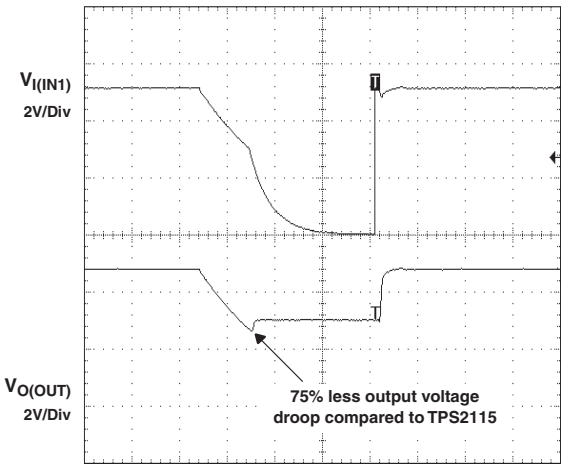


Output Switchover Voltage Droop Test Circuit

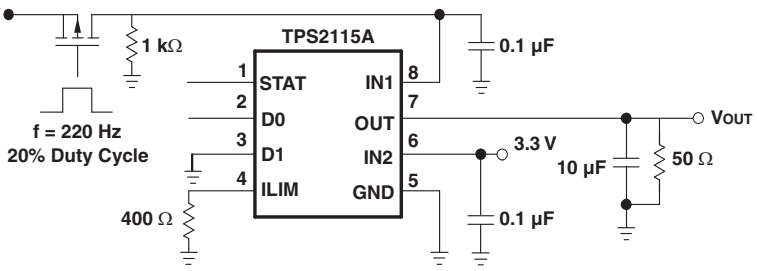
Figure 6.

TYPICAL CHARACTERISTICS (continued)

AUTO SWITCHOVER VOLTAGE DROOP



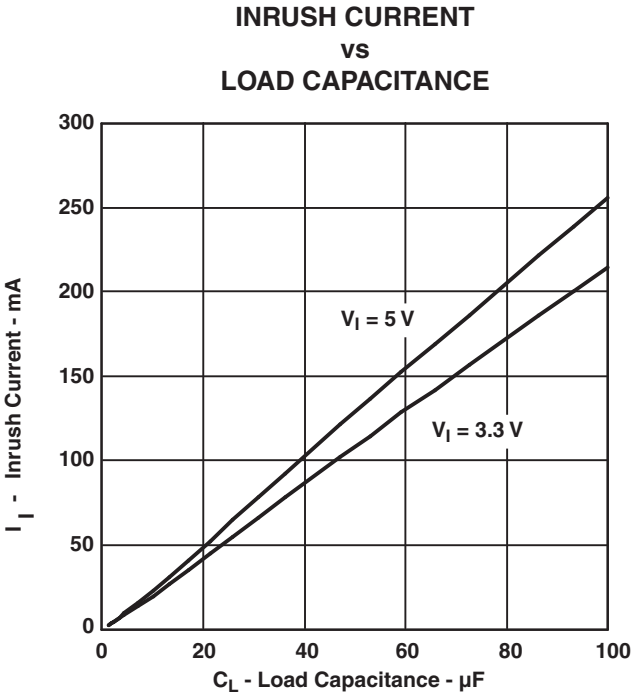
t - Time - 250 µs/div

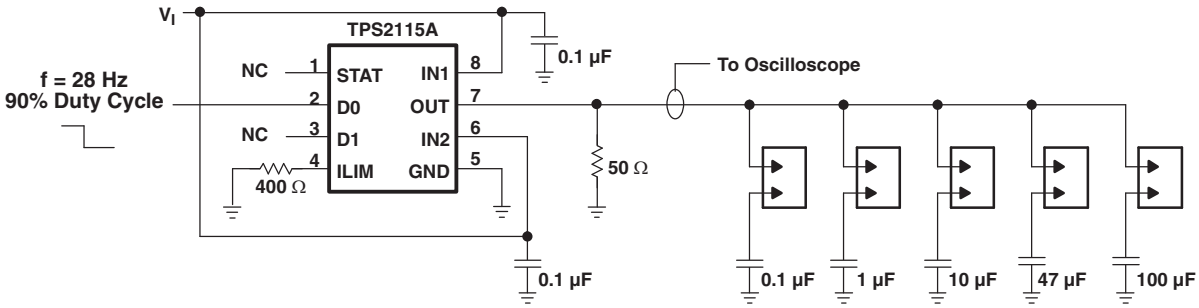


Auto Switchover Voltage Droop Test Circuit

Figure 7.

TYPICAL CHARACTERISTICS (continued)





Output Capacitor Inrush Current Test Circuit

Figure 8.

TYPICAL CHARACTERISTICS (continued)

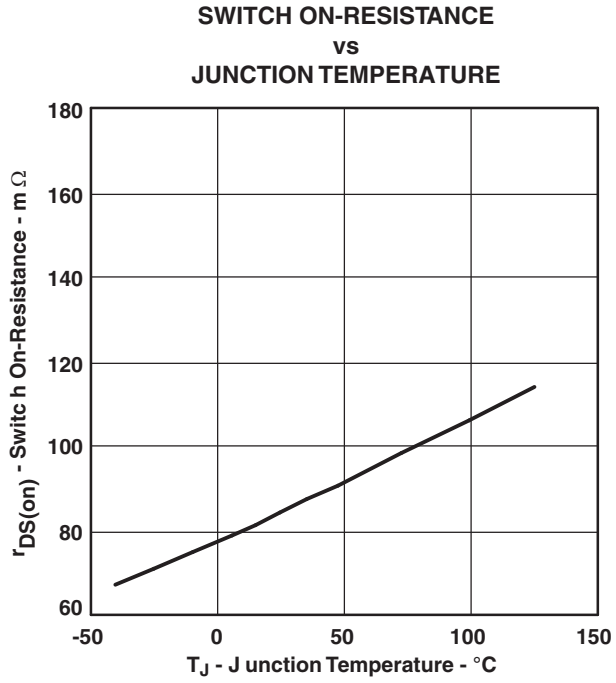


Figure 9.

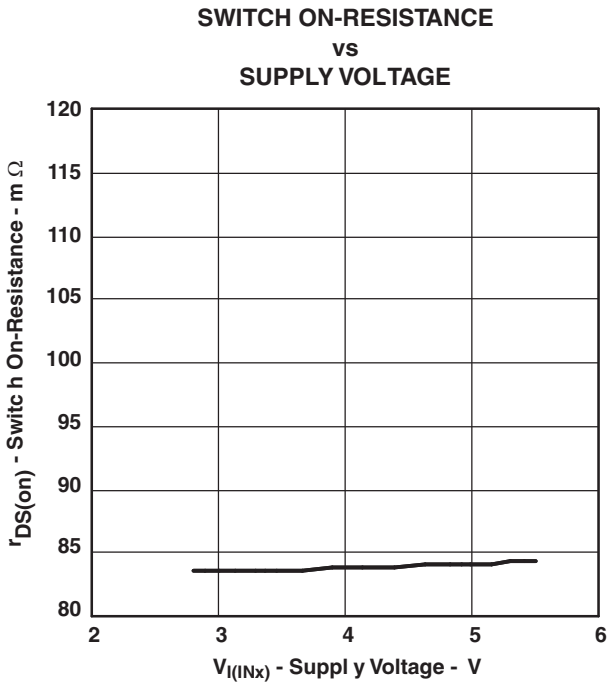


Figure 10.

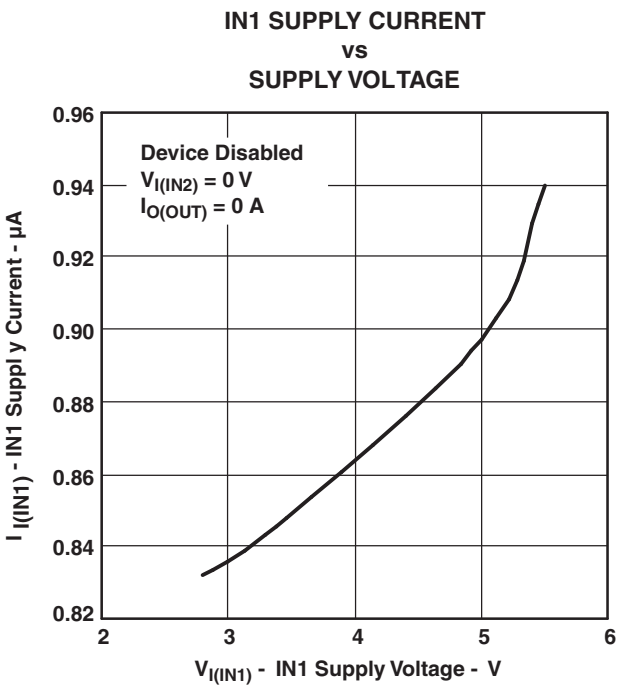


Figure 11.

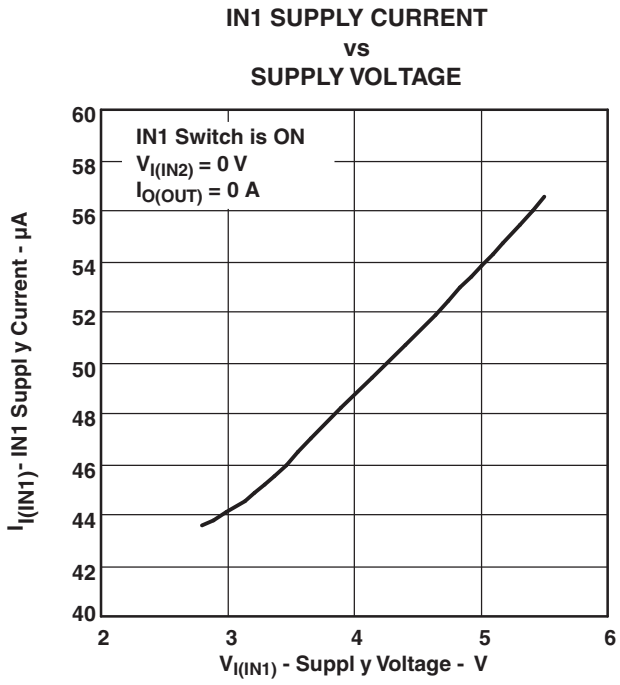


Figure 12.

TYPICAL CHARACTERISTICS (continued)

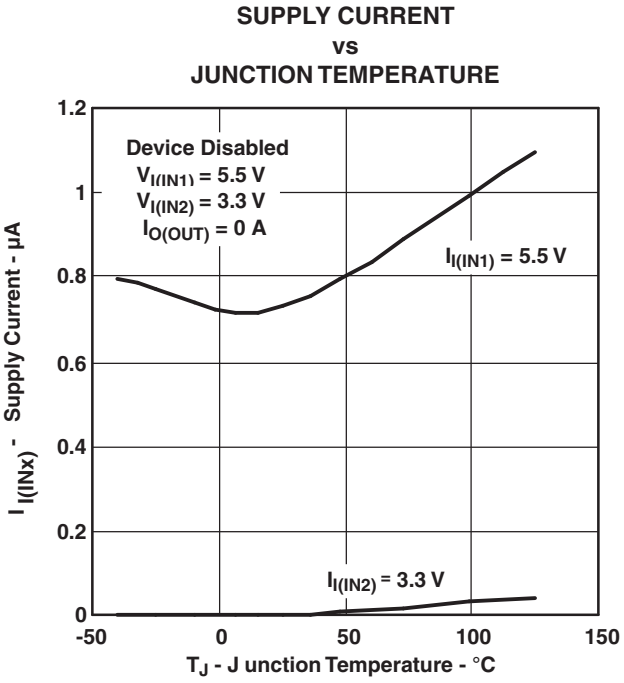


Figure 13.

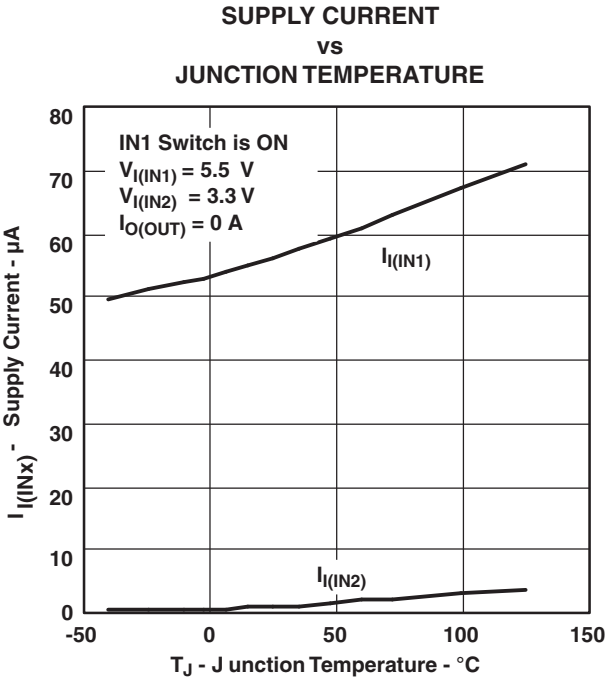


Figure 14.

APPLICATION INFORMATION

Some applications have two energy sources, one of which should be used in preference to another. Figure 15 shows a circuit that will connect IN1 to OUT until the voltage at IN1 falls below a user-specified value. Once the voltage on IN1 falls below this value, the TPS2115A will select the higher of the two supplies. This usually means that the TPS2115A will swap to IN2.

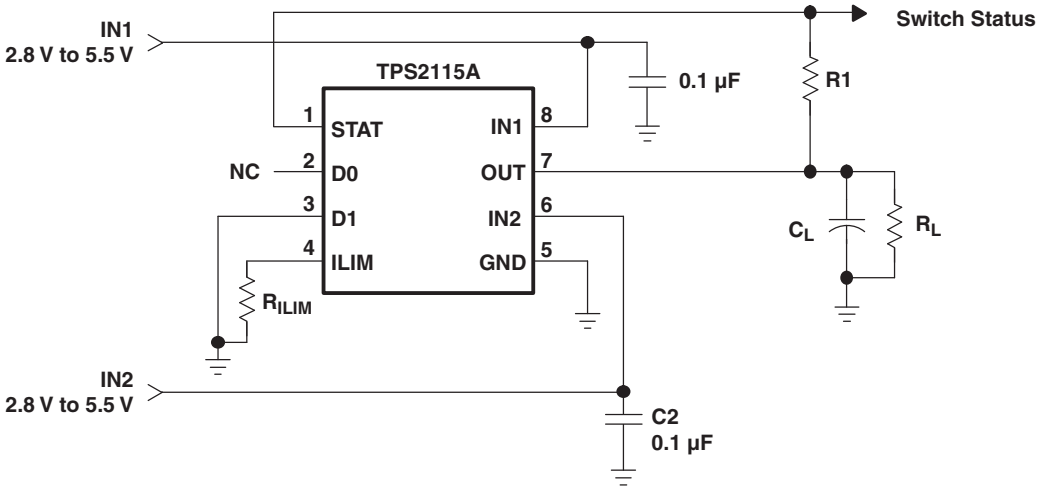


Figure 15. Auto-Selecting for a Dual Power Supply Application

In Figure 16, the multiplexer selects between two power supplies based upon the D1 logic signal. OUT connects to IN1 if D1 is logic 1; otherwise, OUT connects to IN2. The logic thresholds for the D1 terminal are compatible with both TTL and CMOS logic.

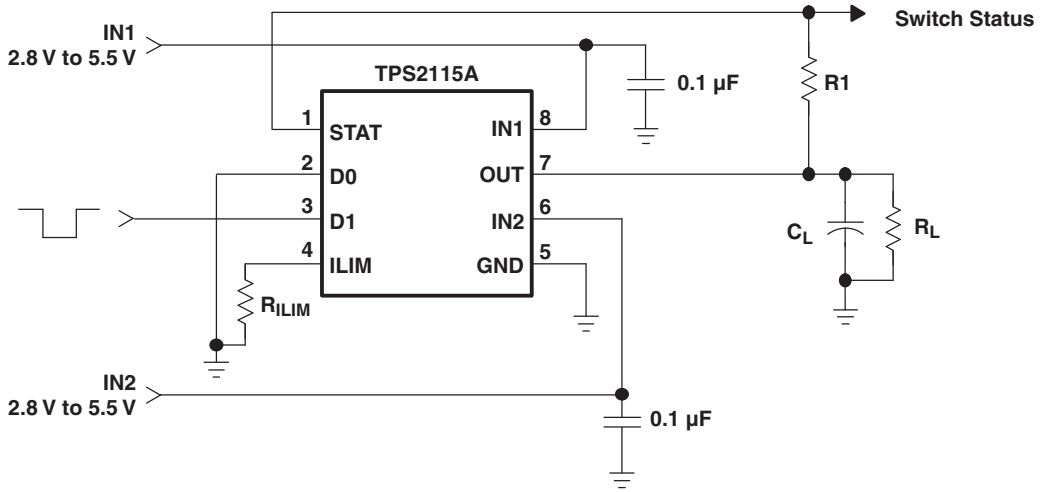


Figure 16. Manually Switching Power Sources

DETAILED DESCRIPTION

Auto-Switching Mode

D0 equal to logic 1 and D1 equal to logic 0 selects the auto-switching mode. In this mode, OUT connects to the higher of IN1 and IN2.

Manual Switching Mode

D0 equal to logic 0 selects the manual-switching mode. In this mode, OUT connects to IN1 if D1 is equal to logic 1, otherwise OUT connects to IN2.

N-Channel MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turn-on of a FET switch if the output voltage is greater than the input voltage.

Cross-Conduction Blocking

The switching circuitry ensures that both power switches will never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turn-on threshold voltage.

Reverse-Conduction Blocking

When the TPS2115A switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS2115A will not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it will remain connected regardless of output voltage.

Charge Pump

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

Current Limiting

A resistor R_{ILIM} from ILIM to GND sets the current limit to $500/R_{ILIM}$. Setting resistor R_{ILIM} equal to zero is not recommended as that disables current limiting.

Output Voltage Slew-Rate Control

The TPS2115A slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see *Truth Table*). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can glitch the voltage bus and cause a system to hang up or reset. It can also cause reliability issues such as pitting the connector power contacts when hot-plugging a load such as a PCI card. The TPS2115A slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS2115AIPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

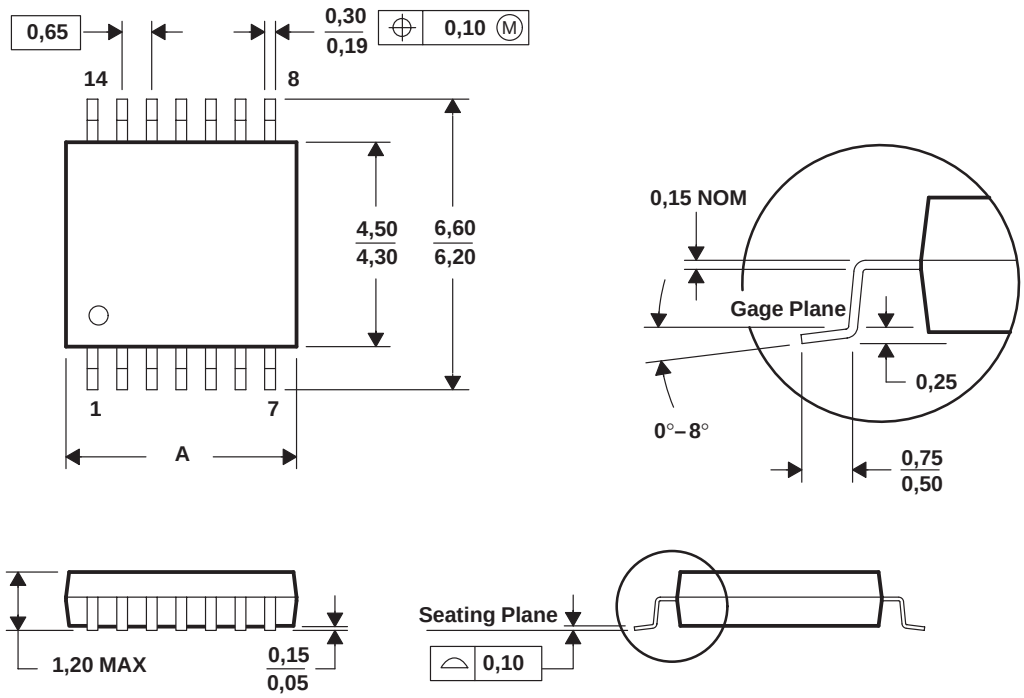
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF TPS2115A-Q1 :
- Catalog: TPS2115A

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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