

[查询"34702"供应商](#)

# 3.0 A Switch-Mode Power Supply with Linear Regulator

The 34702 provides the means to efficiently supply the Freescale Power QUICC™ I, II, and other families of Freescale microprocessors and DSPs. The 34702 incorporates a high-performance switching regulator, providing the direct supply for the microprocessor's core, and a low dropout (LDO) linear regulator control circuit providing the microprocessor I/O and bus voltage.

The switching regulator is a high-efficiency synchronous buck regulator with integrated N-channel power MOSFETs to provide protection features and to allow space-efficient, compact design.

The 34702 incorporates many advanced features; e.g., precisely maintained up/down power sequencing, ensuring the proper operation and protection of the CPU and power system.

## Features

- Operating Voltage from 2.8 V to 6.0 V
- High-Accuracy Output Voltages
- Fast Transient Response
- Switcher Output Current Up to 3.0 A
- Undervoltage Lockout and Overcurrent Protection
- Enable Inputs and Programmable Watchdog Timer
- Voltage Margining via I<sup>2</sup>C™ Bus
- Reset with Programmable Power-ON Delay
- Pb-Free Packaging Designated by Suffix Code EK

I<sup>2</sup>C is a trademark of Philips Corporation.

**34702**

**POWER SUPPLY  
INTEGRATED CIRCUIT**



ORDERING INFORMATION		
Device	Temperature Range (T <sub>A</sub> )	Package
MC34702EK/R2	-40 to 85°C	32 SOICW

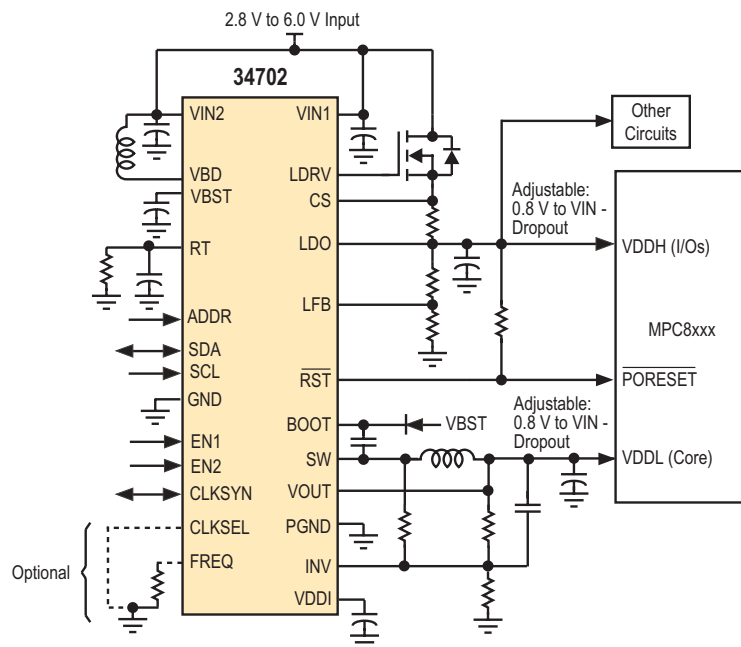


Figure 1. 34702 Simplified Application Diagram

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### INTERNAL BLOCK DIAGRAM

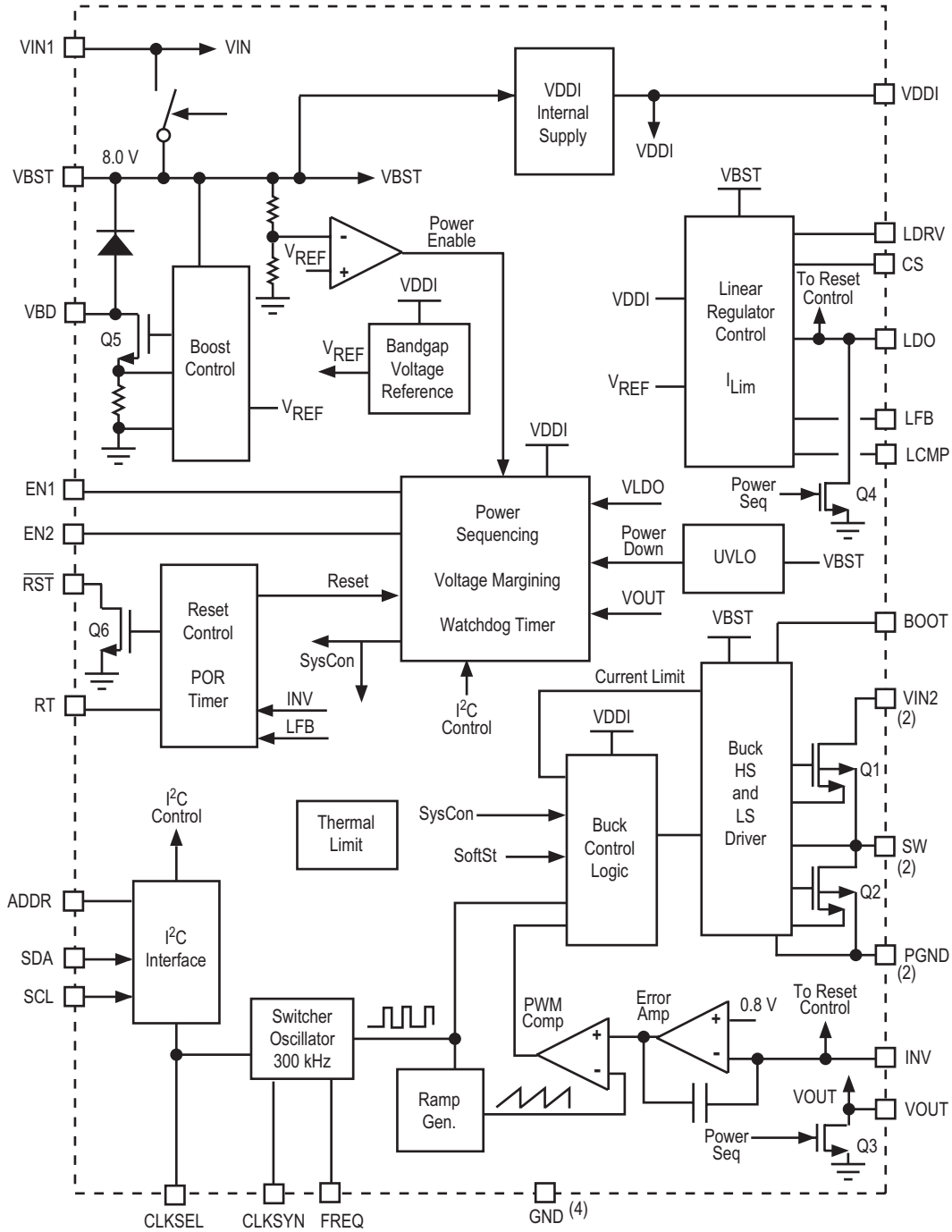
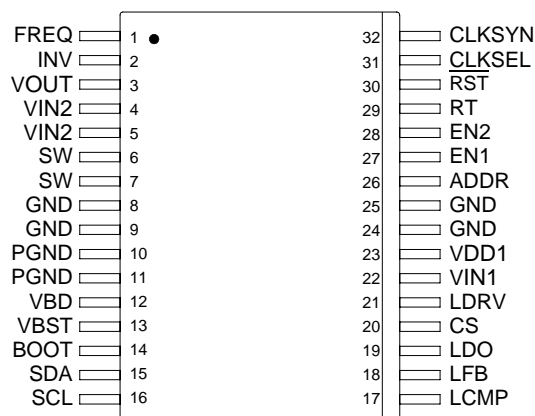


Figure 2. 34702 Simplified Internal Block Diagram

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## PIN CONNECTIONS



**Figure 3. Pin Connections**

**Table 1. Pin Function Description**

A functional description of each pin can be found in the [Functional Pin Description](#) section beginning on [page 16](#).

Pin	Pin Name	Formal Name	Definition
1	FREQ	Oscillator Frequency	This switcher frequency selection pin can be adjusted by connecting external resistor RF to the FREQ pin. The default switching frequency (FREQ pin left open or tied to VDDI) is set to 300 kHz.
2	INV	Inverting Input	Buck Controller Error Amplifier inverting input.
3	VOUT	Output Voltage	Output voltage of the buck converter. Input pin of the switching regulator power sequence control circuit.
4, 5	VIN2	Input Voltage 2	Buck regulator power input. Drain of the high-side power MOSFET.
6, 7	SW	Switch	Buck regulator switching node. This pin is connected to the inductor.
8, 9 24, 25	GND	Ground	Analog ground of the IC, thermal heatsinking.
10, 11	PGND	Power Ground	Buck regulator power ground.
12	VBD	Boost Drain	Drain of the internal boost regulator power MOSFET.
13	VBST	Boost Voltage	Internal boost regulator output voltage. The internal boost regulator provides a 20 mA output current to supply the drive circuits for the integrated power MOSFETs and the external N-channel power MOSFET of the linear regulator. The voltage at the VBST pin is 7.75V nominal.
14	BOOT	Bootstrap	Bootstrap capacitor input.
15	SDA	Serial Data	I <sup>2</sup> C bus pin. Serial data.
16	SCL	Serial Clock	I <sup>2</sup> C bus pin. Serial clock.
17	LCMP	Linear Compensation	Linear regulator compensation pin.
18	LFB	Linear Feedback	Linear regulator feedback pin.
19	LDO	Linear Regulator	Input pin of the linear regulator power sequence control circuit.

[查询"34702"供应商](#)**Table 1. Pin Function Description (continued)**

A functional description of each pin can be found in the [Functional Pin Description](#) section beginning on [page 16](#).

Pin	Pin Name	Formal Name	Definition
20	CS	Current Sense	Current sense pin of the LDO. Overcurrent protection of the linear regulator external power MOSFET. The voltage drop over the LDO current sense resistor RS is sensed between the CS and LDO pins. The LDO current limit can be adjusted by selecting the proper value of the current sensing resistor RS.
21	LDRV	Linear Drive	LDO gate drive of the external pass N-channel MOSFET.
22	VIN1	Input Voltage 1	The input supply pin for the integrated circuit. The internal circuits of the IC are supplied through this pin.
23	VDDI	Power Supply	Internal supply voltage. A ceramic low ESR 1uF 6V X5R or X7R capacitor is recommended.
26	ADDR	Address	I <sup>2</sup> C address selection. This pin can either be left open, tied to VDDI, or grounded through a 10 kΩ resistor.
27	EN1	Enable 1	Enable 1 Input. The combination of the logic state of the Enable 1 and Enable 2 inputs determines operation mode and type of power sequencing of the IC.
28	EN2	Enable 2	Enable 2 Input. The combination of the logic state of the Enable 1 and Enable 2 inputs determines operation mode and type of power sequencing of the IC.
29	RT	Reset Timer	This pin allows programming of the Power-ON Reset delay by means of an external RC network.
30	$\overline{\text{RST}}$	Reset Output (Active LOW)	The Reset Control circuit monitors both the switching regulator and the LDO feedback voltages. It is an open drain output and has to be pulled up to some supply voltage (e.g., the output of the LDO) by an external resistor.
31	CLKSEL	Clock Selection	This pin sets the CLKSYN pin as either an oscillator output or a synchronization input pin. The CLKSEL pin is also used for the I <sup>2</sup> C address selection.
32	CLKSYN	Clock Synchronization	Oscillator output/synchronization input pin.

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## ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

**Table 2. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
<b>ELECTRICAL RATINGS</b>			
Supply Voltage	$V_{IN1}, V_{IN2}$	-0.3 to 7.0	V
Switching Node Voltage	$V_{SW}$	-1.0 to 7.0	V
Buck Regulator Bootstrap Input Voltage (BOOT - SW)	$V_{IN(BOOT)}$	-0.3 to 8.5	V
Boost Regulator Output Voltage	$V_{BST}$	-0.3 to 8.5	V
Boost Regulator Drain Voltage	$V_{BD}$	-0.3 to 9.5	V
$\overline{RST}$ Drain Voltage	$V_{\overline{RST}}$	-0.3 to 7.0	V
Enable Pin Voltage at EN1, EN2	$V_{EN}$	-0.3 to 7.0	V
Logic Pin Voltage at SDA, SCL	$V_{LOG}$	-0.3 to 7.0	V
Analog Pin Voltage LDO, VOUT, $\overline{RST}$ LDRV, LCMP, CS	$V_{OUT}$ $V_{LIN}$	-0.3 to 7.0 -0.3 to 8.5	V
Pin Voltage at CLKSEL, ADDR, RT, FREQ, VDDI, CLKSYN, INV, LFB	$V_{LOGIC}$	-0.3 to 3.6	V
ESD Voltage <sup>(1)</sup> Human Body Model Machine Model	$V_{ESD}$	$\pm 2000$ $\pm 200$	V

## Notes

- ESD1 testing is performed in accordance with the Human Body Model (CZAP=100 pF, RZAP=1500  $\Omega$ ), ESD2 testing is performed in accordance with the Machine Model (CZAP=200 pF, RZAP=0  $\Omega$ ), and the Charge Device Model.

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**Table 2. Maximum Ratings (continued)**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
<b>THERMAL RATINGS</b>			
Storage Temperature	$T_{STG}$	-65 to 150	°C
Peak Package Reflow Temperature During Reflow <sup>(2), (3)</sup>	$T_{PPRT}$	Note 3	°C
Maximum Junction Temperature	$T_{JMAX}$	125	°C
Thermal Resistance	$R_{\theta JA}$		°C/W
Junction to Ambient (Single Layer) <sup>(4), (5)</sup>		70	
Junction to Ambient (Four Layers) <sup>(4), (5)</sup>		55	
Thermal Resistance, Junction to Base <sup>(6)</sup>	$R_{\theta JB}$	18	°C/W
Operational Package Temperature (Ambient Temperature)	$T_A$	-40 to 85	°C

Notes

- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescle's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics..
- Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board and board thermal resistance.
- Per JEDEC JESD51-6 with the board horizontal
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[查询"34702"供应商](#)**STATIC ELECTRICAL CHARACTERISTICS****Table 3. Static Electrical Characteristics**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figure 33](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>GENERAL</b>					
Operating Voltage Range ( $V_{IN1}$ , $V_{IN2}$ )	$V_{IN}$	2.8	–	6.0	V
Start-Up Voltage Threshold (Boost Switching)	$V_{ST}$	–	1.6	1.8	V
VBST Undervoltage Lockout (VBST rising)	$V_{BST\_UVLO}$	5.5	–	6.5	V
VBST Undervoltage Lockout Hysteresis	$V_{BST\_UVLO\_HYS}$	0.5	–	1.5	V
Input DC Supply Current (Normal Operation Mode, Enabled), Unloaded Outputs	$I_{IN}$	–	60	–	mA
$V_{IN1}$ Pin Input Supply Current ( $EN1 = EN2 = 0$ )	$I_{IN1}$	–	10	–	mA
$V_{IN2}$ Pin Input Leakage Current ( $EN1 = EN2 = 0$ )	$I_{IN2}$	–	100	–	$\mu\text{A}$
VDDI Internal Supply Voltage	$V_{DDI}$	2.9	–	3.3	V
VDDI Maximum Output Current (Externally Loaded)	$I_{DDI}$	–	–	-10	mA
<b>BUCK CONVERTER</b>					
Buck Converter Feedback Voltage (7), (8) I <sub>VOUT</sub> = 15 mA to 3.0 A. Includes Load Regulation Error	$V_{INV}$	0.784	0.800	0.816	V
Buck Converter Voltage Margining Step Size	$V_{MVO}$	–	1.0	–	%
Buck Converter Voltage Margining Highest Positive Value	$V_{MP}$	5.9	7.0	7.9	%
Buck Converter Voltage Margining Lowest Negative Value	$V_{MN}$	-7.9	7.0	-5.9	%
Buck Converter Line Regulation (7), (8) $V_{IN1} = V_{IN2} = 2.8\text{ V to }6.0\text{ V}$ , I <sub>VOUT</sub> = 15 mA to 3.0 A	$REG_{LNVO}$	-1.0	–	1.0	%
Buck Converter Load Regulation (7), (8) $V_{IN1} = V_{IN2} = 2.8\text{ V to }6.0\text{ V}$ , I <sub>VOUT</sub> = 15 mA to 3.0 A	$REG_{LDVO}$	-1.0	–	1.0	%
V <sub>OUT</sub> Input Leakage Current V <sub>OUT</sub> = 5.25 V	$I_{VOUTLK}$	–	3.5	–	mA
INV Input Leakage Current INV = 0.8 V	$INV_{LEAK}$	-1.0	–	1.0	$\mu\text{A}$

**Notes**

7. Design information only. This parameter is not production tested.
8. V<sub>OUT</sub> refers to load current on output switcher.

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**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figure 33](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>BUCK CONVERTER (CONTINUED)</b>					
High-Side Power MOSFET Q1 $R_{DS(ON)}$ <sup>(9),(10)</sup> ID = 500 mA, $T_A = 25^{\circ}\text{C}$ , $V_{BST} = 8.0\text{ V}$	$R_{DS(ON)}$	–	60	–	m $\Omega$
Low-Side Power MOSFET Q2 $R_{DS(ON)}$ <sup>(9),(10)</sup> ID = 500 mA, $T_A = 25^{\circ}\text{C}$ , $V_{BST} = 8.0\text{ V}$	$R_{DS(ON)}$	–	65	–	m $\Omega$
Buck Converter Peak Current Limit (High Level)	$I_{LIMH}$	-7.0	-4.7	-4.0	A
VOUT Pull-down MOSFET Q3 Current Limit $T_A = 25^{\circ}\text{C}$ , $V_{BST} = 8.0\text{ V}$	$I_{M3\_LIM}$	0.75	–	2.0	A
VOUT Pull-down MOSFET Q3 $R_{DS(ON)}$ <sup>(10)</sup> ID = 1.0 A, $V_{BST} = 8.0\text{ V}$	$R_{DS(ON)}$	–	–	1.9	$\Omega$
Thermal Shutdown (VOUT Pull-down MOSFET Q3) <sup>(9)</sup>	$T_{SD}$	150	170	190	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis <sup>(9)</sup>	$T_{SDHYS}$	–	10	–	$^{\circ}\text{C}$

Notes

9. Design information only. This parameter is not production tested.
10. ID refers to the MOSFET drain current



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**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figure 33](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ERROR AMPLIFIER (BUCK CONVERTER)</b>					
Input Impedance <sup>(11)</sup>	$R_{OUT}$	–	150	–	$\Omega$
Output Impedance <sup>(11)</sup>	AVOL	–	80	–	dB
DC Open Loop Gain <sup>(11)</sup>	GBW	–	35	–	MHz
Gain Bandwidth Product <sup>(11)</sup>	SR	–	200	–	V/ $\mu\text{s}$
Slew Rate <sup>(11)</sup>	$V_{EA\_OH}$	–	2.0	–	V
Output Voltage – High Level VIN1 > 3.3 V, IOEA = -1.0 mA <sup>(11), (12)</sup>	$V_{EA\_OL}$	–	0.4	–	V
Output Voltage – Low Level IOEA = -1.0 mA <sup>(11), (12)</sup>	$V_{SCRamp}$	–	0.5	–	V
Oscillator Ramp <sup>(11)</sup>	$V_{SCRamp}$	–	0.5	–	V

**OSCILLATOR**

CLKSYN Pin (open) Low Level Output Voltage IOL = +1.0 mA <sup>(13)</sup>	$V_{OSC\_OL}$	–	–	0.4	V
CLKSYN Pin (open) High Level Output Voltage IOH = -1.0 mA <sup>(14)</sup>	$V_{OSC\_OH}$	VDDI -0.4 V	–	–	V
CLKSYN Pin (grounded) Input Voltage Threshold	$V_{OSC\_IH}$	1.2	–	2.0	V
CLKSYN Pin Pullup Resistance	RPU	60	–	240	k $\Omega$
Frequency Adjusting Reference Voltage	$V_{FREQ}$	–	1.26	–	V

**BOOST REGULATOR**

Regulator Output Voltage IBST = 20 mA, VIN1 = VIN2 = 2.8 V to 6.0 V	$V_{BST}$	7.3	7.7	8.3	V
Power MOSFET Q5 RDS(ON) <sup>(11)</sup> IBD = 500 mA, TA = 25°C	$R_{DS(ON)}$	–	650	1000	m $\Omega$
Regulator Recommended Output Capacitor	CBST	–	10	–	$\mu\text{F}$
Regulator Recommended Output Capacitor Maximum ESR	ESRCBST	–	100	–	m $\Omega$

Notes

11. Design information only. This parameter is not production tested.
12. IOEA Refers to Error Amplifier Output Current.
13. IOL Refers to IO Low Level Threshold Voltage Current
14. IOH Refers to IO High Level Threshold Voltage Current

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**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figure 33](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>LINEAR REGULATOR (LDO)</b>					
LDO Feedback Voltage <sup>(16)</sup> VIN1 = VIN2 = 2.8 V to 6.0 V, ILDO = 10 mA to 1000 mA. Includes Load Regulation Error	V <sub>LFB</sub>	0.784	0.800	0.816	V
LDO Voltage Margining Step Size	V <sub>MLDO</sub>	–	1.0	–	%
LDO Voltage Margining Highest Positive Value	V <sub>MP</sub>	5.9	7.0	7.9	%
LDO Voltage Margining Lowest Negative Value	V <sub>MN</sub>	-7.9	7.0	-5.9	%
LDO Line Regulation <sup>(16)</sup> VIN1 = VIN2 = 2.8 V to 6.0 V, ILDO = 1000 mA	REG <sub>LNVLDO</sub>	-1.0	–	1.0	%
LDO Load Regulation <sup>(16)</sup> ILDO = 10 mA to 1000 mA	REG <sub>LDVLD0</sub>	-1.0	–	1.0	%
LDO Ripple Rejection, Dropout Voltage <sup>(16)</sup> VDO = 1.0 V, VRIPPLE = +1.0 V p-p Sinusoidal, f = 300 kHz, ILDO = 500 mA <sup>(15)</sup>	V <sub>LDO_RR</sub>	–	40	–	dB
LDO Maximum Dropout Voltage (VIN - VLDO), using IRL2703 <sup>(16)</sup> VLDO = 2.5 V, ILDO = 1000 mA	V <sub>DO</sub>	–	50	75	mV
LDO Current Sense Comparator Threshold Voltage (VCS - VLDO)	V <sub>CSTH</sub>	35	50	65	mV
LDO Pin Input Current, VLDO = 5.25 V	I <sub>LDO</sub>	1.0	1.9	4.0	mA
LDO Feedback Input Current (LFB Pin), VLFB = 0.8 V	I <sub>LFB</sub>	-1.0	–	1.0	μA
LDO Drive Output Current (LDRV Pin), VLDRV = 0 V	I <sub>LDRV</sub>	-5.0	-3.3	-2.0	mA
CS Pin Input Leakage Current VCS = 5.25 V	I <sub>CSLK</sub>	50	–	200	μA
LDO Pulldown MOSFET Q4 Current Limit T <sub>A</sub> = 25°C, VBST = 8.0 V (LDO Pin)	I <sub>M4_LIM</sub>	0.75	–	2.0	A
LDO Pulldown MOSFET Q4 RDS(ON) ID = 1.0 A, VBST = 8.0 V	R <sub>DS(ON)</sub>	–	–	1.9	Ω
LDO Recommended Output Capacitance	C <sub>LDO</sub>	–	10	–	μF
LDO Recommended Output Capacitor ESR	E <sub>SRCLDO</sub>	–	5.0	–	mΩ
Thermal Shutdown (LDO Pull-down MOSFET Q4) <sup>(15)</sup>	T <sub>SD</sub>	150	170	190	°C
Thermal Shutdown Hysteresis <sup>(15)</sup>	T <sub>SDHYS</sub>	–	10	–	°C

Notes

15. Design information only. This parameter is not production tested.
16. IDO refers to Load Current on External LDOFET - IRL2703 is the Intersil MOSFET IRL2703

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**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figure 33](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>CONTROL AND SUPERVISORY CIRCUITS</b>					
Enable (EN1, EN2) Input Voltage Threshold	$V_{TH\_EN}$	1.0	1.5	2.0	V
Enable (EN1, EN2) Pulldown Resistance	$R_{PU}$	30	55	90	$k\Omega$
$\overline{RST}$ Low-Level Output Voltage, $I_{OL} = 5.0\text{ mA}$	$V_{OL}$	–	–	0.4	V
$\overline{RST}$ Leakage Current, OFF State, Pulled Up to 5.25 V	$I_{LKG-RST}$	–	–	10	$\mu\text{A}$
$\overline{RST}$ Undervoltage Threshold on VOUT ( $\Delta V_{OUT}/V_{OUT}$ ) <sup>(17)</sup>	$V_{OUTITh}$	-14	–	-0.5	%
$\overline{RST}$ Overvoltage Threshold on VOUT ( $\Delta V_{OUT}/V_{OUT}$ ) <sup>(17)</sup>	$V_{OUTITh}$	0.5	–	14	%
$\overline{RST}$ Undervoltage Threshold on VLDO ( $\Delta V_{LDO}/V_{LDO}$ ) <sup>(17)</sup>	$V_{LDOITh}$	-12	–	-4.0	%
$\overline{RST}$ Overvoltage Threshold on VLDO ( $\Delta V_{LDO}/V_{LDO}$ ) <sup>(17)</sup>	$V_{LDOITh}$	4.0	–	12	%
$\overline{RST}$ Timer Voltage Threshold	$V_{TH-RT}$	1.0	1.2	1.5	V
$\overline{RST}$ Timer Source Current (RT pin at 0 V)	$I_{S-RT}$	-17	–	-34	mA
$\overline{RST}$ Timer Leakage Current	$I_{LKG-RT}$	-1.0	–	1.0	$\mu\text{A}$
$\overline{RST}$ Timer Saturation Voltage, Reset Timer Current = 300 $\mu\text{A}$	$V_{SAT-RT}$	–	35	100	mV
Maximum Recommended Value of the Reset Timer Capacitor	$C_t$	–	–	47	$\mu\text{F}$
CLKSEL Threshold Voltage	$V_{THCLKS}$	1.2	1.6	2.0	V
CLKSEL Pullup Resistance	$R_{PU-CLKS}$	60	120	240	$k\Omega$
ADDR Threshold Voltage <sup>(17)</sup>	$V_{THADDR}$	1.2	1.6	2.0	V
ADDR Pullup Resistance	$R_{PU-ADDR}$	60	120	240	$k\Omega$
Thermal Shutdown (IC sensor) <sup>(17)</sup>	$T_{LIM}$	150	170	190	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis <sup>(17)</sup>	$T_{LIMHYS}$	–	10	–	$^{\circ}\text{C}$

**SDA, SCL PINS I<sup>2</sup>C BUS (STANDARD)**

Input Threshold Voltage (Pin SCL), Rising Edge <sup>(17)</sup>	$V_{LTH}$	1.3	–	1.7	V
Input Threshold Voltage (Pin SDA)	$V_{LTH}$	1.3	–	1.7	V
SDA, SCL Input Current, Input Voltage = 5.25 V ( $V_{IN1}$ )	$I_I$	–	1.0	10	$\mu\text{A}$
SDA Low-Level Output Voltage, 3.0 mA Sink Current	$V_{OL}$	–	–	0.4	V
SDA, SCL Capacitance <sup>(17)</sup>	$C_{INPUT}$	–	7.0	10	pF

## Notes

17. Design information only. This parameter is not production tested.

**DYNAMIC ELECTRICAL CHARACTERISTICS**

**Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figures 33](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>BUCK CONVERTER</b>					
Duty Cycle Range (Normal Operation) <sup>(18)</sup>	D	0	–	95	%
Switching Node SW Rise Time <sup>(18)</sup> VIN = 5.0 V, ILOAD = 1.0 A	t <sub>RISE</sub>	–	7.0	–	ns
Switching Node SW Fall Time <sup>(18)</sup> VIN = 5.0 V, ILOAD = 1.0 A	t <sub>FALL</sub>	–	17	–	ns
Maximum Deadtime <sup>(18)</sup>	t <sub>D</sub>	–	35	–	ns
Buck Control Loop Propagation Delay <sup>(18)</sup> VINV < 0.8 V to VSW > 90% of High Level or VINV > 0.8 V to VSW < 10% of Low Level	t <sub>PD</sub>	–	50	–	ns
Soft Start Duration (Power Sequencing Disabled, EN1 = 1, EN2 = 1) <sup>(18)</sup>	t <sub>SS</sub>	200	350	800	μs
Fault Condition Time-Out <sup>(18)</sup>	t <sub>FAULT</sub>	–	10	–	ms
Retry Timer Cycle <sup>(18)</sup>	t <sub>Ret</sub>	–	100	–	ms
<b>OSCILLATOR</b>					
Oscillator Center Frequency <sup>(20)</sup> RF = 11.3 kΩ	f <sub>OSC</sub>	270	300	330	kHz
Oscillator Frequency Range	f <sub>OSC</sub>	200	–	400	kHz
Oscillator Frequency Adjusting Resistor Range	R <sub>FREQ</sub>	7.0	–	22	kΩ
Oscillator Frequency Adjustment <sup>(19), (20)</sup> RF = 7.0 kΩ	f <sub>OSC</sub>	400	–	–	kHz
Oscillator Frequency Adjustment <sup>(19), (20)</sup> RF = 22 kΩ	f <sub>OSC</sub>	–	–	200	kHz
Oscillator Default Frequency (Switching Frequency), FREQ Pin Open	f <sub>OSC</sub>	–	300	–	kHz
Oscillator Output Signal Duty Cycle (Square Wave, 180° Out-of-Phase with the Internal Suitable Oscillator)	D <sub>OSC</sub>	40	50	60	%
Synchronization Pulse Minimum Duration <sup>(18)</sup>	t <sub>SYNC</sub>	1.0	–	–	μs

Notes

- 18. Design information only. This parameter is not production tested.
- 19. see Figure 4 for more details
- 20. RF = RFREQ resistor connected to the FREQ pin.

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**Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figures 33](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

**BOOST REGULATOR**

Boost Regulator MOSFET Maximum ON Time <sup>(21)</sup>	$t_{ON}$	–	24	–	$\mu\text{s}$
Boost Regulator Control Loop Propagation Delay <sup>(21)</sup>	$t_{BST\_PD}$	–	50	–	ns
Boost Switching Node VBD Rise Time <sup>(21)</sup> IBST = 20 mA	$t_{B\_RISE}$	–	5.0		ns
Boost Switching Node VBD Fall Time <sup>(21)</sup> IBST = 20 mA	$t_{B\_FALL}$	–	3.0		ns

**LINEAR REGULATOR (LDO)**

Fault Condition Time-Out	$t_{FAULT}$	8.0	10	12	ms
Retry Timer Cycle	$t_{Ret}$	80	100	120	ms

**Reset Monitor ( $\overline{RST}$ )**

Monitoring LFB Pin Delay	$t_{D\_RST\_LFB}$	12	–	28	$\mu\text{s}$
Monitoring INV Pin Delay	$t_{D\_RST\_INV}$	12	–	28	$\mu\text{s}$

**SCA, SCL PIN, I<sup>2</sup>C BUS (STANDARD)**

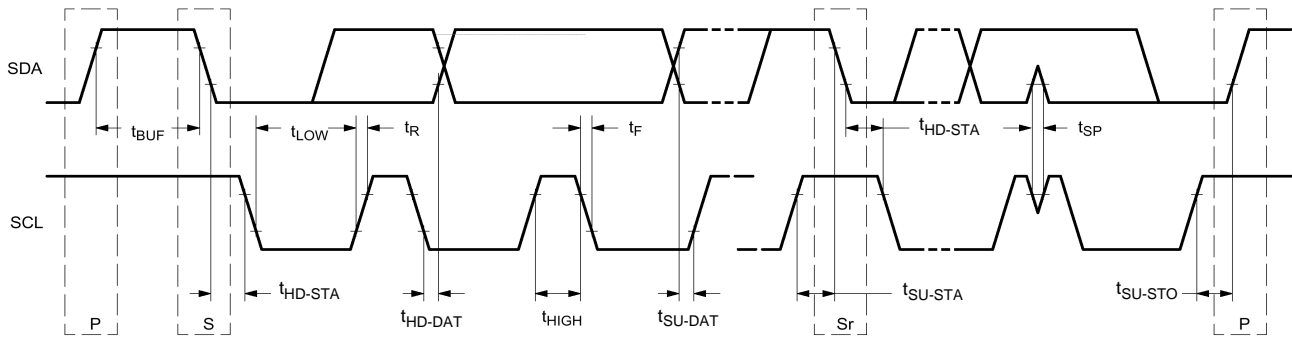
SCL Clock Frequency <sup>(21)</sup>	$f_{SCL}$	–	–	100	kHz
Bus Free Time Between a STOP and a START Condition <sup>(21)</sup>	$t_{BUF}$	4.7	–	–	$\mu\text{s}$
Hold Time (Repeated) START Condition (After this period, the first clock pulse is generated.) <sup>(21)</sup>	$t_{HD\_STA}$	4.0	–	–	$\mu\text{s}$
Low Period of the SCL Clock <sup>(21)</sup>	$t_{LOW}$	4.7	–	–	$\mu\text{s}$
High Period of the SCL Clock <sup>(21)</sup>	$t_{HIGH}$	4.0	–	–	$\mu\text{s}$
SDA Fall Time from $V_{IH\_MAX}$ to $V_{IL\_MIN}$ , Bus Capacitance 10 pF to 400 pF, 3.0 mA Sink Current <sup>(21), (23)</sup>	$t_F$	–	–	250	ns
Setup Time for a Repeated START Condition <sup>(21)</sup>	$t_{SU\_STA}$	4.7	–	–	$\mu\text{s}$
Data Hold Time for I <sup>2</sup> C Bus Devices <sup>(21), (22)</sup>	$t_{HD\_DAT}$	0.0	–	–	$\mu\text{s}$
Data Setup Time <sup>(21)</sup>	$t_{SU\_DAT}$	250	–	–	ns
Setup Time for STOP Condition <sup>(21)</sup>	$t_{SU\_STO}$	4.0	–	–	$\mu\text{s}$
Capacitive Load for Each Bus Line <sup>(21)</sup>	CB	–	–	400	pF

Notes

- Design information only. This parameter is not production tested.
- The device provides an internal hold time of at least 300 ns for the SDA signal (refer to the  $V_{IH\_MIN}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- $V_{IH}$  = High level voltage on I<sup>2</sup>C bus and  $V_{IL}$  = Low level voltage on I<sup>2</sup>C bus

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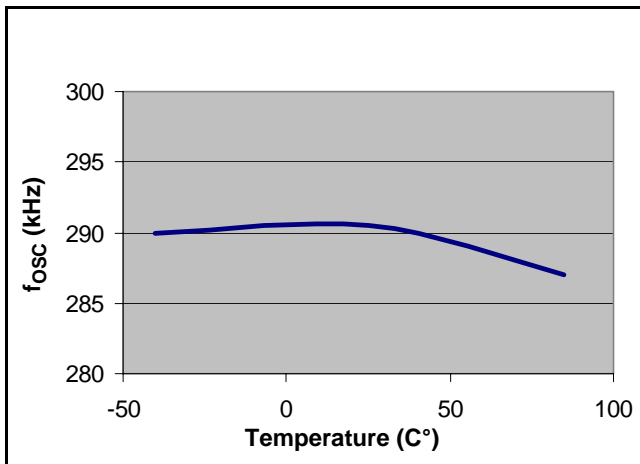
**TIMING DIAGRAM**



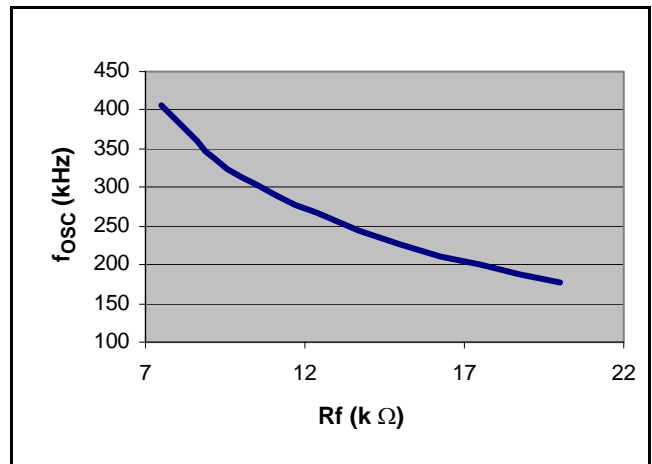
Note: Refer to the latest I<sup>2</sup>C bus specification for further details.

**Figure 4. Definition of Time on the I<sup>2</sup>C Bus**

**ELECTRICAL PERFORMANCE CURVES**



**Figure 5.  $f_{osc}$  vs. Temperature**



**Figure 6.  $f_{osc}$  vs.  $R_f$**

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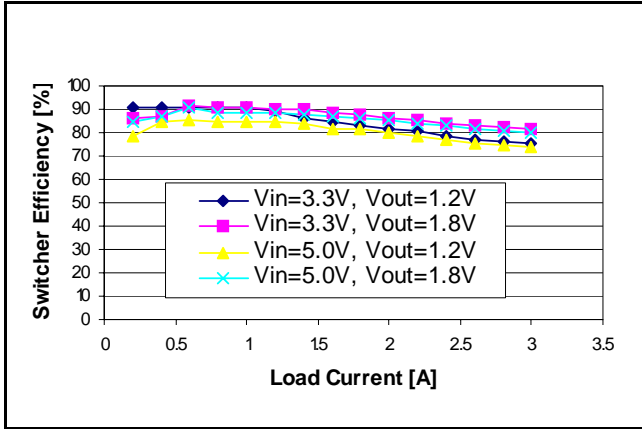


Figure 7. Switcher Efficiency vs. Load Current

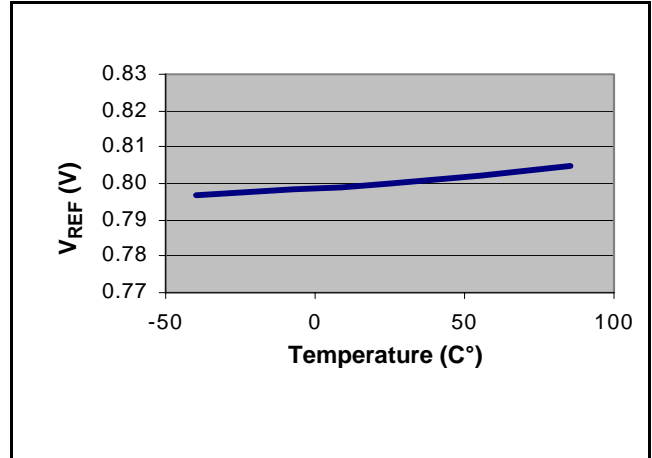


Figure 9. V<sub>REF</sub> vs. Temperature

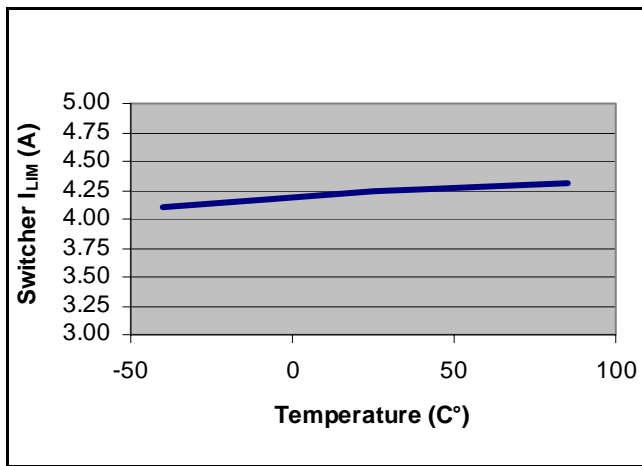


Figure 8. Switcher I<sub>LIM</sub> vs. Temperature

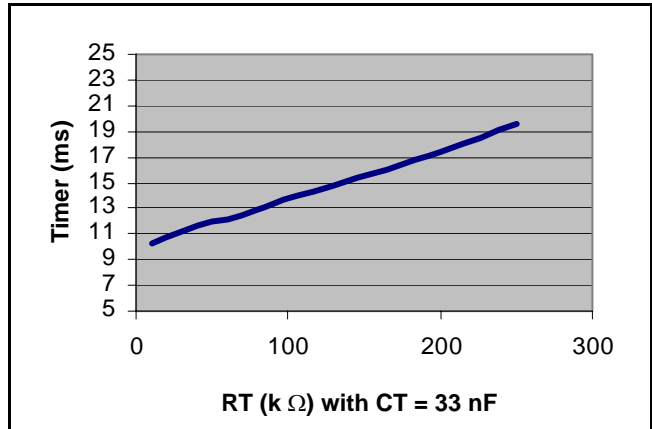


Figure 10. Timer (ms) vs. RT

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## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 34702 power supply integrated circuit provides the means to efficiently supply the Freescale Power QUICC and other families of Freescale microprocessors. It incorporates a high-performance synchronous buck regulator, supplying the microprocessor's core, and a low dropout (LDO) linear regulator providing the microprocessor I/O and bus voltages.

This device incorporates many advanced features; e.g., precisely maintained up/down power sequencing, ensuring the proper operation and protection of the CPU and power system. At the same time, it provides high flexibility of configuration, allowing the maximum optimization of the power supply system.

### FUNCTIONAL PIN DESCRIPTION

#### OSCILLATOR FREQUENCY PIN (FREQ)

This switcher frequency selection pin can be adjusted by connecting external resistor RF to the FREQ pin. The default switching frequency (FREQ pin left open or tied to VDDI) is set to 300 kHz.

#### INVERTING INPUT PIN (INV)

Buck Controller Error Amplifier inverting input.

#### OUTPUT VOLTAGE PIN (VOUT)

Output voltage of the buck converter. Input pin of the switching regulator power sequence control circuit.

#### INPUT VOLTAGE 2 PINS (VIN2)

Buck regulator power input. Drain of the high-side power MOSFET.

#### SWITCH PINS (SW)

Buck regulator switching node. This pin is connected to the inductor.

#### GROUND PINS (GND)

Analog ground of the IC, thermal heatsinking.

#### POWER GROUND PINS (PGND)

Buck regulator power ground.

#### BOOST DRAIN PIN (VBD)

Drain of the internal boost regulator power MOSFET.

#### BOOST VOLTAGE PIN (VBST)

Internal boost regulator output voltage. The internal boost regulator provides a 20 mA output current to supply the drive circuits for the integrated power MOSFETs and the external N-channel power MOSFET of the linear regulator. The voltage at the VBST pin is 7.75V nominal.

#### BOOTSTRAP PIN (BOOT)

Bootstrap capacitor input.

#### SERIAL DATA PIN (SDA)

I<sup>2</sup>C bus pin. Serial data.

#### SERIAL CLOCK PIN (SCL)

I<sup>2</sup>C bus pin. Serial clock.

#### LINEAR COMPENSATION PIN (LCMP)

Linear regulator compensation pin.

#### LINEAR FEEDBACK PIN (LFB)

Linear regulator feedback pin.

#### LINEAR REGULATOR PIN (LDO)

Input pin of the linear regulator power sequence control circuit.

#### CURRENT SENSE PIN (CS)

Current sense pin of the LDO. Overcurrent protection of the linear regulator external power MOSFET. The voltage drop over the LDO current sense resistor RS is sensed between the CS and LDO pins. The LDO current limit can be adjusted by selecting the proper value of the current sensing resistor RS.

#### LINEAR DRIVE PIN (LDRV)

LDO gate drive of the external pass N-channel MOSFET.

#### INPUT VOLTAGE 1 PIN (VIN1)

The input supply pin for the integrated circuit. The internal circuits of the IC are supplied through this pin.



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**POWER SUPPLY PIN (VDDI)**

Internal supply voltage. A ceramic low ESR 1uF 6V X5R or X7R capacitor is recommended.

**ADDRESS PIN (ADDR)**

The ADDR pin is used to set the address of the device when used in an I<sup>2</sup>C communication. This pin can either be tied to VDDI or grounded through a 10 kΩ resistor. Refer to [I<sup>2</sup>C Bus Operation on page 26](#) for more information on this pin.

**ENABLE 1 AND 2 PINS (EN1 AND EN2)**

These two pins permit positive logic control of the Enable function and selection of the Power Sequencing mode concurrently. [Table 5](#) depicts the EN1 and EN2 function and Power Sequencing mode selection.

Both EN1 and EN2 pins have internal pull-down resistors and both can withstand a short circuit to the supply voltage, 6.0 V.

**Table 5. Operating Mode Selection**

EN1	EN2	Operating Mode
0	0	Regulators Disabled
0	1	Standard Power Sequencing
1	0	Inverted Power Sequencing
1	1	No Power Sequencing, Regulators Enabled

**RESET TIMER PIN (RT)**

The Reset Timer power-up delay (RT) pin is used to set the delay between the time when the LDO and switcher outputs are active and stable and the  $\overline{RST}$  output is released. An external resistor and capacitor are used to program the timer. The power-up delay can be obtained by using the following formula:

$$t_D = 10 \text{ ms} + R_t C_t$$

Where  $R_t$  is the Reset Timer programming resistor and  $C_t$  is the Reset Timer programming capacitor, both connected in parallel from RT to ground.

**Note** Observe the maximum  $C_t$  value and expect reduced accuracy if  $R_t$  is less than 10 kΩ.

**RESET OUTPUT PIN ( $\overline{RST}$ )**

The Reset Control circuit monitors both the switching regulator and the LDO feedback voltages. It is an open drain output and has to be pulled up to some supply voltage (e.g., the output of the LDO) by an external resistor.

The Reset Control circuit supervises both output voltages—the linear regulator output VLDO and the switching regulator output VOUT. When either of these two regulators is out of regulation (high or low), the  $\overline{RST}$  pin is pulled low. There is a 20 μs delay filter preventing erroneous resets. During power-up sequencing,  $\overline{RST}$  is held low until the Reset Timer times out.

**CLOCK SELECTION PIN (CLKSEL)**

This pin sets the CLKSYN pin as either an oscillator output or a synchronization input pin. The CLKSEL pin is also used for the I<sup>2</sup>C address selection.

**CLOCK SYNCHRONIZATION PIN (CLKSYN)**

Oscillator output/synchronization input pin.

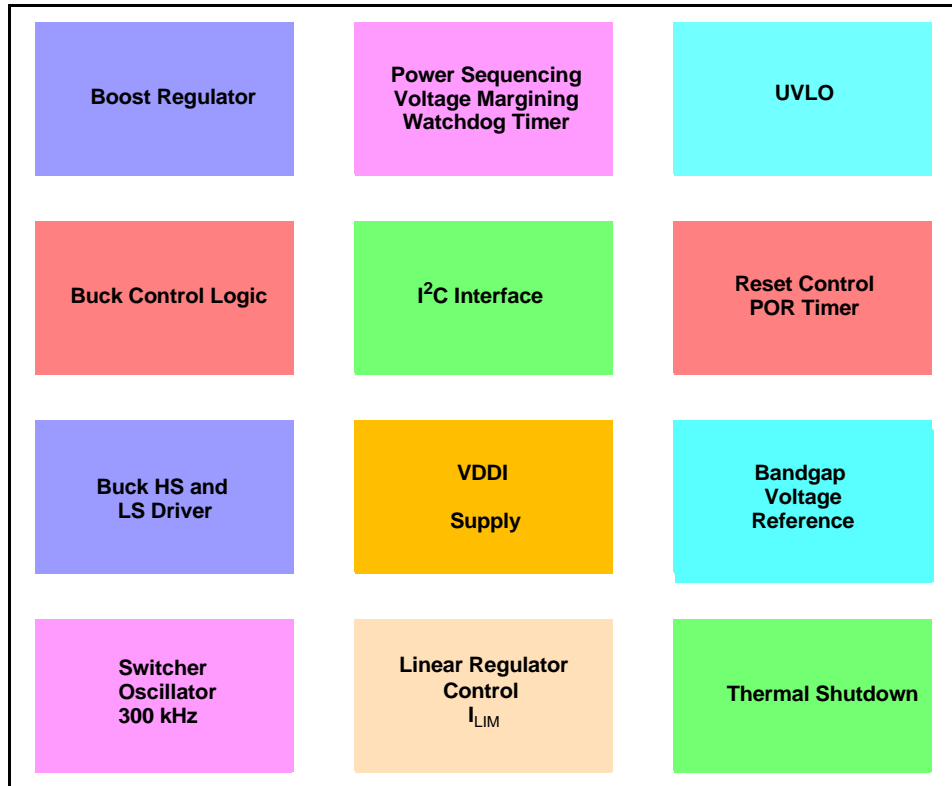
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**FUNCTIONAL INTERNAL BLOCK DESCRIPTION**

**INTRODUCTION**

The 34702 incorporates a high-performance synchronous buck regulator, supplying the microprocessor's core, and a low dropout (LDO) linear regulator providing the microprocessor I/O and bus voltages. This device

incorporates many advanced features; e.g., precisely maintained up/down power sequencing, ensuring the proper operation and protection of the CPU and power system.



**Figure 11. 34702 Functional Internal Block Diagram**

**BOOST REGULATOR**

A boost regulator provides a high voltage necessary to properly drive the buck regulator power MOSFETs, especially during the low input voltage condition. The LDO regulator external N-channel MOSFET gate is also powered from the boost regulator. In order to properly enhance the high-side MOSFETs when only a +3.3 V supply rail powers the integrated circuit, the boost regulator provides an output voltage of 7.75 V nominal value.

The 34702 boost regulator uses a simple hysteretic current control technique, which allows fast power-up and does not require any compensation. When the boost regulator main power switch (low side) is turned on, the current in the inductor starts to ramp up. After the inductor current reaches the upper current limit (nominally set at 1.0 A), the low-side switch is turned off and the current charges the output capacitor through the internal rectifier.

When the inductor current falls below the valley current limit value (nominally 600 mA), the low-side switch is turned on again, starting the next switching cycle. After the boost regulator output capacitor reaches approximately 6.0 volts, the peak and valley current limit levels are proportionally scaled down to approximately one fifth of their original values. When the boost regulator reaches its regulation limit (7.75 V typical), the low-side switch is turned off until the output voltage falls below the regulation limit again.

The higher current limit values in the beginning of the boost regulator start-up sequence allow fast power up of the whole IC, while the normal operation with reduced current limit greatly reduces the switching noise and therefore improves the overall EMC performance. See [Figure 12](#) for the boost regulator output voltage and inductor current waveforms (picture not to scale).

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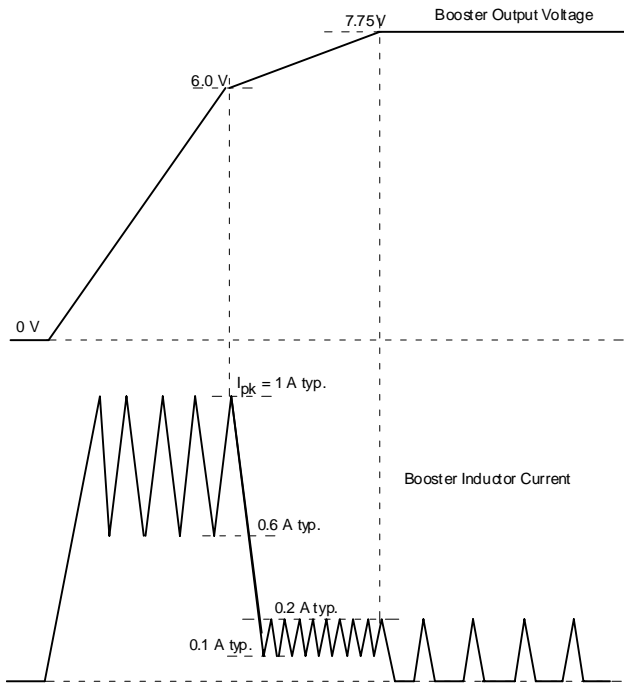


Figure 12. Boost Regulator Startup (Not To Scale)

**SWITCHING REGULATOR**

The switching regulator is a high-frequency (300 kHz default, adjustable in the range from 200 kHz to 400 kHz), synchronous buck converter driving integrated high-side and low-side N-channel power MOSFETs. The switching regulator output voltage is adjustable by means of an external resistor divider to provide the required output voltage within  $\pm 2.0\%$  accuracy, and is intended to directly power the core of the microprocessor. The buck controller uses a PWM Voltage Mode Control topology with Feed-Forward to achieve excellent line and load regulation.

The 34702 integrated boost regulator provides a 7.75 V rail which is used to properly bias the switcher's MOSFET. In addition, the boost structure has a very low start up voltage (Typically 1.6 V), hence ensuring very low input voltage functionality. A typical bootstrap technique is used to provide voltage necessary to properly enhance the high-side MOSFET gate. When the regulator is supplied only from low-input voltage (e.g., single +3.3 V supply rail), the bootstrap capacitor is charged from the internal boost regulator output VBST through an external diode. This arrangement allows the 34702 to operate from very low input voltage and also comply with the power sequencing requirements of the supplied microcontroller.

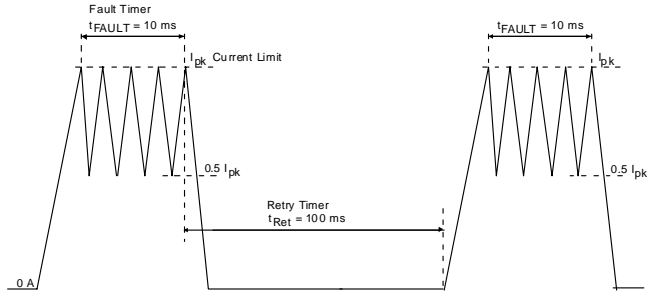


Figure 13. Switching Regulator Current Limit (Not To Scale)

To avoid destruction of the supplied circuits, the switching regulator has a current limit with retry capability. When an overcurrent condition occurs and the switch current reaches the peak current limit value, the main (high-side) switch is turned off until the inductor current decays to the valley value, which is one-half of the peak current limit. If an overcurrent condition exists for 10 ms, the buck regulator control circuit shuts the switcher OFF and the switcher retry timer starts to time out. When the timer expires after 100 ms, the switcher engages the start-up sequence and runs for 10 ms, repeatedly checking for the overcurrent condition. Figure 13 describes the switching regulator overcurrent condition and current limit. During the current limited operation (e.g., in case of short circuit on the switching regulator output), the switching regulator operation is not synchronized to the oscillator frequency. Figure 14 (respectively Figure 15) depicts the current limit with a retry capability feature of the switcher (respectively LDO).

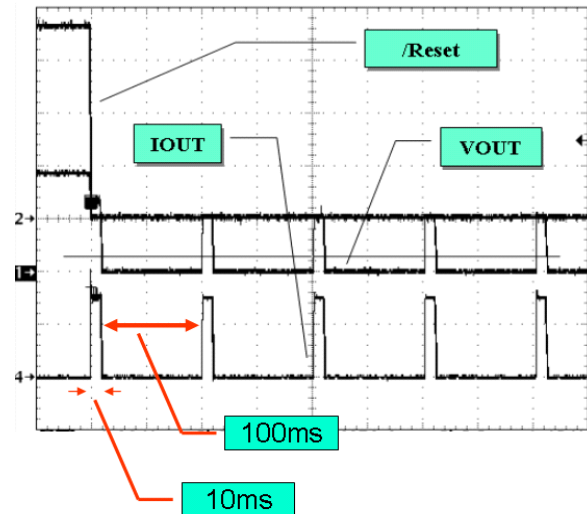
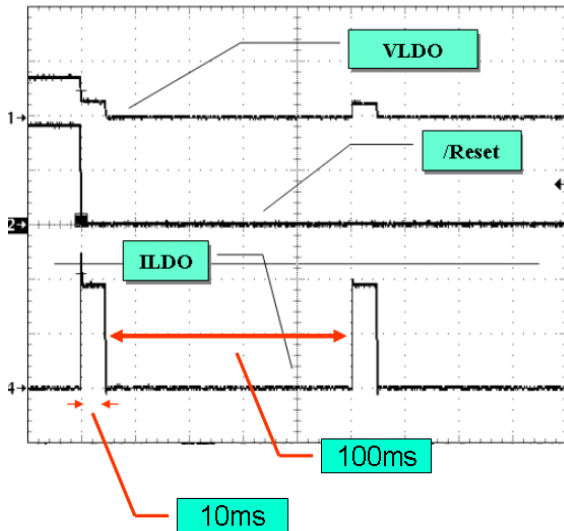


Figure 14. Switching Converter Overcurrent Protection

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**Figure 15. LDO Converter Overcurrent Protection**

The output voltage VOUT can be adjusted by means of an external resistor divider connected to the feedback control pin INV. The switching regulator output voltage can be adjusted in the range of 0.8 V to VIN - buck dropout voltage. Power-up, power-down, and fault management are coordinated with the linear regulator.

**SWITCHER OSCILLATOR**

A 300 kHz (default) oscillator sets the switching frequency of the buck regulator. The frequency of the oscillator can be adjusted between 200 kHz and 400 kHz by an optional external resistor RF connected from the FREQ pin of the integrated circuit to ground. See [Figure 6](#) on page 14 for frequency resistor selection.

The CLKSYN pin can be configured as either an oscillator output when the CLKSEL pin is left open or as a synchronization input when the CLKSEL pin is grounded. The oscillator output signal is a square wave logic signal with 50% duty cycle, 180 degrees out-of-phase with the internal clock signal. This allows opposite phase synchronization of two 34702 devices.

When the CLKSYN pin is used as a synchronization input (CLKSEL pin grounded), the external resistor RF chosen from the chart in [Figure 6](#) should be used to synchronize the internal slope compensation ramp to the external clock. Operation is only recommended between 200 kHz and 400 kHz. The supplied synchronization signal does not need to be 50% duty cycle. Minimum pulse width is 1.0 μs.

**LOW DROPOUT LINEAR REGULATOR (LDO)**

The adjustable low dropout linear regulator (LDO) is capable of supplying a 1.0 A output current. It has a current limit with retry capability. When the voltage measured across the current sense resistor reaches the 50 mV threshold, the control circuit limits the current for 10 ms. If the overcurrent condition still exists, the linear regulator is turned off and the retry timer starts to time out. When the timer expires after

100 ms, the LDO tries to power up again for 10 ms, repeatedly checking for the overcurrent condition. The current limit of the LDO can be set by using the following formula:

$$I_{LIM} = 50 \text{ mV} / R_S$$

Where RS is the LDO current sense resistor, connected between the CS pin and the LDO pin output (see [Figure 33](#) on page 34), and 50 mV is the typical value of the LDO current sense comparator threshold voltage.

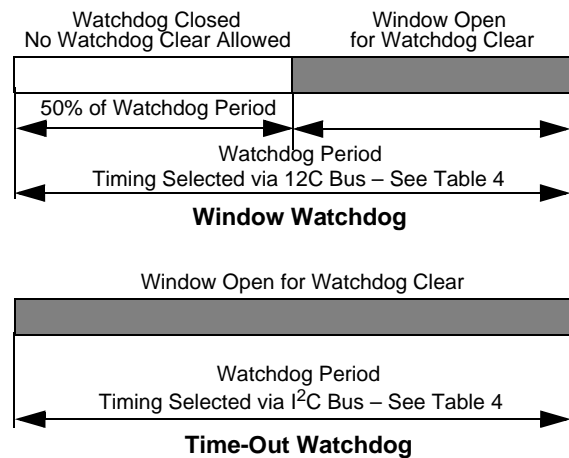
When no current sense resistor is used, it is still possible to detect the overcurrent condition by tying the current sense pin CS to the VBST voltage. In this case, the overcurrent condition is sensed by saturation of the linear regulator driver buffer.

The output voltage of the LDO can be adjusted by means of an external resistor divider connected to the feedback control pin LFB. The linear regulator output voltage can be adjusted in the range of 0.8 V to VIN - LDO dropout voltage. Power-up, power-down, and fault management are coordinated with the switching regulator.

**POWER SEQUENCING VOLTAGE MARGINING WATCHDOG TIMER**

A watchdog function is available via I<sup>2</sup>C bus communication. It is possible to select either window watchdog or time-out watchdog operation, as illustrated in [Figure 16](#).

Watchdog time-out starts when the watchdog function is activated via I<sup>2</sup>C bus sending a Watchdog Programming command byte, thus determining watchdog operation (window or time-out) and period duration (refer to [Table 8](#), page 27). If the watchdog is cleared by receiving a new Watchdog Programming command through the I<sup>2</sup>C bus, the watchdog timer is reset and the new time-out period begins. If the watchdog time expires, the RST will become active (LOW) for a time determined by the RC components of the RT timer plus 10 ms. After a watchdog time-out, the function is no longer active.



**Figure 16. Watchdog Operation**

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When the Window Watchdog function is selected, the timer cannot be cleared during the Closed Window time, which is 50% of the total watchdog period. When the watchdog is cleared, the timer is reset and starts a new time-out period. If the watchdog is not cleared during the Open

Window time, the  $\overline{\text{RST}}$  will become active (LOW) for a time determined by the RC components of the RT timer plus 10 ms.



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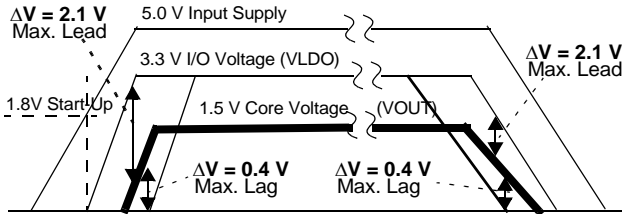
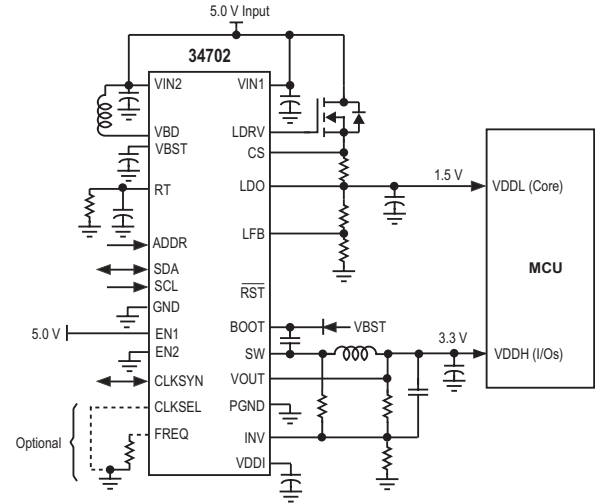
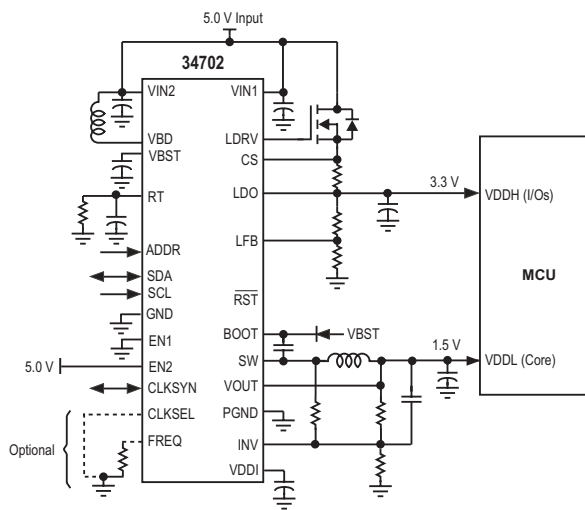


Figure 18. Standard Power Up/Down Sequence in +5.0 V Supply System

STANDARD POWER SEQUENCING

When the power supply IC operates in the Standard Power Sequencing mode, the switcher output provides the core voltage for the microprocessor. This situation and operating conditions are illustrated in Figures 17 and 18. Table 5, page 17, shows the Power Sequencing mode selection.

INVERTED POWER SEQUENCING

When the power supply IC is operating in the Inverted Power Sequencing mode, the linear regulator (LDO) output provides the core voltage for the microprocessor, as illustrated in Figure 19. Table 5 shows the Power Sequencing mode selection.

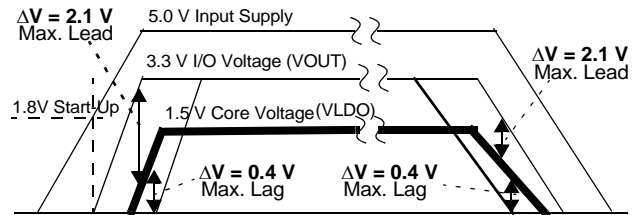


Figure 19. Inverted Power Up/Down Sequence in +5.0 V Supply System

ASSUMED REQUIREMENTS

1. I/O supply voltage not to exceed core voltage by more than 2.0 V.
2. Core supply voltage not to exceed I/O voltage by more than 0.4 V.

Methods of Control

The 34702 has several methods of monitoring and controlling the regulator output voltages, as described in the paragraphs below. Power sequencing control is also achieved through the intrinsic operation of the regulators. The EN1 and EN2 pins can be used to select the proper power sequencing mode required by the powered system or to disable the power sequencing (refer to Table 5).

Intrinsic Operation

For both the LDO and switcher, whenever the output voltage is below the regulation point, the LDO external Pass MOSFET is on, or the Buck High-Side MOSFET is on at a duty cycle controlled by the switcher. Because these devices are MOSFETs, current can flow in either direction, balancing the voltages via the common supply pin. The ability to maintain the MOSFETs on is dependent on the available gate voltage, and thus the size of the boost regulator storage capacitor.

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### Standard Power Sequencing Control

Comparators monitor voltage differences between the LDO (LDO pin) and the switcher (VOUT pin) outputs as follows:

1.  $LDO > VOUT + 1.9 V$ , *turn off LDO*. The LDO can be forced off. This occurs whenever the LDO output voltage exceeds the switcher output voltage by more than 1.9 V.
2.  $LDO > VOUT + 2.0 V$ , *shunt LDO to ground*. If turning off the LDO is insufficient and the LDO output voltage exceeds the switcher output voltage by more than 2.0 V, a 1.5  $\Omega$  shunt MOSFET is turned on that discharges the LDO load capacitor to ground. The shunt MOSFET is used for switcher output shorts to ground and for power down in case of  $VIN1 \neq VIN2$  with the switcher output falling faster than the LDO.
3.  $LDO < VOUT + 1.9 V$  cancel (2).
4.  $LDO < VOUT + 1.8 V$ , *cancel (1) above, re-enable LDO*. Normal operation resumes when the LDO output voltage is less than 1.8 V above the switcher output voltage.
5.  $LDO < VOUT - 0.1 V$ , *turn off switcher*. The switcher can be forced off. This occurs whenever the LDO is less than  $VOUT - 0.1 V$ .
6.  $LDO < VOUT - 0.3 V$ , *turn on Sync (LS) MOSFET and 1.5  $\Omega$  VOUT sink MOSFET*. The Buck High-Side MOSFET is forced off and the Sync MOSFET is forced on. This occurs when the switcher output voltage exceeds the LDO output by more than 300 mV.
7.  $LDO > VOUT - 0.3 V$ , *cancel (6)*.
8.  $LDO > VOUT - 0.1 V$ , *cancel (5)*. Normal operation resumes when  $LDO < VOUT - 0.1 V$ .

### Inverted Power Sequencing Control

Comparators monitor voltage differences between the switcher (VOUT pin) and LDO (LDO pin) outputs as follows:

1.  $VOUT > LDO + 1.8 V$ , *turn off VOUT*. The switcher VOUT can be forced off. This occurs whenever the VOUT output voltage exceeds the LDO output voltage by more than 1.8 V.
2.  $VOUT > LDO + 2.0 V$ , *shunt VOUT to ground*. If turning off the switcher VOUT is insufficient and the VOUT output voltage exceeds the LDO output voltage by more than 2.0 V, a 1.5  $\Omega$  shunt MOSFET and the switcher synchronous MOSFET are turned on to discharge the VOUT load capacitor to ground. The shunt MOSFET and synchronous MOSFET are used for LDO output shorts to ground and for power-down in case of  $VIN1 \neq VIN2$  with LDO output falling faster than the VOUT.
3.  $VOUT < LDO + 1.8 V$ , *cancel (1) and (2) above, re-enable VOUT*. Normal operation resumes when the

VOUT output voltage is less than 1.8 V above the LDO output voltage.

4.  $VOUT < LDO + 2.0 V$ , *cancel (2)*
5.  $VOUT < LDO - 0.2 V$ , *turn off LDO*. The LDO can be forced off. This occurs whenever the VOUT is less than  $VLDO - 0.2 V$ .
6.  $VOUT < LDO - 0.3 V$ , *turn on the 1.5  $\Omega$  LDO sink MOSFET*. This occurs when the LDO output voltage exceeds the VOUT output by more than 300 mV.
7.  $VOUT < LDO - 0.2 V$ , *cancel (6)*.
8.  $VOUT < LDO - 0.1 V$ , *cancel (5)*. Normal operation resumes when  $VOUT > LDO - 0.1 V$ .

### STANDARD OPERATING MODE

#### Single 3.3 V Supply, $VIN = VIN1 = VIN2 = 3.3 V$

The 3.3 V supplies the microprocessor I/O voltage, the switcher supplies core voltage (e.g., 1.5 V nominal), and the LDO operates independently (see [Figure 17](#), page 22). Power sequencing depends only on the normal switcher intrinsic operation to control the Buck High-Side MOSFET.

#### Power-Up

When  $VIN$  is rising, initially VOUT is below the regulation point and the Buck High-Side MOSFET is on. In order not to exceed the 2.1 V differential requirement between the I/O ( $VIN$ ) and the core (VOUT), the switcher must start up at 2.1 V or less and be able to maintain the 2.1 V or less differential. The maximum slew rate for  $VIN$  is 1.0 V/ms.

#### Power-Down

When  $VIN$  is falling, VOUT falls below the regulation point; therefore, the Buck High-Side MOSFET is on. In the case where VOUT is falling faster than  $VIN$ , the Buck High-Side MOSFET attempts to maintain VOUT. In the case where  $VIN$  is falling faster than VOUT, the Buck High-Side MOSFET is also on, and the VOUT load capacitor is discharged through the Buck High-Side MOSFET to  $VIN$ . Thus, provided  $VIN$  does not fall too fast, the core voltage (VOUT) does not exceed the I/O voltage ( $VIN$ ) by more than a maximum of 0.4 V.

#### Shorted Load

1. *VOUT shorted to ground*. This causes the I/O voltage to exceed the core voltage by more than 2.1 V. No load protection.
2. *VIN shorted to ground*. Until the switcher load capacitance is discharged, the core voltage exceeds the I/O voltage by more than 0.4 V. By the intrinsic operation of the switcher, the load capacitor is discharged rapidly through the Buck High-Side MOSFET to  $VIN$ .
3. *VOUT shorted to supply*. No load protection. 34702 is protected by current limit and thermal shutdown.



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### Single 5.0 V Supply, VIN1 = VIN2, or Dual Supply VIN1 ≠ VIN2

The LDO supplies the microprocessor I/O voltage. The switcher supplies the core (e.g., 1.5 V nominal) (see [Figure 18](#), page 23).

#### Power-Up

This condition depends upon the regulator current limit, load current and capacitance, and the relative rise times of the VIN1 and VIN2 supplies. There are two cases:

1. *LDO rises faster than VOUT.* The LDO uses control methods (1) and (2) described in the section [Methods of Control on page 23](#).
2. *VOUT rises faster than LDO.* The switcher uses control methods (5) and (6) described in the section [Methods of Control on page 23](#).

#### Power-Down

This condition depends upon the regulator load current and capacitance and the relative fall times of the VIN1 and VIN2 supplies. There are two cases:

1. *VOUT falls faster than LDO.* The LDO uses control methods (1) and (2) described in the section [Methods of Control on page 23](#).  
In the case VIN1 = VIN2, the intrinsic operation turns on both the Buck High-Side MOSFET and the LDO external Pass MOSFET, and discharges the LDO load capacitor into the VIN supply.
2. *LDO falls faster than VOUT.* The switcher uses control methods (5) and (6) described in the section [Methods of Control on page 23](#).

#### Shorted Load

1. *VOUT shorted to ground.* The LDO uses method (1) and (2) described in the section [Methods of Control on page 23](#).
2. *LDO shorted to ground.* The switcher uses control methods (5) and (6) described in the section [Methods of Control on page 23](#).
3. *VIN1 shorted to ground.* Device is not working.
4. *VIN2 shorted to ground with VIN1 and VIN2 different.* This is equivalent to the switcher output shorted to ground.
5. *VOUT shorted to supply.* No load protection. 34702 is protected by current limit and thermal shutdown.
6. *LDO shorted to supply.* No load protection. 34702 is protected by current limit and thermal shutdown.

## INVERTED OPERATING MODE

### Single 3.3 V Supply, VIN = VIN1 = VIN2 = 3.3 V

The 3.3 V supplies the microprocessor I/O voltage, the LDO supplies core voltage (e.g., 1.5 V nominal), and the switcher VOUT operates independently. Power sequencing

depends only on the normal LDO intrinsic operation to control the Pass MOSFET.

#### Power-Up

When VIN is rising, initially LDO is below the regulation point and the Pass MOSFET is on. In order not to exceed the 2.1 V differential requirement between the I/O (VIN) and the core (LDO), the LDO must start up at 2.1 V or less and be able to maintain the 2.1 V or less differential. The maximum slew rate for VIN is 1.0 V/ms.

#### Power-Down

When VIN is falling, LDO falls below the regulation point; therefore, the Pass MOSFET is on. In the case where LDO is falling faster than VIN, the Pass MOSFET attempts to maintain LDO. In the case where VIN is falling faster than LDO, the Pass MOSFET is also on, and the LDO load capacitor is discharged through the Pass MOSFET to VIN. Thus, provided VIN does not fall too fast, the core voltage (LDO) does not exceed the I/O voltage (VIN) by more than maximum of 0.4 V.

#### Shorted Load

1. *LDO shorted to ground.* This will cause the I/O voltage to exceed the core voltage by more than 2.1 V. No load protection.
2. *VIN shorted to ground.* Until the LDO load capacitance is discharged, the core voltage exceeds the I/O voltage by more than 0.4 V. By the intrinsic operation of the LDO, the load capacitor is discharged rapidly through the Pass MOSFET to VIN.
3. *LDO shorted to supply.* No load protection.

### Single 5.0 V Supply, VIN1 = VIN2, or Dual Supply VIN1 ≠ VIN2

The switcher VOUT supplies the microprocessor I/O voltage. The LDO supplies the core (e.g., 1.5 V nominal) (see [Figure 19](#), page 23).

#### Power-Up

This condition depends upon the regulator current limit, load current and capacitance, and the relative rise times of the VIN1 and VIN2 supplies. There are two cases:

1. *VOUT rises faster than LDO.* The switcher VOUT uses control methods (1) and (2) described in the section [Methods of Control on page 23](#).
2. *LDO rises faster than VOUT.* The LDO uses control methods (5) and (6) described in the section [Methods of Control on page 23](#).

#### Power-Down

This condition depends upon the regulator load current and capacitance and the relative fall times of the VIN1 and VIN2 supplies. There are two cases:

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1. *LDO falls faster than VOUT*. The VOUT uses control methods (4) and (5) described in the section [Methods of Control on page 23](#).  
 In the case VIN1 = VIN2, the intrinsic operation turns on both the Buck High-Side MOSFET and the LDO external Pass MOSFET, and discharges the VOUT load capacitor into the VIN supply.
2. *VOUT falls faster than LDO*. The LDO uses control methods (5) and (6) described in the section [Methods of Control on page 23](#).

### Shorted Load

1. *LDO shorted to ground*. The VOUT uses methods (1) and (2) described in the section [Methods of Control on page 23](#).
2. *VOUT shorted to ground*. The LDO uses control methods (5) and (6) described in the section [Methods of Control on page 23](#).
3. VIN1 shorted to ground. Device is not working.
4. *VIN2 shorted to ground*. This is equivalent to the switcher VOUT output shorted to ground.
5. *LDO shorted to supply*. No load protection. 34702 is protected by current limit and thermal shutdown.
6. *VOUT shorted to supply*. No load protection. 34702 is protected by current limit and thermal shutdown.

## LOGIC COMMANDS AND REGISTERS

### I<sup>2</sup>C BUS OPERATION

The 34702 device is compatible with the I<sup>2</sup>C interface standard. SDA and SCL pins are the Serial Data and Serial Clock pins of the I<sup>2</sup>C bus.

### I<sup>2</sup>C COMMAND AND DATA FORMATS

#### Communication Start

Communication starts with a START condition, followed by the slave device unique address. The Read/Write (R/W) bit defines whether the data should be read from or written to the device (the 34702 operates only as a slave device; therefore, the R/W bit should always be set to 0). The 34702 responds by sending the Acknowledge bit (Ack) to the master device. [Figure 20](#) illustrates the beginning of an I<sup>2</sup>C communication for a 7-bit slave address.

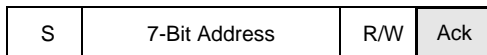


Figure 20. Communication Start Using 7-Bit Address

#### Slave Address Definition

34702 has the two least significant address bits (LSB) defined by the state of the CLKSEL pin (A1) and the ADDR pin (A0).

**Note** The state of the CLKSEL pin also defines the configuration of the oscillator synchronization CLKSYN pin. Leaving the CLKSEL pin open or pulling it high defines the CLKSYN pin as an oscillator output. When the CLKSEL pin is pulled low, the CLKSYN pin is configured as a synchronization input for the external clock signal.

This feature allows up to four 34702 ICs to communicate in the same I<sup>2</sup>C bus, all of them sharing the same high-order address bits. A different combination of the two LSB address bits A1 and A0 can be assigned to each individual part to

assure its unique address. [Figure 21](#) illustrates the flexible addressing feature for a 7-bit address. [Table 6](#) provides the definition of the selectable portion of the device address.

When the ADDR pin is used and put to low level, pull the ADDR pin to ground through a 10 kΩ resistor.

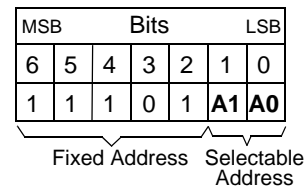


Figure 21. Address Bit Definition for 7-Bit Address

Table 6. Definition of Selectable Portion of Device Address

CLKSEL Pin	ADDR Pin	A1	A0
Low	Low	0	0
Low	High (Open)	0	1
High (Open)	Low	1	0
High (Open)	High (Open)	1	1

#### Writing Data Into the Slave Device

After the address acknowledgment by the slave, DATA can be written into the slave registers. The R/W bit must be set to 0 to allow DATA to be written into the 34702. [Figure 22](#) shows the data write sequence. Actions performed by the slave device are grayed.

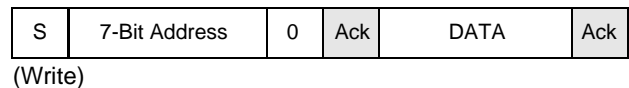


Figure 22. Data Transfer for Write Operations

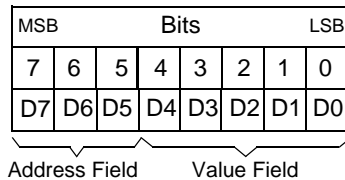
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**DATA Definition**

The DATA field in the single Data Transfer contains one or several Command Bytes. The Command Byte identifies the kind of operation required by the master to be performed and has two fields, as illustrated in [Figure 23](#):

1. Address field
2. Value field

The address field is selected from the list in [Table 7](#).



**Figure 23. Command Byte**

**Table 7. Address Field Definitions**

Address Field	Operation	Write
001	Voltage Margining	W
011	Watchdog	W

Refer to [Table 8](#), page 27, which summarizes the value field definitions for the entire set of operation options.

**Table 8. Command Byte Definitions**

Operation	Address			Value				Action	
Voltage Margining (As a 2nd Command Byte)	0	0	1	0	0	0	0	1st Command	
	0	0	1	x	0	0	0	Output Nominal	
	0	0	1	x	0	0	0	1	+ 1.0%
	0	0	1	x	0	0	1	1	+ 2.0%
	0	0	1	x	0	1	0	0	+ 3.0%
	0	0	1	x	0	1	0	0	+ 4.0%
LDO Output: x=0	0	0	1	x	0	1	0	1	+ 5.0%
Switcher Output x=1	0	0	1	x	0	1	1	0	+ 6.0%
	0	0	1	x	0	1	1	1	+ 7.0%
	0	0	1	x	1	0	0	0	- 1.0%
	0	0	1	x	1	0	0	1	- 2.0%
	0	0	1	x	1	0	1	0	- 3.0%
	0	0	1	x	1	0	1	1	- 4.0%
	0	0	1	x	1	1	0	0	- 5.0%
	0	0	1	x	1	1	0	1	- 6.0%
0	0	1	x	1	1	1	0	- 7.0%	

**Table 8. Command Byte Definitions**

Watchdog Programming (As a 2nd Command Byte)	0	1	1	0	0	0	0	0	1st Command
	0	1	1	0	0	0	0	0	WD OFF (24)
	0	1	1	0	1	0	0	0	WD 1280 ms Wind. OFF
	0	1	1	0	1	0	0	1	WD 320 ms Wind. OFF
	0	1	1	0	1	0	1	0	WD 80 ms Wind. OFF
	0	1	1	0	1	0	1	1	WD 20 ms Wind. OFF
	0	1	1	0	1	1	0	0	WD 1280 ms Wind. ON
	0	1	1	0	1	1	0	1	WD 320 ms Wind. ON
	0	1	1	0	1	1	1	0	WD 80 ms Wind. ON
	0	1	1	0	1	1	1	1	WD 20 ms Wind. ON

Notes

24. The Watchdog timer is turned ON automatically after receiving any other valid command byte changing watchdog time.

**Security in Writing Commands**

To improve the security level, a so-called *first command* is defined to initiate each write communications. The first command identifies the operation, which is executed by the following Command Byte.

A first command has the address field equal to the related operation one, followed by a null value field (all zeros). [Table 9](#) summarizes first command definitions. The master sends the first command before the Command Byte for the intended operation.

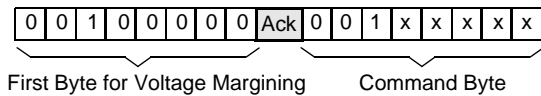
**Table 9. First Command Definitions**

First Command	Operation
001 00000	Voltage Margining
011 00000	Watchdog Programming

**VOLTAGE MARGINING OPERATION**

After starting the communication in Writing mode, the master sends the first command followed by the specific Command Byte to set the required voltage margining for either the LDO or the switcher (see [Figure 24](#)). To achieve a simultaneous set for both LDO and switcher, two specific commands must be issued in sequence after the first command, one for each supply.

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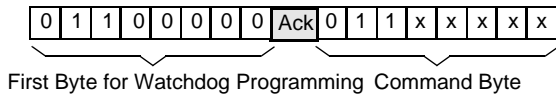
**Figure 24. Voltage Margining Programming (One Supply Only)**

**Note:** x bits, which set the voltage margining value are defined in [Table 8](#).

**WATCHDOG PROGRAMMING OPERATION**

For watchdog operation control, the master periodically sends a watchdog first command followed by a command byte selecting, or confirming, the watchdog period according to the options listed in [Table 8](#). See [Figure 25](#) for the watchdog timer programming command example.

The internal watchdog timer is turned ON by receiving a valid Watchdog Programming command (after receiving the Watchdog Programming First Command), and it is cleared each time the next Watchdog Programming command is written into the device, provided it arrives during the window open time. Thus, the Watchdog Programming command clears the timer and sets the new timing conditions at the same time. The Watchdog Programming First Command 01100000 sent twice shuts the timer OFF, and the watchdog function is disabled. Any other valid watchdog command turns the timer ON again.



**Figure 25. Watchdog Timer Programming**

**Note:** x bits, which set the watchdog timer value are defined in [Table 8](#), page [27](#).

**Communication Stop**

Only the master can terminate the data transfer by issuing a STOP condition. The slave waits for this condition to resume its initial state waiting for the next START condition (see [Figure 26](#)).

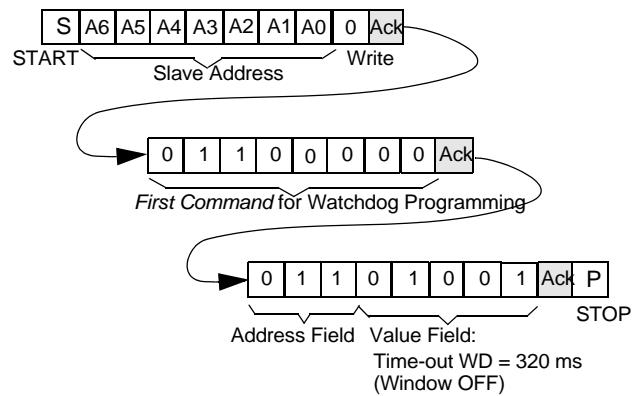
**COMPLETE DATA TRANSFER EXAMPLES**

The master device controlling the I<sup>2</sup>C bus always starts addressing a 34702 slave IC in writing mode (R/W = 0) to enable it to write a Command Byte just after receiving the

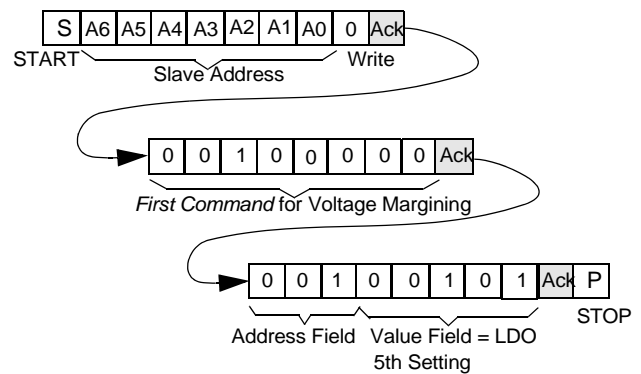
address acknowledge sent by 34702. I<sup>2</sup>C bus protocol defines this circumstance as a master-transmitter and slave-receiver configuration.

[Figure 27](#) illustrates a communication beginning with the slave address, the *first command* for voltage margining, and a third byte containing the address field 001 and the value field 00101 corresponding with the LDO fifth setting (LDO output voltage = +5% above its nominal value). If a simultaneous setting for switcher is needed, a fourth byte should be included before the STOP condition (P); for instance, 001 11100 to set the switcher in its twelfth setting (switcher output voltage = -5% below its nominal value) - see [Figure 28](#).

The example of data transfer setting the Watchdog timer is shown in the [Figure 26](#).



**Figure 26. Data Transfer Example - Watch Dog Timer Setting.**



**Figure 27. Data Transfer Example - LDO Voltage Margining**

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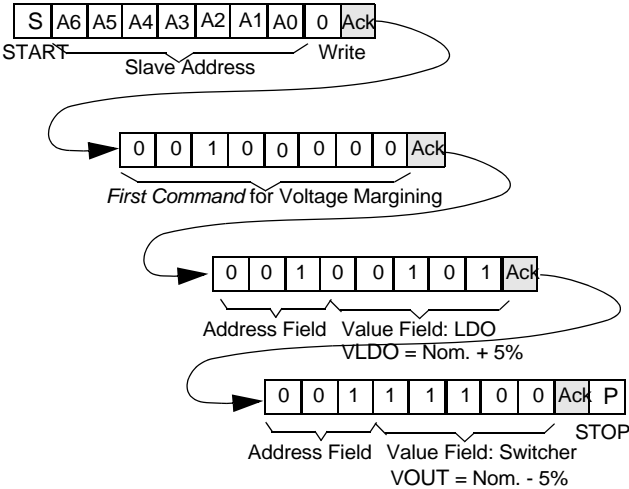


Figure 28. Data Transfer Example - LDO and Switcher Voltage Margining

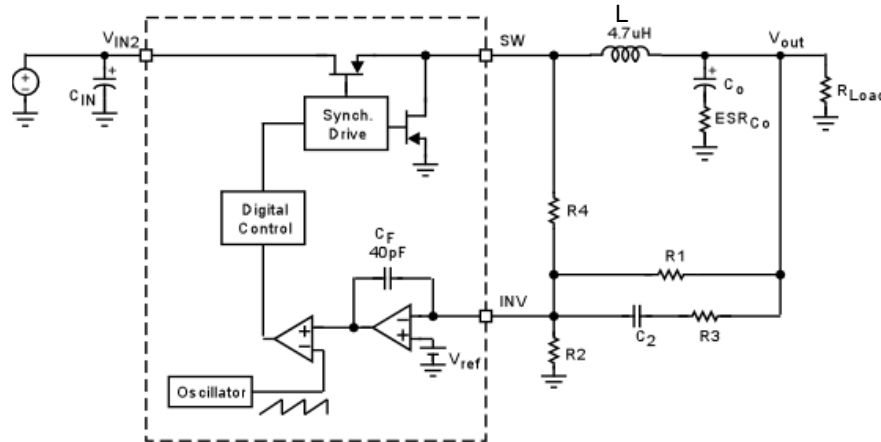
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## TYPICAL APPLICATIONS

### BUCK REGULATOR CONTROL CIRCUIT

The 34702 buck regulator utilizes a PWM Voltage Mode topology with Feed-Forward to achieve an excellent line and

load regulation. The control circuit block diagram is shown in [Figure 29](#).



**Figure 29. Buck Regulator Control Circuit**

The integrated 40 pF capacitor CF charged through the external resistor R4 provides the feed-forward ramp waveform, the amplitude of which is proportional to the input voltage, thus providing the feed-forward function.

[Figure 30](#) shows the Bode plot of the 34702 buck regulator control loop gain and phase versus frequency.

The first double pole on the Bode plot is created by the buck regulator output L-C filter, and its frequency can be calculated as:

$$f_{LC} = \frac{1}{2\pi\sqrt{C_O L}}$$

Where CO is the value of the buck output capacitor and L is the inductance value of the output filter inductor L.

The frequency of the compensating zero can be calculated as follows.

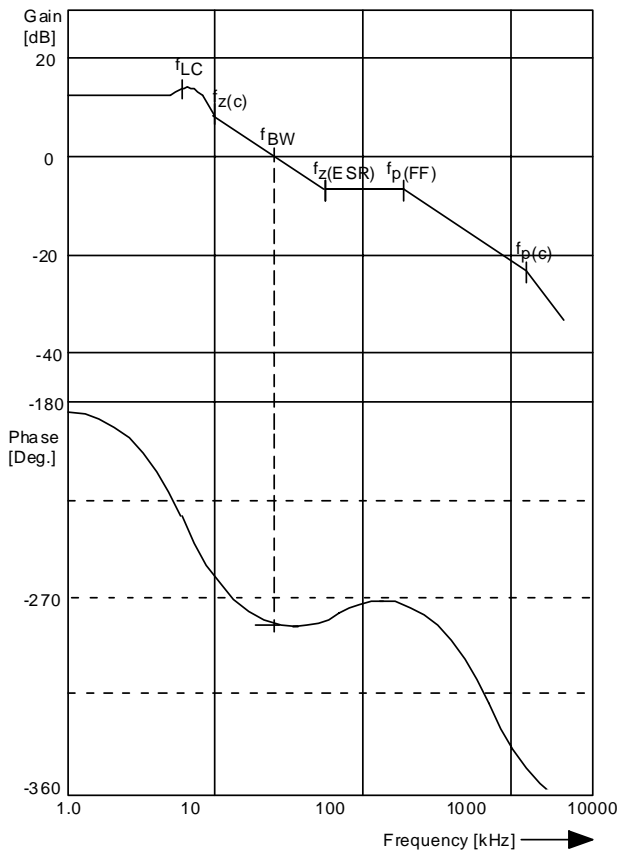
$$f_{z(c)} = \frac{1}{2\pi C_2 (R_1 + R_3)}$$

The Feed-Forward implemented by resistor R4 and integrated capacitor CF creates a pole in the overall loop transfer function, the frequency of which can be calculated from the following formula.

$$f_{p(FF)} = \frac{V_{IN}}{\frac{1}{f_{sw}} \times \frac{(V_{IN} - V_{Ref})}{R_4 C_F} + V_{m1}} \times \frac{1}{2\pi R_4 C_F}$$

Where VRef is the buck regulator reference voltage (VRef = 0.8 V typ.) at the INV pin, VIN is the buck regulator input voltage, Vm1 is the ramp generated by the internal ramp generator (Vm1 = 0.5 V typ.).

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**Figure 30. Buck Control Loop Bode Plot**

The frequency of the zero created by the ESR of the output capacitor  $C_O$  is calculated as:

$$f_{z(ESR)} = \frac{1}{2\pi C_O ESR}$$

Where  $C_O$  is the value of the buck regulator output capacitor, and ESR is the equivalent series resistance of the output capacitor.

The frequency of the compensating network pole can be calculated as follows:

$$f_{p(c)} = \frac{1}{2\pi C_2 \frac{R_1 R_3}{(R_1 + R_3)}}$$

The well designed and compensated buck regulator should yield at least 45 deg. phase margin  $\Phi_m$  of its overall loop as depicted in the [Figure 30](#), page [31](#).

### Selecting Buck Regulator Output Voltage

The 34702 buck regulator output voltage can be set by selecting the right value of the resistors  $R_1$ ,  $R_2$  and  $R_4$ , and can be determined from the following formula (see [Figure 29](#), page [30](#) for the component references):

$$R_2 = V_{Ref} \times \frac{1}{\frac{(V_O + I_O \times R_L) - V_{Ref}}{R_4} + \frac{V_O - V_{Ref}}{R_1}}$$

Where  $V_{Ref}$  is the buck regulator reference voltage ( $V_{Ref} = 0.8 \text{ V typ.}$ ) at the INV pin,  $V_O$  is the selected output voltage,  $I_O$  is the output load current,  $R_L$  is the DC resistance of the inductor  $L$ .

It is apparent that the buck regulator output voltage is affected by the voltage drop caused by the inductor serial resistance and the regulator output current. In those applications which do not require precise output voltage, setting the formula for calculating selected output voltage can be simplified as follows:

$$R_2 = V_{Ref} \times \frac{1}{(V_O - V_{Ref}) \times \frac{(R_1 + R_4)}{R_1 \times R_4}}$$

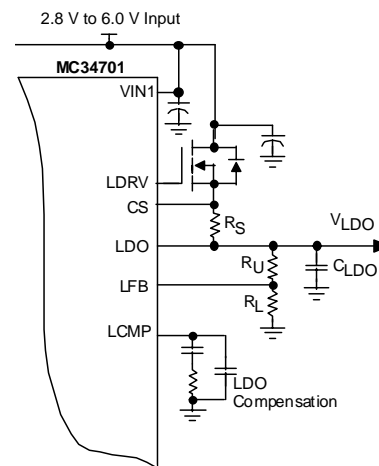
### Linear Regulator Output Voltage

The output voltage of the linear regulator (LDO) can be set by a simple resistor divider according to the following formula:

$$V_{LDO} = V_{Ref} \times \left(1 + \frac{R_U}{R_L}\right)$$

Where  $V_{Ref}$  is the linear regulator reference voltage ( $V_{Ref} = 0.8 \text{ V typ.}$ ) at the LFB pin,  $V_{LDO}$  is the LDO selected output voltage,  $R_U$  is the "upper" resistor of the LDO resistor divider,  $R_L$  is the "lower" resistor of the LDO resistor divider.

[Figure 31](#) describes the 34702 linear regulator circuit with the resistor divider  $R_U$ ,  $R_L$  setting the output voltage  $V_{LDO}$ .



**Figure 31. 34702 Linear Regulator Circuit**

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### Linear Regulator Current Limit

As described in the Linear Regulator Functional Description section, the current limit of the linear regulator can be adjusted by means of an external current sense resistor RS. The voltage drop caused by the regulator output current flowing through the current sense resistor RS is sensed between the LDO and the CS pins. When the sensed voltage exceeds 50 mV (typical), the current limit timer starts to time out while the control circuit limits the output current. If the overcurrent condition lasts for more than 10 ms, the linear regulator is shut off and turned on again after 100 ms. This type of operation provides equivalent protection to the analog "current foldback" operation.

It is important to keep in mind that the amount of capacitive load which can be supplied by the by the linear regulator is limited by the setting of the LDO current limit. During the power-up period, the linear regulator operates in the current limit, supplying the current into the load of the LDO, which includes all the capacitors connected to the regulator output. If the total amount load is so large that the regulator could not reach its regulation voltage in 10 ms during the power-up, it turns off and tries to power up again after 100 ms. This situation may lead to the power-up oscillations.

### Linear Regulator External MOSFET

The linear regulator uses an external N-channel power MOSFET to provide a pass element for the power path. The selection of the proper type of the external power MOSFET is critical for optimum performance and safe operation of the linear regulator.

The power MOSFET's threshold voltage, RDS(on), gate charge, capacitances and transconductance are important parameters for the stable operation of the linear regulator while the package of the power MOSFET determines the maximum power dissipation, and hence the maximum output current for the required input-to-output voltage drop. The power dissipation of the external MOSFET can be calculated from the simple formula:

$$P_{D(Q)} = I_{LDO} \times (V_{IN} - V_{LDO})$$

Where PD(Q) is the power MOSFET power dissipation  
VIN is the LDO input voltage,  
VLDO is the LDO output voltage,  
ILDO is the LDO output load current.

[Table 10](#) shows the recommended power MOSFET types for the 34702 linear regulator, their typical power dissipation, and thermal resistance junction-to-case.

**Table 10. Recommended Power MOSFETs**

Part No.	Package	Typ. PD	RthJ-C
IRL2703S	D2PAK	2.0 W	3.3 °C/W
MTD20N03HDL	DPAK	1.75 W*	1.67 °C/W

**NOTE:** Freescale does not assume liability, endorse, or warrant components from external manufacturers referenced in figures or tables. Although Freescale offers component recommendations, it is the customer's responsibility to validate their application.

\*When mounted to an FR4 using 0.5 sq.in. drain pad size

The maximum power dissipation is limited by the maximum operating junction temperature TJmax. The allowed power dissipation in the given application can be calculated from the following expression:

$$P_{D(Q)max} \leq \frac{T_{Jmax} - T_A}{R_{thJC} + R_{thCB} + R_{thBA}}$$

Where PD(Q)max is the power MOSFET maximum allowed dissipation,  
TJmax is the power MOSFET maximum operating junction temperature,  
TA is the ambient temperature,  
RthJC is the power MOSFET thermal resistance junction-to-case,  
RthCB is the thermal resistance case-to-board,  
RthBA is the thermal resistance board-to-ambient of the PC board.

### PCB Layout Considerations

As with any power application, the proper PCB layout plays a critical role in the overall power regulator performance. While good careful printed circuit board layout significantly improves regulation parameters and electromagnetic compatibility (EMC) performance of the switching regulator, poor layout practices can lead not only to significant degradation of regulation and EMC parameters but even to total dysfunction of the whole regulator IC.

Extreme care should be taken when laying out the ground of the regulator circuit. In order to avoid any inductive or capacitive coupling of the switching regulator noise into the sensitive analog control circuits, the noisy power ground and the clean quiet signal ground should be well separated on the printed circuit board, and connected only at one connection point. The power routing should be made by heavy traces or areas of copper. The power path and its return should be placed, if possible, atop each other on the different layers or opposite sides of the PC board. The switching regulator input and output capacitors should be physically placed very close to the power pins (VIN2, SW, PGND) of the 34702 switching regulator; and their ground pins, together with the 34702 power ground pins (PGND), should be connected by a single island of the power ground copper to create the "single-point" grounding. [Figure 32](#) illustrates the 34702 switching regulator grounding concept. The bootstrap capacitor Cb should be tightly connected to the integrated circuit as well.



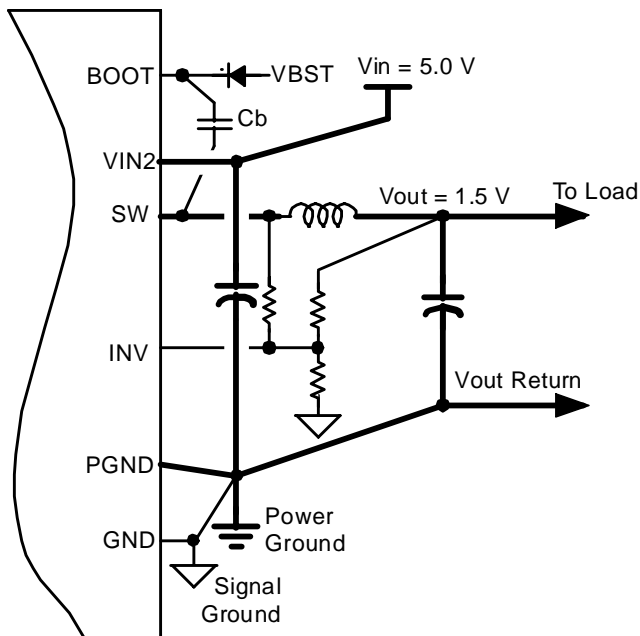
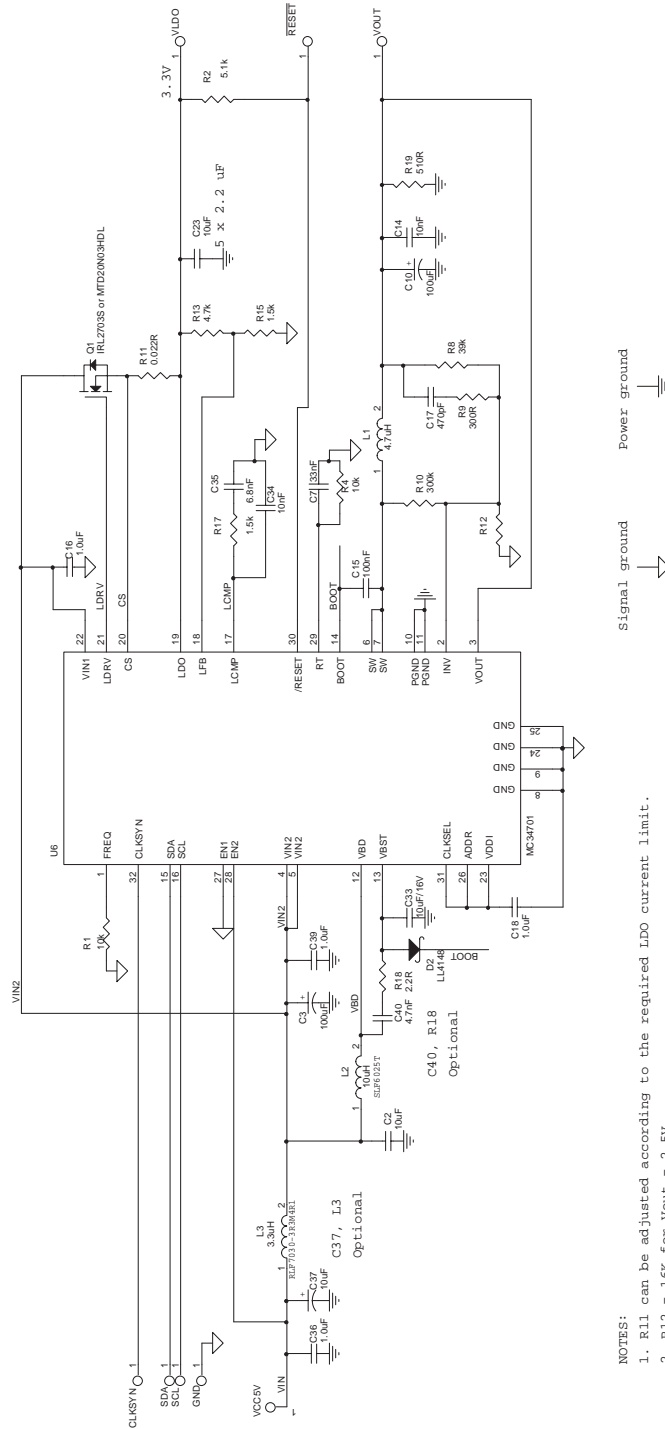
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Figure 32. 34702 Buck Regulator Layout

The same guidelines as those for the layout of the main switching buck regulator should be applied to the layout of the low power auxiliary boost regulator and to some extent, the power path of the linear regulator.



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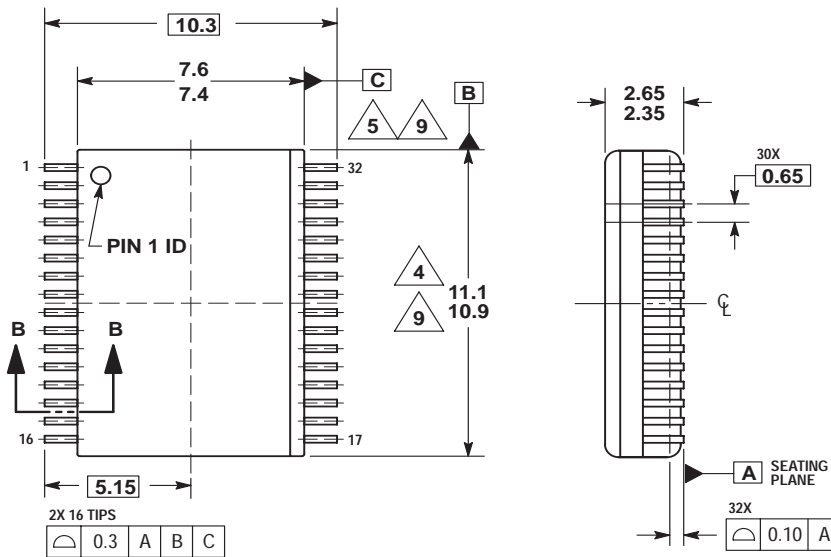
- NOTES:
1. R11 can be adjusted according to the required LDO current limit.
  2. R12 = 16k for Vout = 2.5V  
R12 = 27k for Vout = 1.8V.  
R12 = 36k for Vout = 1.5V.
  3. L1 = 4.7µH, DO3316P-472HC from Coilcraft  
or CDRH104R-4R7 from Sumida.
  4. L2 = 10µH, SLF6025T-100M/R3 from TDK  
or 1812PS-103M from Coilcraft.
  5. L3 = 3.3µH, RLF7030-3R3M4R1 from TDK
  6. C2 = 10µF/10V, ceramic capacitor .
  7. C3, C10 = 100µF/6.3V, 10THB100ML POSCAP capacitor from Sanyo.

Figure 34. 34702 Typical Application Circuit

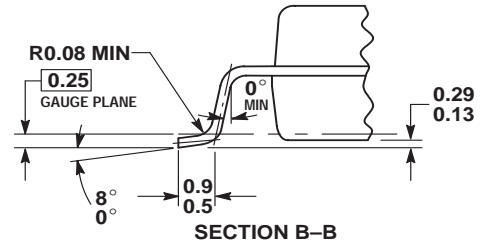
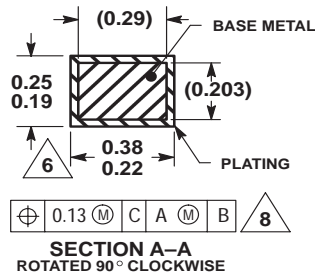
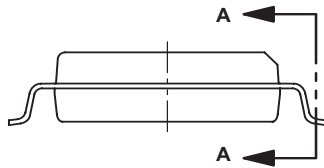
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# PACKAGE DIMENSIONS

**Important:** For the most current package revision, visit [www.freescale.com](http://www.freescale.com) and perform a "keyword" search for "98AARH99137A".



- NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 MM PER SIDE. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
  7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
  8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.3 MM FROM THE LEAD TIP.
  9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.



98AARH99137A  
CASE 1324-02  
ISSUE A

[查询"34702"供应商](#)**REVISION HISTORY**

REVISION	DATE	DESCRIPTION OF CHANGES
5.0	2/2006	<ul style="list-style-type: none"><li>• Changed Document Order No.</li></ul>
6.0	2/2007	<ul style="list-style-type: none"><li>• Updated to the current Freescale form and style.</li><li>• Changed the status from Advance Information to Final.</li><li>• Added <a href="#">Peak Package Reflow Temperature During Reflow</a> <sup>(2)</sup>, <sup>(3)</sup></li><li>• Added Notes <sup>(2)</sup> and <sup>(3)</sup></li></ul>

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