Timer

555

FEATURES

- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

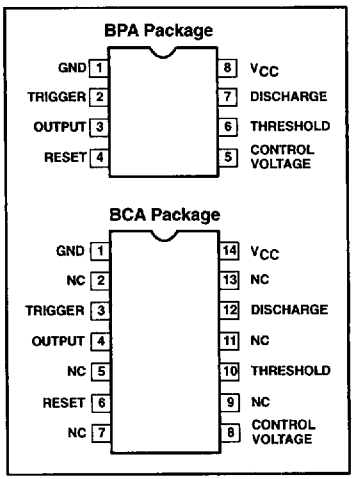
APPLICATIONS

- Precision timing
- Pulse generation

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

PIN CONFIGURATION

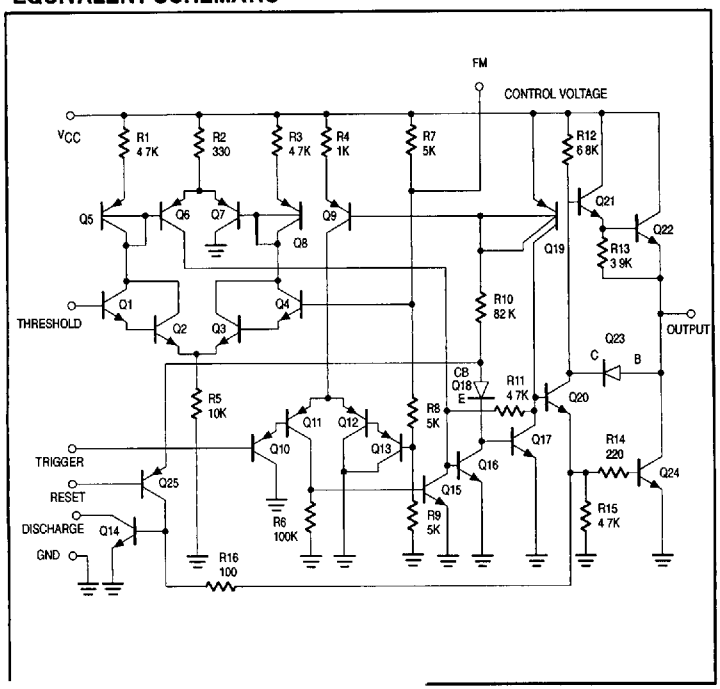


ORDERING INFORMATION

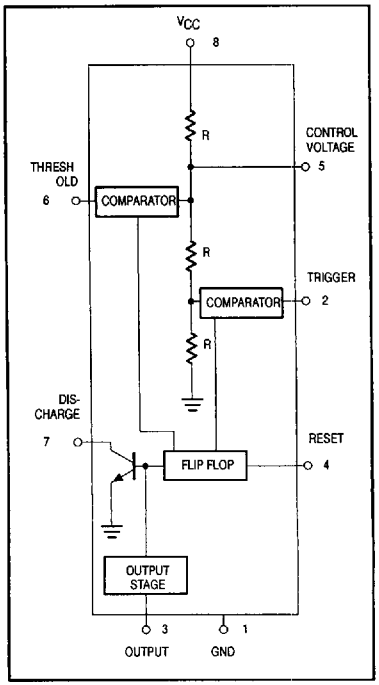
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
14-Pin Ceramic DIP	555/BCA	GDIP1-T14
8-Pin Ceramic DIP	555/BPA	GDIP1-T8

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

EQUIVALENT SCHEMATIC



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING[1]	UNIT
V_{CC}	Supply voltage	+18	V
P_D	Power dissipation	600	mW
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V to V_{CC} = +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	T_{amb} = +25°C			T_{amb} = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5		18	4.5		18	V
I_{CC}	Supply current (low state)[2]	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞		3 10	5 12			6 14	mA mA
t_M $\Delta t_M/\Delta T$ $\Delta t_M/\Delta V_S$	Timing error (monostable) Initial accuracy[3] Drift with temperature[7, 8] Drift with supply voltage	R_A = 2kΩ to 100kΩ C = 0.1µF		 0.5 0.05	 2.0 0.2			 2.5 100 0.25	 % ppm/°C %/V
t_A $\Delta t_A/\Delta T$ $\Delta t_A/\Delta V_S$	Timing error (astable) Initial accuracy[3] Drift with temperature[7] Drift with supply voltage[9]	R_A, R_B = 1kΩ to 100kΩ C = 0.1µF V_{CC} = 15V		 4 0.15	 6 0.6			 10.0 500 1.5	 % ppm/°C %/V
V_C	Control voltage level	V_{CC} = +15V V_{CC} = +5V	9.6 2.9	10.0 3.33	10.4 3.8	9.6 2.9		10.4 3.8	V V
V_{TH}	Threshold voltage	V_{CC} = +15V V_{CC} = +5V	9.4 2.7	10.0 3.33	10.6 4.0	9.4 2.4		10.6 4.0	V V
I_{TH}	Threshold current[4]	V_{TH} = 10.6V		0.1	0.25			0.35	mA
V_{TRIG} I_{TRIG} V_{RESET} I_{RESET} I_{RESET}	Trigger voltage Trigger current Reset voltage[5] Reset current Reset current	V_{CC} = +15V V_{CC} = +5V V_{TRIG} = 0V V_{RESET} = 0.4V V_{RESET} = 0V	4.8 1.45 0.3	5.0 1.67 0.5 -0.1 -0.4	5.2 1.9 0.9 1.0 -0.4 -1.0	4.5 1.5 0.1		5.5 2.2 2.0 1.3 -0.6 -1.2	V V µA V mA mA
V_{OL}	Output voltage (low)[10]	V_{CC} = +15V I_{SINK} = 10mA I_{SINK} = 50mA I_{SINK} = 100mA		0.1 0.4 2.0	0.15 0.5 2.2			0.25 0.70 2.6	V V V
		V_{CC} = +5V I_{SINK} = 8mA I_{SINK} = 5mA		0.1 0.05	0.25 0.2			0.43 0.38	V V
V_{OH}	Output voltage (high)[10]	V_{CC} = +15V I_{SOURCE} = 100mA V_{CC} = +5V I_{SOURCE} = 100mA	13.0 3.0	13.3 3.3		12.5 2.6			 V V
I_D	Discharge leakage current			20	100			500	nA

7AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, V_{CC} = +15V, unless otherwise specified.

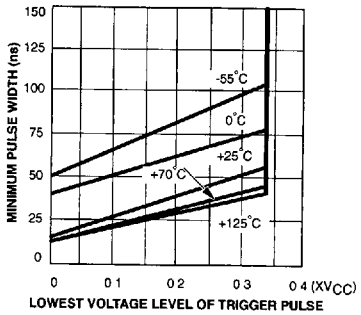
SYMBOL	PARAMETER	TEST CONDITIONS	T_{amb} = +25°C			T_{amb} = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{OFF}	Turn-off time[6, 7]	$V_{RESET} = V_{CC}$		0.5	2.0				µs
t_R t_F	Rise time of output[7] Fall time of output[7]			100 100	200 200				ns ns

NOTES:

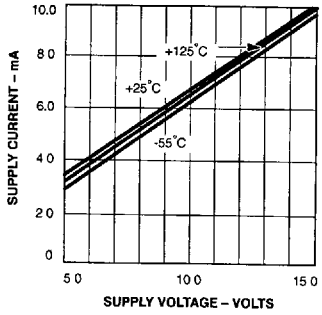
1. Operation beyond the limits in this table may impair the useful life of the device.
2. Supply current when output high typically 1mA less.
3. Tested at V_{CC} = +5V and V_{CC} = +15V.
4. This will determine the max. value of $R_A + R_B$, for 15V operation, the max. total R = 10MΩ, and for 5V operation, the max. total R = 3.4MΩ.
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to 0.8 X V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.
7. This parameter is guaranteed, but not tested.
8. Testing performed at R_A = 100kΩ only.
9. Testing performed at $R_A = R_S$ = 1kΩ only.
10. For long term static operation, derate the sink and source currents to 50mA maximum.

TYPICAL PERFORMANCE CHARACTERISTICS

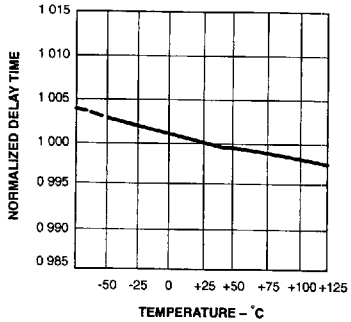
Minimum Pulse Width Required for Triggering



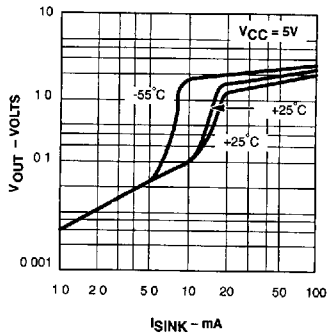
Supply Current vs Supply Voltage



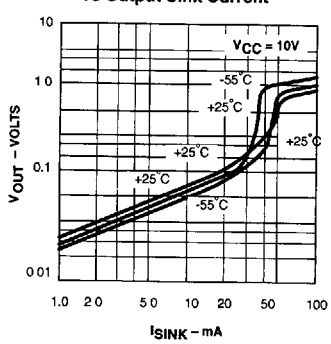
Delay Time vs Temperature



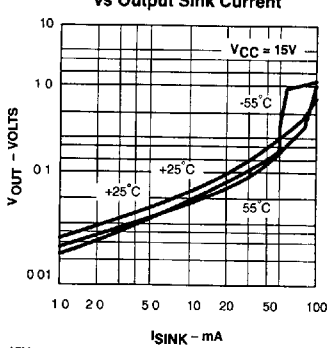
Low Output Voltage vs Output Sink Current



Low Output Voltage vs Output Sink Current

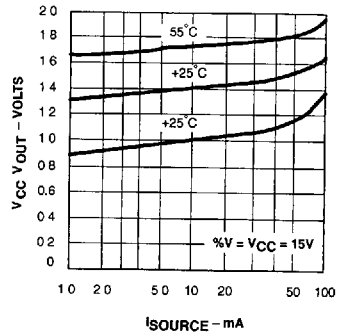


Low Output Voltage vs Output Sink Current

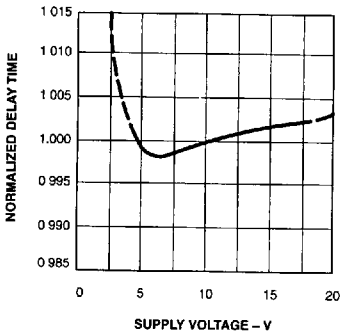


%V = VCC = 15V

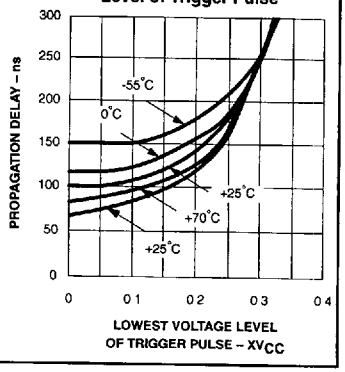
High Output Voltage Drop vs Output Source Current



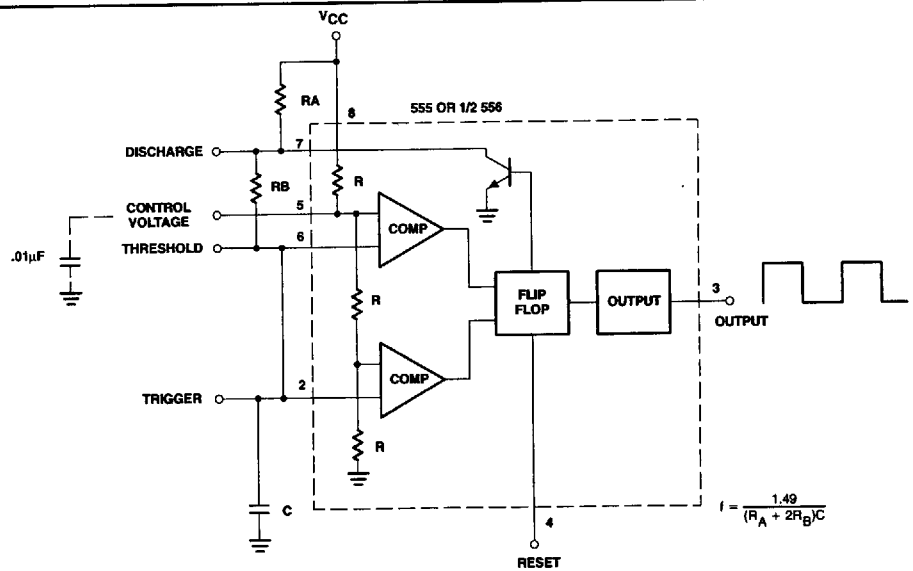
Delay Time vs Supply Voltage



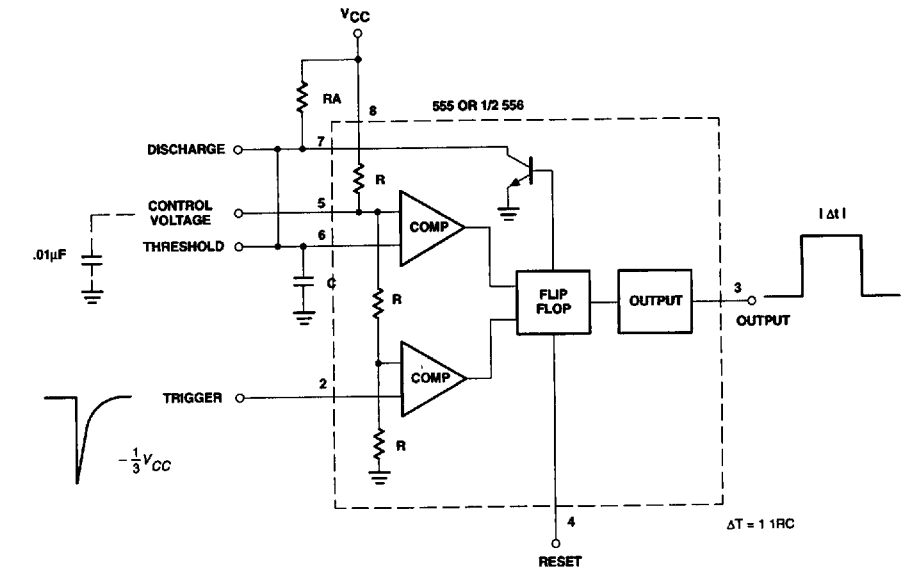
Propagation Delay vs Voltage Level of Trigger Pulse



TYPICAL APPLICATIONS



Astable Operation



Monostable Operation

TYPICAL APPLICATIONS (Continued)

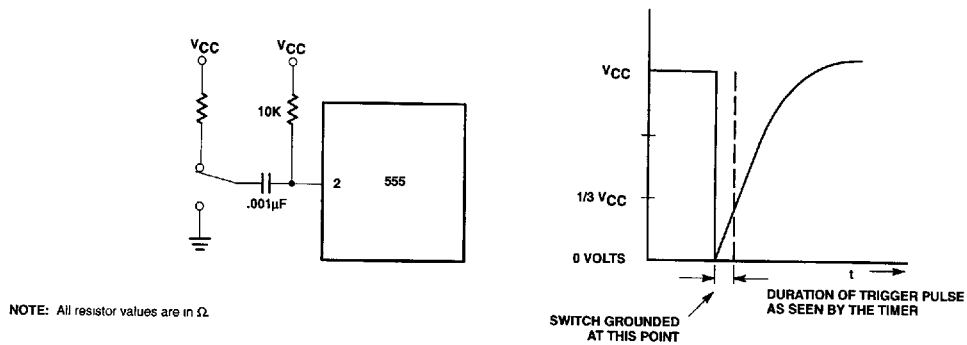


Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger (see Figure 1), a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle, the output will remain in a high state for the duration of the low trigger signal without regard to the threshold comparator state. This is due to the predominance of Q15 on the base of Q16, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q5, which turns on Q6. Current from Q6 turns on Q16 which turns Q17 off. This allows current from Q19 to turn on Q20 and Q24 to give an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q10 is on and turns on Q11 which turns on Q15. Q15 turns off Q16 and allows Q17 to turn on. This turns off current to Q20 and Q24, which results in output high. When the trigger is released, Q10 and Q11 shut off, Q15 turns off, Q16 turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.