# Four Output Clock Generator/Jitter Cleaner With Integrated Dual VCOs

## Check for Samples: CDCE62002

## FEATURES

- **Frequency Synthesizer With PLL/VCO and Partially Integrated Loop Filter**
- **Fully Configurable Outputs Including Frequency and Output Format**
- **Smart Input Multiplexer Automatically Switches Between one of two Reference Inputs.**
- **Multiple Operational Modes Include Clock Generation via Crystal, SERDES Startup Mode, Jitter Cleaning, and Oscillator Based Holdover Mode.**
- **Integrated EEPROM Determines Device Configuration at Power-up.**
- **Excellent Jitter Performance**
- **Integrated Frequency Synthesizer Including PLL, Multiple VCOs, and Loop Filter:**
  - **Full Programmability Facilitates Phase Noise Performance Optimization Enabling Jitter Cleaner Mode**
  - **Programmable Charge Pump Gain and Loop Filter Settings**
  - **Unique Dual-VCO Architecture Supports a Wide Tuning Range 1.750 GHz – 2.356 GHz.**
- **Universal Output Blocks Support up to 2 Differential, 4 Single-Ended, or Combinations of Differential or Single-Ended:**
  - **0.5 ps RMS (10 kHz to 20 MHz) Output Jitter Performance**
  - **Low Output Phase Noise: −130 dBc/Hz at 1 MHz offset, Fc = 491.52 MHz**
  - **Output Frequency Ranges From 10.94 MHz to 1.175 GHz in Synthesizer Mode**
  - **LVPECL, LVDS and LVCMOS**
  - **Independent Output Dividers Support Divide Ratios for 1,2,3,4,5,8,10,12,16,20,24 and 32.**

- **Flexible Inputs With Innovative Smart Multiplexer Feature:**
  - **Two Universal Differential Inputs Accept Frequencies from 1 MHz up to 500 MHz (LVPECL), 500 MHz (LVDS), or 250 MHz (LVCMOS).**
  - **One Auxiliary Input Accepts Crystals in the Range of 2MHz–42MHz**
  - **Clock Generator Mode Using Crystal Input**
  - **Smart Input Multiplexer can be Configured to Automatically Switch Between Highest Priority Clock Source Available Allowing for Fail-Safe Operation.**
- **Typical Power Consumption 750mW at 3.3V**
- **Integrated EEPROM Stores Default Settings; Therefore, the Device can Power up in a Known, Predefined State.**
- **Offered in QFN-32 Package**
- **ESD Protection Exceeds 2kV HBM**
- **Industrial Temperature Range –40°C to 85°C**

## APPLICATIONS

- **Data Converter and Data Aggregation Clocking**
- **Wireless Infrastructure**
- **Switches and Routers**
- **Medical Electronics**
- **Military and Aerospace**
- **Industrial**
- **Clock Generation and Jitter Cleaning**

---

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION

The CDCE62002 is a high performance clock generator featuring low output jitter, a high degree of configurability via a SPI interface, and programmable start up modes determined by on-chip EEPROM. Specifically tailored for clocking data converters and high-speed digital signals, the CDCE62002 achieves jitter performance under 0.5 ps RMS[1]. It incorporates a synthesizer block with partially integrated loop filter, a clock distribution block including programmable output formats, and an input block featuring an innovative smart multiplexer. The clock distribution block includes two individually programmable outputs that can be configured to provide different combinations of output formats (LVPECL, LVDS, LVCMOS). Each output can also be programmed to a unique output frequency (ranging from 10.94 MHz to 1.175 GHz[2]). If Both outputs are configured in single-ended mode (e.g., LVCMOS), the CDCE62002 supports up to four outputs. The input block includes one universal differential inputs which support frequencies up to 500 MHz and an auxiliary input that can be configured to connect to an external AT-Cut crystal via an on board oscillator block. The smart input multiplexer has two modes of operation, manual and automatic. In manual mode, the user selects the synthesizer reference via the SPI interface. In automatic mode, the input multiplexer will automatically select between the highest priority input clock available.
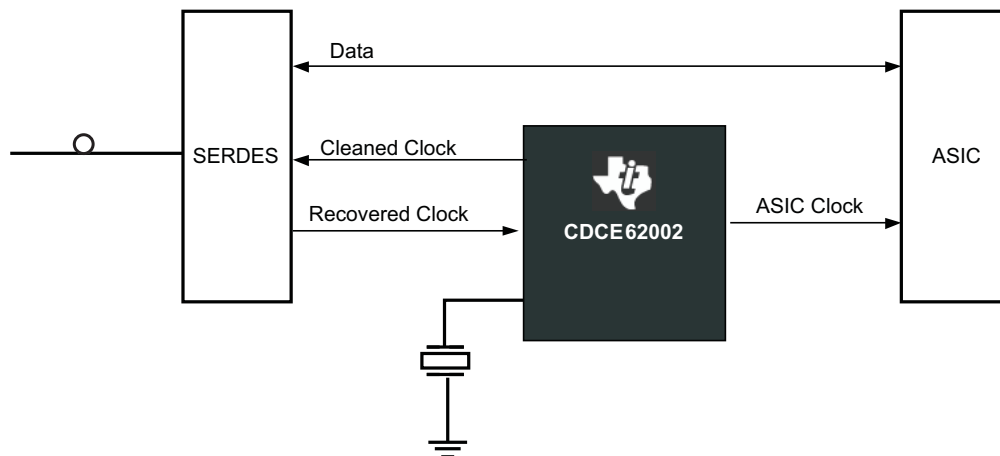


**Figure 1. CDCE62002 Application Example**

(1) 10 kHz to 20 MHz integration bandwidth.
(2) Frequency range depends on operational mode and output format selected.

Product Folder Link(s): *CDCE62002*

## DEVICE INFORMATION

## PIN FUNCTIONS

### Table 1. CDCE62002 Pin Functions[(1)]

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | QFN | | |
| VCC_OUT0 VCC_OUT1 | 9,12 13,16 | Power | 3.3V Supply for the Output Buffers. There is no internal connection between $V_{CC}$ and $AV_{CC}$. It is recommended, that each $V_{CC}$ uses its own supply filter. |
| VCC_PLLDIV | 22 | Power | 3.3V Supply Power for the PLL circuitry. |
| VCC_PLLD | 4 | Power | 3.3V Supply Power for the PLL circuitry. |
| VCC_PLLA | 28 | A. Power | 3.3V Supply Power for the PLL circuitry. |
| VCC_VCO | 24 | A. Power | 3.3V Supply Power for the VCO Circuitry. |
| VCC_IN | 31 | Power | 3.3V Supply Power for Input Buffer Circuitry |
| VCC_AUX | 1 | A. Power | 3.3V Supply Power for Crystal/Auxiliary Input Buffer Circuitry |
| GND_PLLDIV | 21 | Ground | Ground for PLL Divider circuitry. (short to GND) |
| GND | PAD | Ground | Ground is on Thermal PAD. See Layout recommendation |
| SPI_MISO | 7 | OD | 3-state LVCMOS Output that is enabled when SPI_LE is asserted low. It is the serial Data Output to the SPI bus interface. |
| SPI_LE | 18 | I | LVCMOS input, control Latch Enable for Serial Programmable Interface. *Note: The SPI_LE signal has to be high in order for the EEPROM to load correctly on the Rising edge of $\overline{PD}$.* The input has an internal 150-kΩ pull-up resistor |
| SPI_CLK | 17 | I | LVCMOS input, serial Control Clock Input for the SPI bus interface, with Hysteresis. |
| SPI_MOSI | 8 | I | LVCMOS input, Master Out Slave In as a serial Control Data Input to CDCE62002 for the SPI bus interface. |
| $\overline{PD}$ | 6 | I | $\overline{PD}$ or Power Down Pin is an active low pin and can be activated externally **or** via the corresponding Bit in SPI Register 2 |
| | | | In case of $\overline{PD}$ is asserted , the Device shuts Down and after $\overline{PD}$ goes high the EEPROM Loads into RAM and the VCO core re-starts calibration, PLL will try to relock and the Output dividers will get re-initiated. The LVPECL outputs are static low and high respectively and the LVCMOS outputs are all low or high if inverted. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". |
| | | | *Note: The SPI_LE signal has to be high in order for the EEPROM to load correctly into RAM on the Rising edge of $\overline{PD}$.* |
| AUX_IN | 2 | I | Auxiliary Input is a Crystal input pin that connect to an internal oscillator circuitry. |
| REF+ | 29 | I | Universal Input Buffer (LVPECL, LVDS, LVCMOS) positive input for the Reference Clock. |
| REF− | 30 | I | Universal Input Buffer (LVPECL, LVDS,) negative input for the Reference Clock. In case of LVCMOS signaling pull-down this pin. |
| PLL_LOCK | 32 | O | PLL Lock indicator |
| TESTSYNC | 19 | I | Test Point for Use for TI Internal $\overline{SYNC}$ Testing. |
| REG_CAP1 | 5 | Analog | Capacitor for the internal Regulator. Connect to a 10 μF Capacitor (Y5V) |
| REG_CAP2 | 27 | Analog | Capacitor for the internal Regulator. Connect to a 10 μF Capacitor (Y5V) |
| REG_CAP3 | 20 | Analog | Capacitor for the internal Regulator. Connect to a 10 μF Capacitor (Y5V) |
| REG_CAP4 | 23 | Analog | Capacitor for the internal Regulator. Connect to a 10 μF Capacitor (Y5V) |
| VBB | 3 | Analog | Capacitor for the internal termination Voltage. Connect to a 1 μF Capacitor (Y5V) |
| EXT_LFP | 25 | Analog | External Loop Filter Input Positive |
| EXT_LFN | 26 | Analog | External Loop Filter Input Negative. |
| U0P:U0N U1P:U1N | 11,10 15,14 | O | The Main outputs of **CDCE62002** are user definable and can be any combination of up to 2 LVPECL outputs, 2 LVDS outputs or up to 4 LVCMOS outputs. The outputs are selectable via SPI interface. The power-up setting is EEPROM configurable. |

(1)   NOTE: All VCC pins need to be connected for the device to operate properly.

## FUNCTIONAL DESCRIPTION
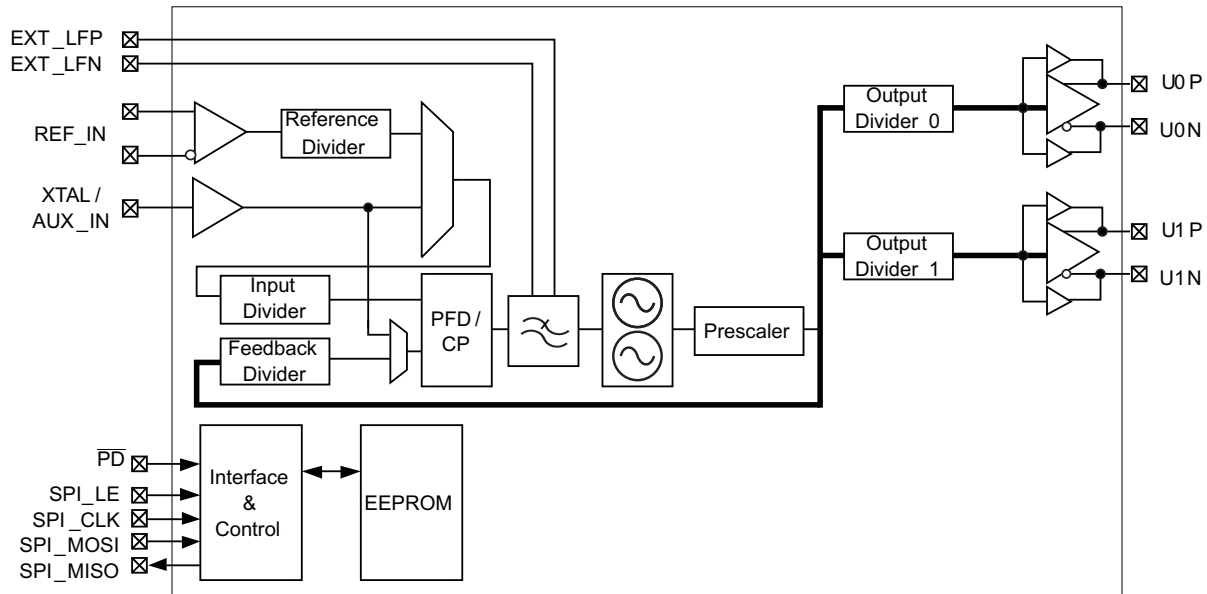


**Figure 2. CDCE62002 Block Diagram**

The CDCE62002 comprises of four primary blocks: the interface and control block, the input block, the output block, and the synthesizer block. In order to determine which settings are appropriate for any specific combination of input/output frequencies, a basic understanding of these blocks is required. The interface and control block determines the state of the CDCE62002 at power-up based on the contents of the on-board EEPROM. In addition to the EEPROM, the SPI port is available to configure the CDCE62002 by writing directly to the device registers after power-up. The input block selects which of the two input ports is available for use by the synthesizer block. The output block provides two separate clock channels that are fully programmable. The synthesizer block multiplies and filters the input clock selected by the input block.

**NOTE**
This Section of the data sheet provides a high-level description of the features of the CDCE62002 for purpose of understanding its capabilities. For a complete description of device registers and I/O, refer to the Device Configuration Section.

**Interface and Control Block**

The CDCE62002 is a highly flexible and configurable architecture and as such contains a number of registers so that the user may specify device operation. The contents of nine 28-bit wide registers implemented in static RAM determine device configuration at all times. On power-up, the CDCE62002 copies the contents of the EEPROM into the RAM and the device begins operation based on the default configuration stored in the EEPROM. Systems that do not have a host system to communicate with the CDCE62002 use this method for device configuration. After power-up, the host system may overwrite the contents of the RAM via the SPI (Serial Peripheral Interface) port. This enables the configuration and reconfiguration of the CDCE62002 during system operation. Finally, the device offers the ability to copy the contents of the RAM into EEPROM
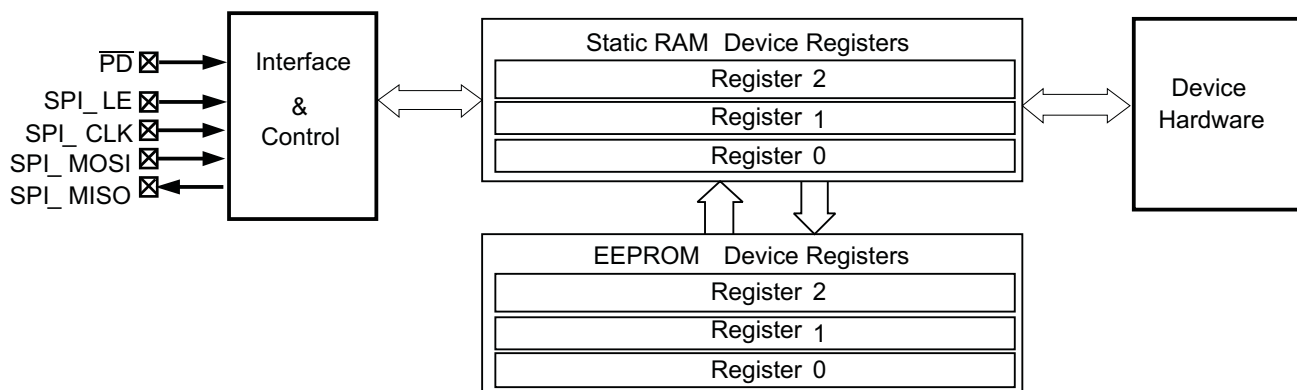


**Figure 3. CDCE62002 Interface and Control Block**

**Input Block**

The Input Block includes one Universal Input Buffer and an Auxiliary Input. The Input Block buffers the incoming signals and facilitates signal routing to the Internal Synthesizer Block via the smart multiplexer (called the Smart MUX). The CDCE62002 can divide the REF_IN signal via the dividers present on the inputs of the first stage of the Smart MUX.
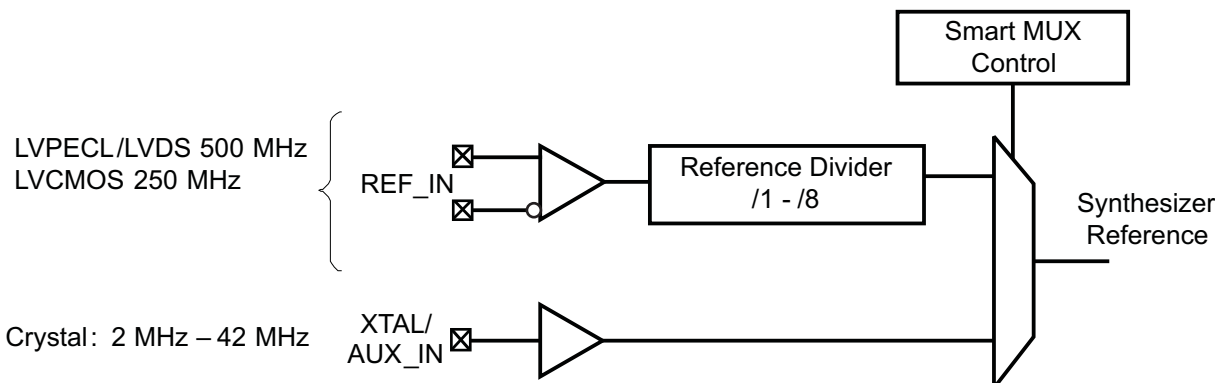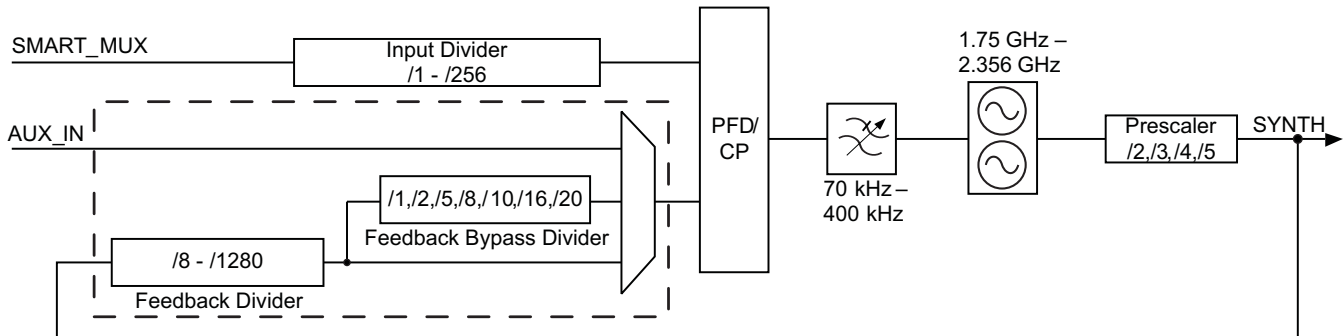


**Figure 4. CDCE62002 Input Block**
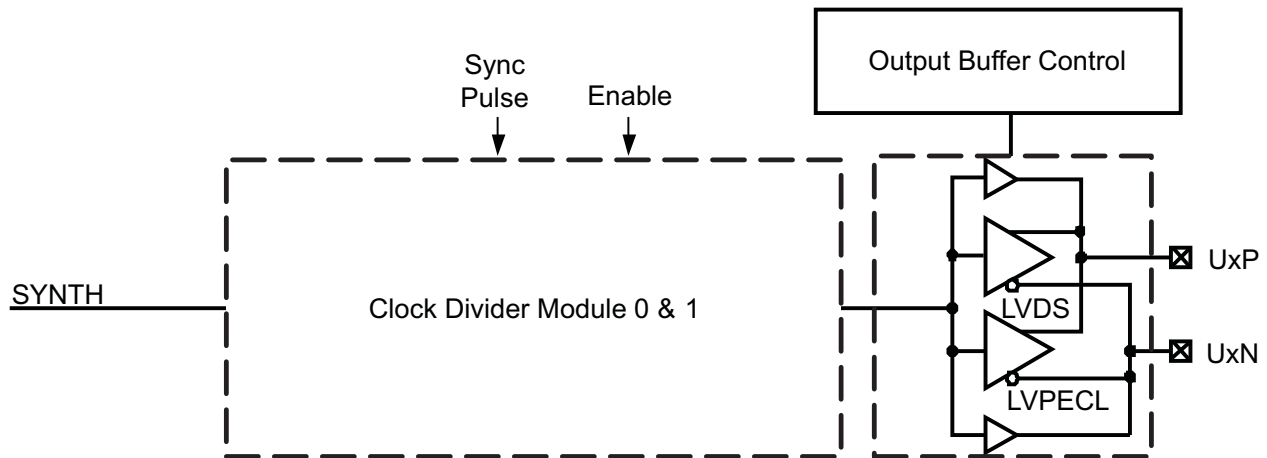
**Synthesizer Block**

Figure 5 presents a high-level overview of the Synthesizer Block on the CDCE62002. This block contains the Phase lock loop, internal loop filter and dual Voltage controlled oscillators. Only one VCO is selected at a time. The loop is closed after a Prescaler divider that feeds the output stage the feedback divider.

**Figure 5. CDCE62002 Synthesizer Block**

**Output Block**

Both identical output blocks incorporate a Clock Divider Module (CDM), and a universal output array buffer driver. If an individual clock output channel is not used, then the user should disable the CDM and Output Buffer for the unused channel to save device power. Each channel includes 4-bit in register "0" to control the divide ratio. The output divider supports divide ratios from divide by 1 (bypass the divider) 2,3,4,5,8,10,12,16,20,24 and 32.

**Figure 6. CDCE62002 Output Block**

## COMPUTING THE OUTPUT FREQUENCY

Figure 7 presents the block diagram of the CDCE62002 synthesizer highlighting the clock path for a single output. It also identifies the following regions containing dividers comprising the complete clock path:

- R: Is the Reference divider values.
- O: The output divider value (see Output Block for more details)
- I: The input divider value (see Synthesizer Block for more details)
- P: The Prescaler divider value (see Synthesizer Block of more details)
- F: The cumulative divider value of all dividers falling within the feedback divider (see Synthesizer Block for more details)
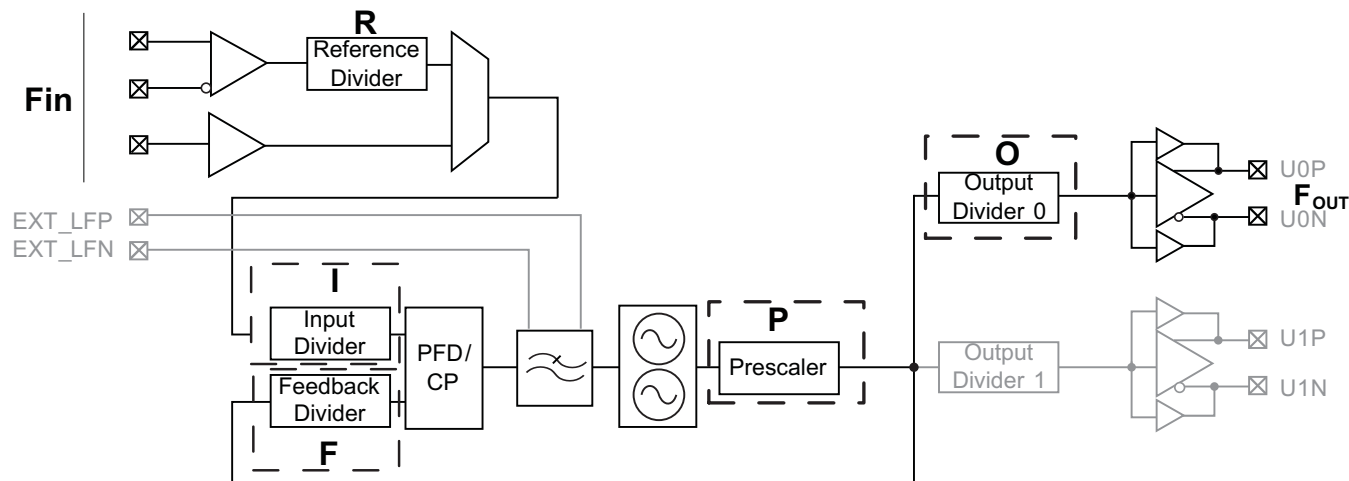


**Figure 7. CDCE62002 Clock Path – Synthesizer**

With respect to Figure 7, any output frequency generated by the CDCE62002 relates to the input frequency connected to the Synthesizer Block by the following equation:

$$F_{OUT} = F_{IN} \cdot \frac{F}{R \cdot I \cdot O} \tag{1}$$

Equation 1 holds true subject to the following constraints:

$$1.750 \text{GHz} < O \cdot P \cdot F_{OUT} < 2.356 \text{GHz} \tag{2}$$

And the comparison frequency $F_{COMP}$,

$$40.0 \text{ kHz} \leq F_{COMP} \leq 40 \text{ MHz}$$

Where:

$$F_{COMP} = \frac{F_{IN}}{R \cdot I} \tag{3}$$

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

| | VALUE / UNIT |
|---|---|
| Supply voltage range VCC[2] | −0.5 V to 4.6 V |
| Input voltage range, $V_I$ [3] | −0.5 V to VCC + 0.5 V |
| Output voltage range, $V_O$ [3] | −0.5 V to VCC + 0.5 V |
| Input Current ($V_I$ < 0, $V_I$ > VCC) | ±20 mA |
| Output current for LVPECL/LVCMOS Outputs (0 < $V_O$ < $V_{CC}$) | ±50 mA |
| Maximum junction temperature, $T_J$ | 125°C |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All supply voltages have to be supplied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## THERMAL CHARACTERISTICS

Package Thermal Resistance for QFN (RGZ) Package

| Airflow (lfm) | | $\theta_{JP}$ (°C/W) | $\theta$JA (°C/W) |
|---|---|---|---|
| 0 | JEDEC Compliant Board (3X3 VIAs on PAD) | 1.13 | 35 |
| 200 | JEDEC Compliant Board (3X3 VIAs on PAD) | 1.13 | 28.3 |
| 400 | JEDEC Compliant Board (3X3 VIAs on PAD) | 1.13 | 27.2 |

## PACKAGE

The CDCE62002 is packaged in a 32-Pin Lead Free "Green" Plastic Quad Flatpack Package with enhanced bottom thermal pad for heat dissipation. The Texas Instruments Package Designator is; RHB (S-PQFP-N32). Please refer to the Mechanical Data appendix at the end of this document for more information.

## ELECTRICAL CHARACTERISTICS

recommended operating conditions for the CDCE62002 Device for under the specified Industrial temperature range of −40°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Supply voltage, $V_{CC\_OUT}$, $V_{CC\_PLLDIV}$, $V_{CC\_PLLD}$, $V_{CC\_IN}$, and $V_{CC\_AUX}$ | | | 3 | 3.3 | 3.6 | V |
| Analog Supply Voltage, VCC_PLLA, & VCC_VCO | | | 3 | 3.3 | 3.6 | V |
| $P_{LVPECL}$ | REF at 30.72MHz Outputs are LVPECL | Output 1 = 491.52 MHz Output 2 = 245.76 MHz In case of LVCMOS Outputs (1) = 245.76MHz | | 850 | | mW |
| $P_{LVDS}$ | REF at 30.72MHz Outputs are LVDS | | | 750 | | mW |
| $P_{LVCMOS}$ | REF at 30.72MHz Outputs are LVCMOS | | | 800 | | mW |
| $P_{OFF}$ | REF at 30.72MHz | Dividers and Outputs are disabled | | 450 | | mW |
| $P_{PD}$ | | Device is Powered Down | | 40 | | mW |
| **DIFFERENTIAL INPUT MODE (REF_IN)** | | | | | | |
| Input amplitude, VINPP ($V_{IN+}$ − $V_{IN−}$) | | | 0.1 | | 1.3 | V |
| Common-mode input voltage, VIC | | | 1.0 | | $V_{CC}$−03 | V |
| $I_{IH}$ | Differential input current High (No internal Termination) | VI = VCC, VCC = 3.6 V | | | 20 | µA |
| $I_{IL}$ | Differential input current Low (No internal Termination) | VI = 0 V, VCC = 3.6 V | −20 | | | µA |
| Input Capacitance on REF_IN | | | | 3 | | pF |
| **CRYSTAL INPUT SPECIFICATIONS** | | | | | | |
| | Crystal Load Capacitance | | 8 | | 10 | pF |

(1) All typical values are at VCC = 3.3 V, temperature = 25°C.

Copyright © 2009–2010, Texas Instruments Incorporated

Product Folder Link(s): *CDCE62002*

## ELECTRICAL CHARACTERISTICS  (continued)

recommended operating conditions for the CDCE62002 Device for under the specified Industrial temperature range of –40°C to 85°C

| | PARAMETER | TEST CONDITIONS | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Equivalent Series Resistance (ESR) | | | | | 50 | Ω |
| **LVCMOS INPUT MODE (SPI_CLK,SPI_MOSI,SPI_LE,PD, REF_IN)** | | | | | | | |
| $V_{IL}$ | Low-level input voltage LVCMOS | | | 0 | | 0.3 VCC | V |
| $V_{IH}$ | High-level input voltage LVCMOS | | | 0.7 VCC | | VCC | V |
| $V_{IK}$ | LVCMOS input clamp voltage | VCC = 3 V, II = –18 mA | | | | –1.2 | V |
| $I_{IH}$ | LVCMOS input current VI = | VCC, VCC = 3.6 V | | | | 20 | µA |
| $I_{IL}$ | LVCMOS input (Except REF_IN) | VI = 0 V, VCC = 3.6 V | | –10 | | –40 | µA |
| $I_{IL}$ | LVCMOS input (REF_IN) | VI = 0 V, VCC = 3.6 V | | –10 | | 10 | µA |
| $C_I$ | Input capacitance (LVCMOS signals) | VI = 0 V or VCC 3 | | | 3 | | pF |
| **SPI OUTPUT (MISO) / PLL** | | | | | | | |
| $I_{OH}$ | High-level output current | VCC = 3.3 V, | $V_O$ = 1.65 V | | –30 | | mA |
| $I_{OL}$ | Low-level output current | VCC = 3.3 V, | $V_O$ = 1.65 V | | 33 | | mA |
| $V_{OH}$ | High-level output voltage for LVCMOS outputs | VCC = 3 V, | $I_{OH}$ = –100 µA | VCC–0.5 | | | V |
| $V_{OL}$ | Low-level output voltage for LVCMOS outputs | VCC = 3 V, | $I_{OH}$ = 100 µA | | | 0.3 | V |
| $C_O$ | Output capacitance o MISO | VCC = 3.3 V; $V_O$ = 0 V or VCC | | | 3 | | pF |
| $I_{OZH}$ | 3-state output current | $V_O$ = $V_{CC}$, $V_O$ = 0 V | | | 5 | | µA |
| $I_{OZL}$ | | | | | –5 | | µA |
| **EEPROM** | | | | | | | |
| EEcyc | Programming cycle of EEPROM | | | 100 | 1000 | | Cycles |
| EEret | Data retention | | | 10 | | | Years |
| **VBB ( INPUT BUFFER INTERNAL TERMINATION VOLTAGE REFERENCE)** | | | | | | | |
| $V_{BB}$ | Input termination voltage | IBB = –0.2 mA, Depending on the setting | | 1.2 | | 1.9 | V |
| **INPUT BUFFERS INTERNAL TERMINATION RESISTORS (REF_IN)** | | | | | | | |
| | Termination resistance | Single ended | | | 5 | | kΩ |
| **PHASE DETECTOR** | | | | | | | |
| $f_{CPmax}$ | Charge pump frequency | | | 0.04 | | 40 | MHz |

## ELECTRICAL CHARACTERISTICS (Continued)

recommended operating conditions for the CDCE62002 Device for under the specified Industrial temperature range of –40°C to 85°C
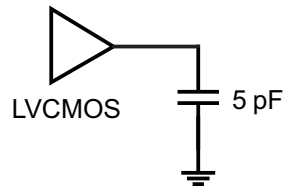
| PARAMETER | | TEST CONDITIONS | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **LVCMOS** | | | | | | | |
| $f_{clk}$ | Output frequency, see Figure below | Load = 5 pF to GND | | | | 250 | MHz |
| $V_{OH}$ | High-level output voltage for LVCMOS outputs | $V_{CC}$ = min to max | $I_{OH}$ = –100 μA | VCC–0.5 | | | V |
| $V_{OL}$ | Low-level output voltage for LVCMOS outputs | $V_{CC}$ = min to max | $I_{OL}$ = 100 μA | | | 0.3 | V |
| $I_{OH}$ | High-level output current | VCC = 3.3 V | VO = 1.65 V | | –30 | | mA |
| $I_{OL}$ | Low-level output current | VCC = 3.3 V | VO = 1.65 V | | 33 | | mA |
| $t_{sko}$ | Skew, output to output For Y0 to Y1 | Both Outputs set at 122.88 MHz, Reference = 30.72 MHz | | | 75 | | ps |
| $C_O$ | Output capacitance on Y0 to Y1 | VCC = 3.3 V; VO = 0 V or VCC | | | 5 | | pF |
| $I_{OZH}$ | Tristate LVCMOS output current | VO = VCC | | | 5 | | μA |
| $I_{OZL}$ | Tristate LVCMOS output current | VO = 0 V | | | -5 | | μA |
| $I_{OPDH}$ | Power Down output current | VO = VCC | | | | 25 | μA |
| $I_{OPDL}$ | Power Down output current | VO = 0 V | | | | 5 | μA |
| Duty cycle | LVCMOS | | | 45% | | 55% | |
| $t_{slew-rate}$ | Output rise/fall slew rate | | | 3.6 | 5.2 | | V/ns |

(1)   All typical values are at VCC = 3.3 V, temperature = 25°C.

LVCMOS          5 pF

## ELECTRICAL CHARACTERISTICS (Continued)

recommended operating conditions for the CDCE62002 Device for under the specified Industrial temperature range of –40°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVDS OUTPUT** | | | | | | |
| $f_{clk}$ | Output frequency | Configuration Load (see Figure below) | 0 | | 800 | MHz |
| $|V_{OD}|$ | Differential output voltage | $R_L = 100\ \Omega$ | 270 | | 550 | mV |
| $\Delta V_{OD}$ | LVDS VOD Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | –40°C to 85°C | | 1.24 | | V |
| $\Delta V_{OS}$ | VOS Magnitude Change | | | 40 | | mV |
| | Short Circuit Vout+ to Ground | VOUT = 0 | | | 27 | mA |
| | Short Circuit Vout- to Ground | VOUT = 0 | | | 27 | mA |
| $t_{sk(o)}$ | Skew, output to output For Y0 to Y1 | Both Outputs set at 122.88 MHz Reference = 30.72 MHz | | 10 | | ps |
| $C_O$ | Output capacitance on Y0 to Y1 | VCC = 3.3 V; VO = 0 V or VCC | | 5 | | pF |
| $I_{OPDH}$ | Power Down output current | VO= $V_{CC}$ | | | 25 | µA |
| $I_{OPDL}$ | Power Down output current | VO= 0 V | | | 5 | µA |
| | Duty Cycle | | 45% | | 55% | |
| $t_r / t_f$ | Rise and fall time | 20% to 80% of Voutpp | 110 | 160 | 190 | ps |
| **LVCMOS-TO-LVDS** | | | | | | |
| $t_{skP\_C}$ | Output skew between LVCMOS and LVDS outputs | VCC/2 to Crosspoint | 1.4 | 1.7 | 2.0 | ns |

(1)  All typical values are at VCC = 3.3 V, temperature = 25°C.
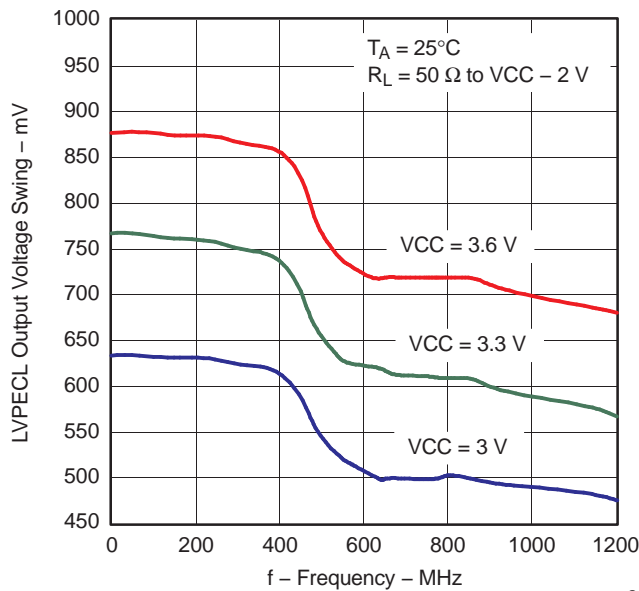
LVDS DC Termination Test

## ELECTRICAL CHARACTERISTICS (Continued)

recommended operating conditions for the CDCE62002 Device for under the specified Industrial temperature range of –40°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVPECL OUTPUT** | | | | | | |
| $f_{clk}$ | Output frequency, | Configuration Load (see Figure below) | 0 | | 1175 | MHz |
| $V_{OH}$ | LVPECL high-level output voltage | Load | VCC –1.1 | | VCC –0.88 | V |
| $V_{OL}$ | LVPECL low-level output voltage | Load | VCC –2.02 | | VCC –1.48 | V |
| \|VOD\| | Differential output voltage | | 510 | | 870 | mV |
| $t_{sko}$ | Skew, output to output For Y0 to Y1 | Both Outputs set at 122.88 MHz | | 15 | | ps |
| CO | Output capacitance on Y0 to Y1 | VCC = 3.3 V; VO = 0 V or VCC | | 5 | | pF |
| $I_{OPDH}$ | Power Down output current | VO= $V_{CC}$ | | | 25 | μA |
| $I_{OPDL}$ | Power Down output current | VO= 0 V | | | 5 | μA |
| | Duty Cycle | | 45% | | 55% | |
| $t_r / t_f$ | Rise and fall time | 20% to 80% of Voutpp | 55 | 75 | 735 | ps |
| **LVDS-TO- LVPECL** | | | | | | |
| $t_{skP\_C}$ | Output skew between LVDS and LVPECL outputs | Crosspoint to Crosspoint | 130 | 200 | 280 | ps |
| **LVCMOS-TO- LVPECL** | | | | | | |
| $t_{skP\_C}$ | Output skew between LVCMOS and LVPECL outputs | VCC/2 to Crosspoint | 1.6 | 1.8 | 2.2 | ns |
| **LVPECL Hi-PERFORMANCE OUTPUT** | | | | | | |
| $V_{OH}$ | LVPECL high-level output voltage | Load | VCC –1.11 | | VCC –0.91 | V |
| $V_{OL}$ | LVPECL low-level output voltage | Load | VCC –2.06 | | VCC –1.84 | V |
| \|VOD\| | Differential output voltage | | 670 | | 950 | mV |
| $t_r / t_f$ | Rise and fall time | 20% to 80% of Voutpp | 55 | 75 | 135 | ps |

(1)    All typical values are at VCC = 3.3 V, temperature = 25°C.



LVPECL AC Termination Test    LVPECL DC Termination Test

Copyright © 2009–2010, Texas Instruments Incorporated
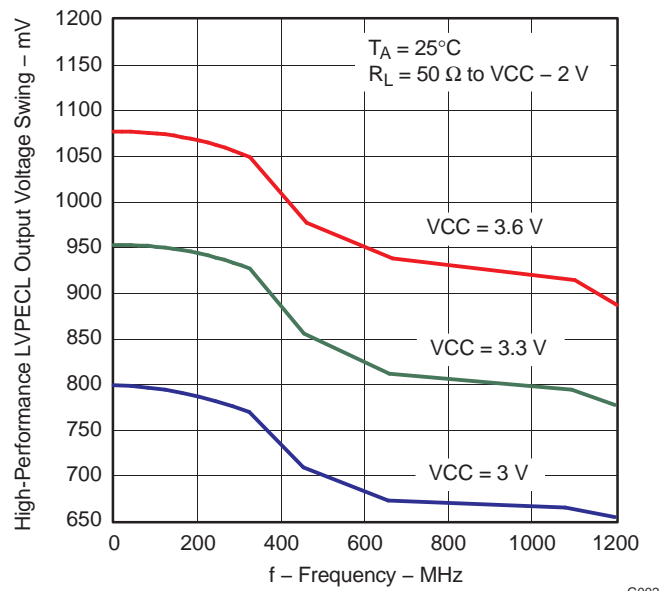
Product Folder Link(s): *CDCE62002*
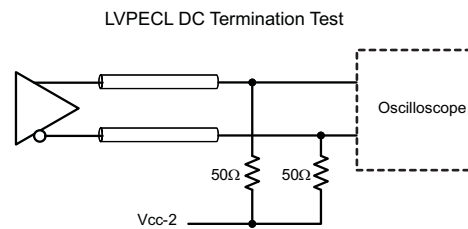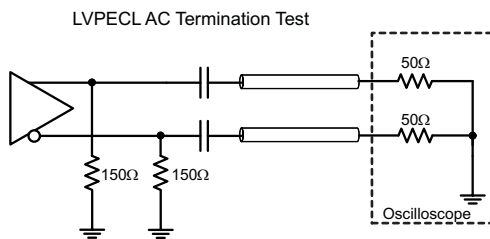
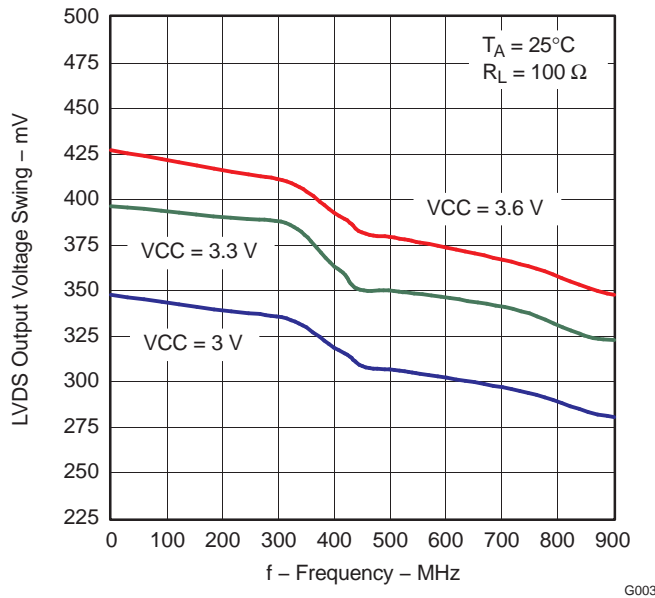**LVPECL OUTPUT VOLTAGE SWING**
**vs**
**FREQUENCY**



Figure 8.

**HIGH-PERFORMANCE LVPECL**
**OUTPUT VOLTAGE SWING**
**vs**
**FREQUENCY**



Figure 9.

**LVDS OUTPUT VOLTAGE SWING**
**vs**
**FREQUENCY**



Figure 10.

**LVCMOS OUTPUT VOLTAGE SWING**
**vs**
**FREQUENCY**



Figure 11.

Product Folder Link(s): CDCE62002
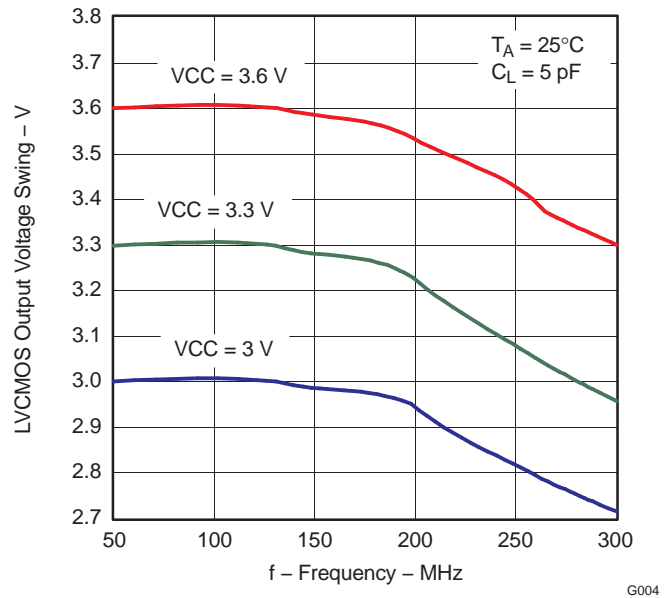
## TIMING REQUIREMENTS

over recommended ranges of supply voltage, load and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **REF_IN REQUIREMENTS** | | | | | |
| $f_{REF – Diff\ IN-DIV}$ | Maximum clock frequency applied to reference divider when (Register 0 Bit 9 = 1) (Reg 0 RAM bit 9 = 1) | | | 500 | MHz |
| $f_{REF – Diff\ REF\_DIV}$ | Maximum clock frequency applied to reference divider when (Register 0 Bit 9 = 0) (Reg 0 RAM bit 9 = 0) | | | 250 | MHz |
| $f_{REF– Single}$ | For Single ended Inputs ( LVCMOS) on REF_IN | | | 250 | MHz |
| Duty Cycle Single | Duty cycle of REF_IN at $V_{CC}$ / 2 | 40% | | 60% | |
| Duty Cycle Diff | Duty cycle of REF_IN at $V_{CC}$ / 2 | 40% | | 60% | |
| **AUXILARY_IN REQUIREMENTS** | | | | | |
| $f_{REF – Crystal}$ | AT-Cut Crystal Input | 2 | | 42 | MHz |
| **$\overline{PD}$ REQUIREMENTS** | | | | | |
| $t_r$ / $t_f$ | Rise and fall time of the $\overline{PD}$ signal from 20% to 80% of $V_{CC}$ | | | 4 | ns |

## PHASE NOISE ANALYSIS

### Table 2. Phase Noise for 30.72MHz External Reference

| Phase Noise Specifications under following configuration: VCO = 1966.08 MHz, REF_IN = 30.72MHz, PFD Frequency = 30.72MHz, Charge Pump Current = 1.5mA Loop BW = 400kHz at 3.3V and 25°C. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **PHASE NOISE AT** | **Reference 30.72MHz** | **LVPECL-HP 491.52MHz** | **LVPECL 491.52MHz** | **LVDS-HP 491.52MHz** | **LVDS 491.52MHz** | **LVCMOS-HP 122.88MHz** | **LVCMOS 122.88MHz** | **UNIT** |
| 10Hz | −108 | −84 | −84 | −85 | −85 | −97 | −97 | dBc/Hz |
| 100Hz | −130 | −98 | −98 | −98 | −97 | −110 | −111 | dBc/Hz |
| 1kHz | −134 | −106 | −106 | −106 | −106 | −118 | −118 | dBc/Hz |
| 10kHz | −152 | −118 | −118 | −118 | −118 | −130 | −130 | dBc/Hz |
| 100kHz | −156 | −121 | −121 | −121 | −121 | −133 | −133 | dBc/Hz |
| 1MHz | −157 | −131 | −131 | −130 | −130 | −143 | −142 | dBc/Hz |
| 10MHz | — | −146 | −146 | −146 | −145 | −152 | −151 | dBc/Hz |
| 20MHz | — | −146 | −146 | −146 | −145 | −152 | −151 | dBc/Hz |
| Jitter(RMS) 10k~20MHz | 195 (10k~20Mhz) | 319 | 316 | 332.4 | 332.2 | 366.5 | 372.1 | fs |

### Table 3. Phase Noise for 25MHz Crystal Reference

| Phase Noise Specifications under following configuration: VCO = 2000.00 MHz, AUX_IN -REF = 25.00MHz, PFD Frequency = 25.00MHz, Charge Pump Current = 1.5mA Loop BW = 400kHz 3.3V and 25°C. | | | | | |
|---|---|---|---|---|---|
| **Phase Noise at** | **Reference 25.00MHz** | **LVPECL-HP 500.00MHz** | **LVDS-HP 250.00MHz** | **LVCMOS-HP 125.00MHz** | **UNIT** |
| 10Hz | — | −72 | −72 | −79 | dBc/Hz |
| 100Hz | — | −97 | −97 | −103 | dBc/Hz |
| 1kHz | — | −111 | −111 | −118 | dBc/Hz |
| 10kHz | — | −120 | −120 | −126 | dBc/Hz |
| 100kHz | — | −124 | −124 | −130 | dBc/Hz |
| 1MHz | — | −136 | −136 | −142 | dBc/Hz |
| 10MHz | — | −147 | −147 | −151 | dBc/Hz |
| 20MHz | — | −148 | −148 | −151 | dBc/Hz |
| Jitter(RMS) 10k~20MHz | — | 426 | 426 | 443 | fs |

Product Folder Link(s): CDCE62002

CDCE62002

# OUTPUT TO OUTPUT ISOLATION

## Measurement Method

1. Connect output 1 to the phase noise and Spectrum analyzer.
2. Measure spurious on Outputs 1.
3. Enable aggressor channel 0
4. Measure spurious on Output 1
5. The difference between the spurious levels of Outputs 1 before and after enabling the aggressor channel determine the output-to-output isolation performance recorded.

### Table 4. Output to Output Isolation

|  |  |  | WORST CASE SPUR | UNIT |
|---|---|---|---|---|
| The Output to Output Isolation was tested at 3.3V supply and 25°C ambient temperature (Default Configuration): | | | | |
| **Output 1** | Measured Channel | **In LVDS Signaling at 125MHz** | -70 | dB |
| *Output 0* | *Aggressor Channel* | *LVPECL 156.25MHz* | | |

## SPI CONTROL INTERFACE TIMING
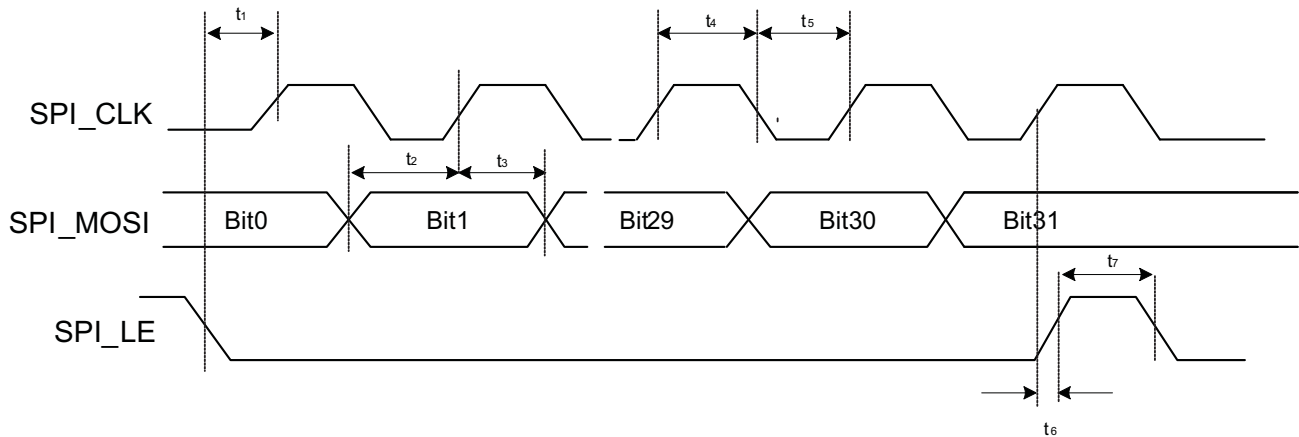


**Figure 12. Timing Diagram for SPI Write Command**
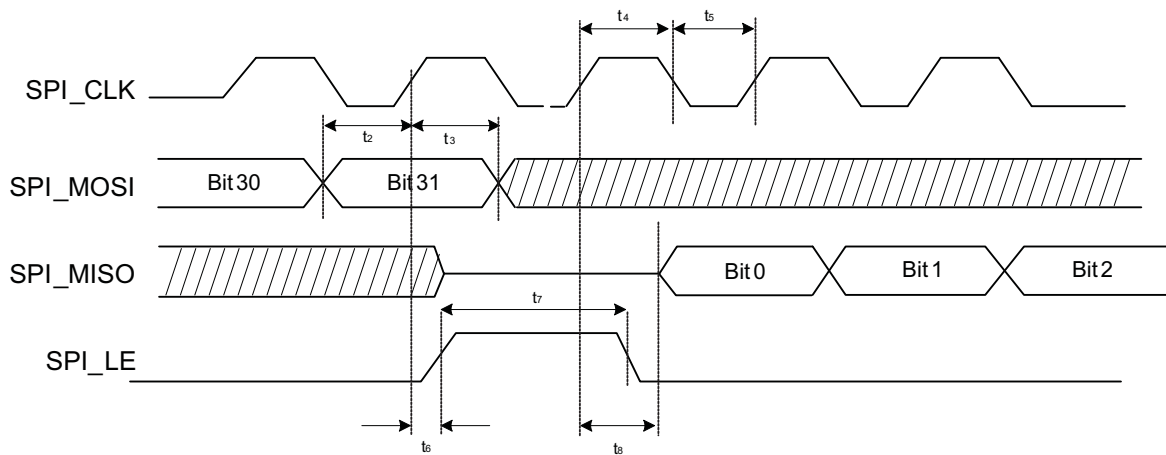


**Figure 13. Timing Diagram for SPI Read Command**

**Table 5. SPI Bus Timing Characteristics**

| SPI BUS TIMINGS | | | | | |
|---|---|---|---|---|---|
| PARAMETER | | MIN | TYP | MAX | UNIT |
| $f_{Clock}$ | Clock Frequency for the SPI_CLK | | | 20 | MHz |
| $t_1$ | SPI_LE to SPI_CLK setup time | 10 | | | ns |
| $t_2$ | SPI_MOSI to SPI_CLK setup time | 10 | | | ns |
| $t_3$ | SPI_MOSI to SPI_CLK hold time | 10 | | | ns |
| $t_4$ | SPI_CLK high duration | 25 | | | ns |
| $t_5$ | SPI_CLK low duration | 25 | | | ns |
| $t_6$ | SPI_CLK to SPI_LE Setup time | 10 | | | ns |
| $t_7$ | SPI_LE Pulse Width | 20 | | | ns |
| $t_8$ | SPI_MISO to SPI_CLK Data Valid (First Valid Bit after LE) | 10 | | | ns |

Product Folder Link(s): *CDCE62002*

## DEVICE CONFIGURATION

The Functional Description Section described four different functional blocks contained within the CDCE62002. Figure 14 depicts these blocks along with a high-level functional block diagram of the circuit elements comprising each block. The balance of this section focuses on a detailed discussion of each functional block from the perspective of how to configure them.
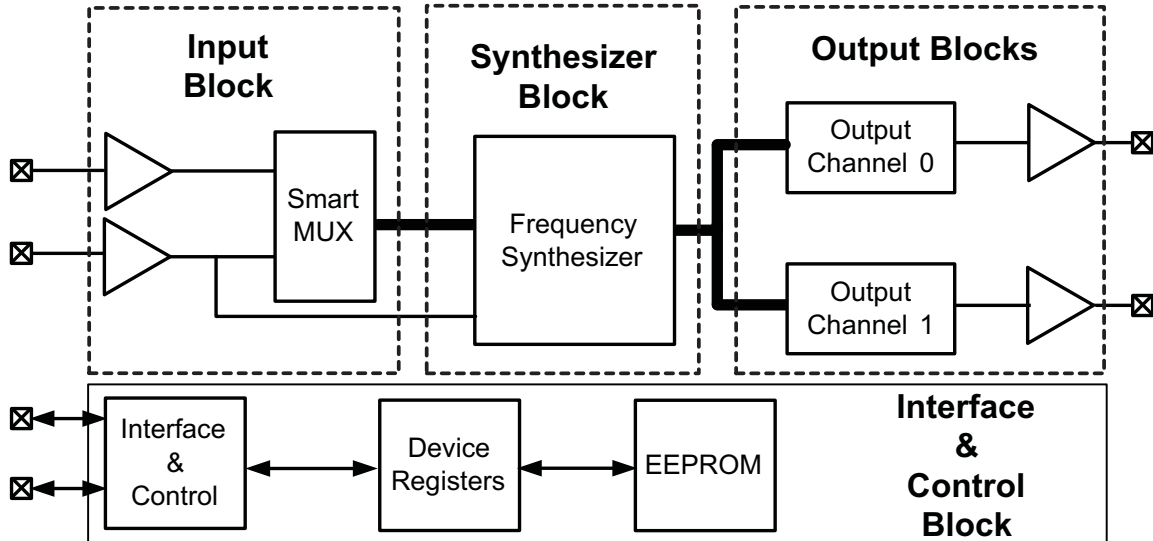


**Figure 14. CDCE62002 Circuit Blocks**

## INTERFACE and CONTROL BLOCK

The Interface and Control Block includes a SPI interface, four control pins, a non-volatile memory array in which the device stores default configuration data, and an array of device registers implemented in Static RAM. This RAM, also called the device registers, configures all hardware within the CDCE62002.
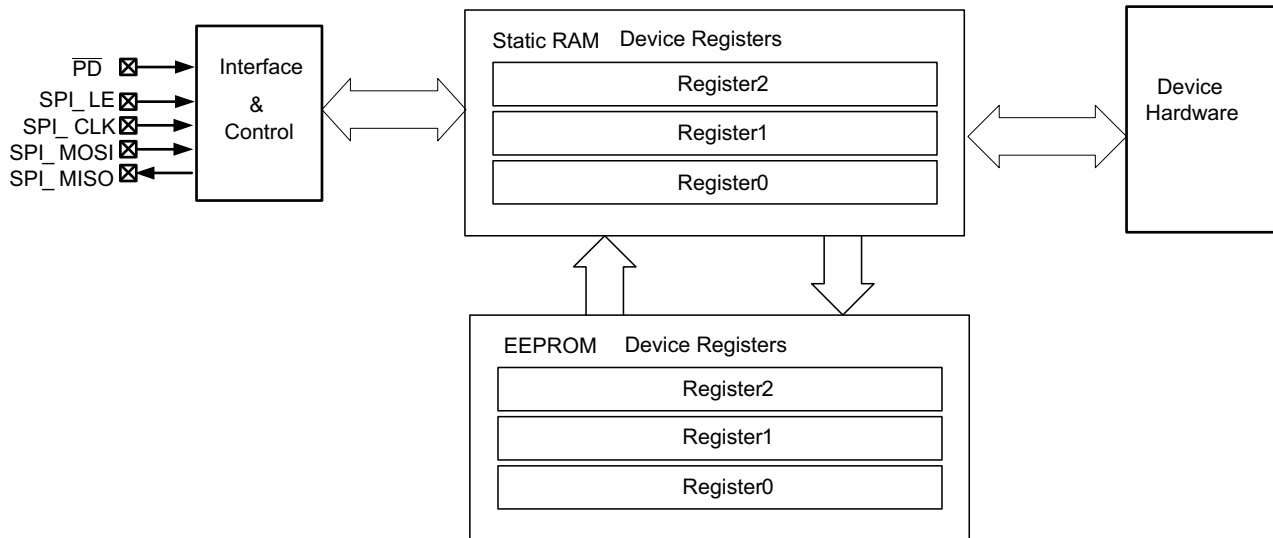
Figure 15. CDCE62002 Interface and Control Block

## SPI (Serial Peripheral Interface)

The serial interface of CDCE62002 is a simple bidirectional SPI interface for writing and reading to and from the device registers. It implements a low speed serial communications link in a master/slave topology in which the CDCE62002 is a slave. The SPI consists of four signals:

- **SPI_CLK:** Serial Clock (Output from Master) – the CDCE62002 clocks data in and out on the rising edge of SPI_CLK. Data transitions therefore occur on the falling edge of the clock.
- **SPI_MOSI:** Master Output Slave Input (Output from Master).
- **SPI_MISO:** Master Input Slave Output (Output from Slave)
- **SPI_LE:** Latch Enable (Output from Master). The falling edge of SPI_LE initiates a transfer. If SPI_LE is high, no data transfer can take place.

The CDCE62002 implements data fields that are 28-bits wide. In addition, it contains 3 registers, each comprising a 28 bit data field. Therefore, accessing the CDCE62002 requires that the host program append a 4-bit address field to the front of the data field as follows:
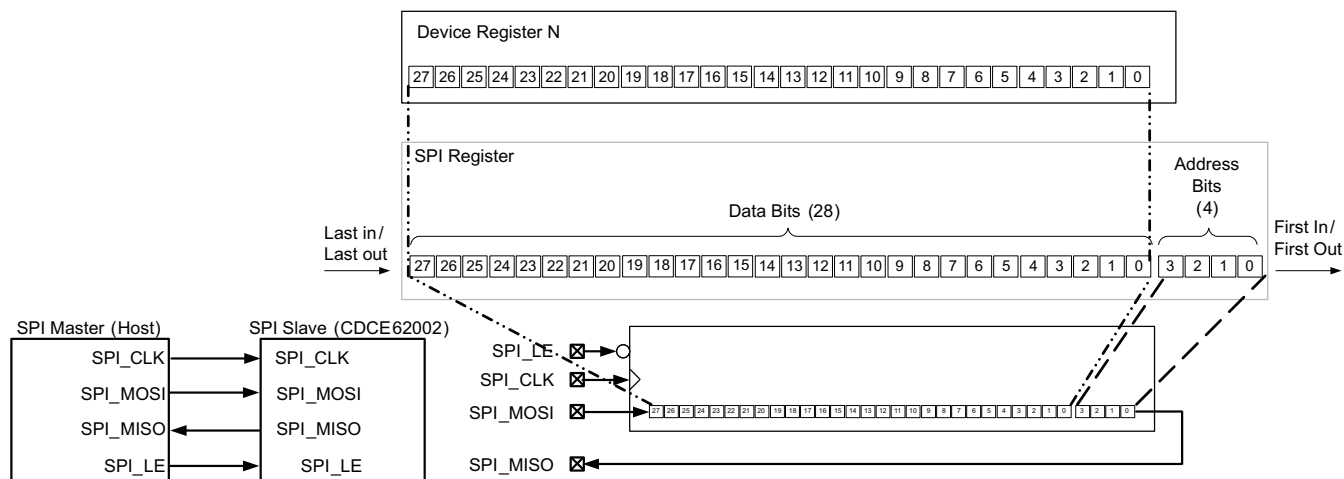


**Figure 16. CDCE62002 SPI Communications Format**

## CDCE62002 SPI Command Structure

The CDCE62002 supports four commands issued by the Master via the SPI:

- Write to RAM
- Read Command
- Copy RAM to EEPROM – unlock

Table 6 provides a summary of the CDCE62002 SPI command structure. The host (master) constructs a Write to RAM command by specifying the appropriate register address in the address field and appends this value to the beginning of the data field. Therefore, a valid command stream must include 32 bits, transmitted LSB first. The host must issue a Read Command to initiate a data transfer from the CDCE62002 back to the host. This command specifies the address of the register of interest in the data field.

**Table 6. CDCE62002 SPI Command Structure**

| Register | Operation | NVM | Data Field (28 Bits) | | | | | | | | | | | | | | | | | | | | | | | | | | Addr Field (4 Bits) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 |
| 0 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 |
| 1 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 1 |
| 2 | Status/Control | No | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 1 | 0 |
| Instruction | Read Command | No | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | A | A | A | 1 | 1 | 1 | 0 |
| Instruction | RAM EEPROM | Unlock | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

## Writing to the CDCE62002

Figure 17 illustrates a Write to RAM operation. Notice that the latching of the first data bit in the data stream (Bit 0) occurs on the first rising edge of SPI_CLK after SPI_LE transitions from a high to a low. For the CDCE62002, data transitions occur on the falling edge of SPI_CLK. A rising edge on SPI_LE signals to the CDCE62002 that the transmission of the last bit in the stream (Bit 31) has occurred.
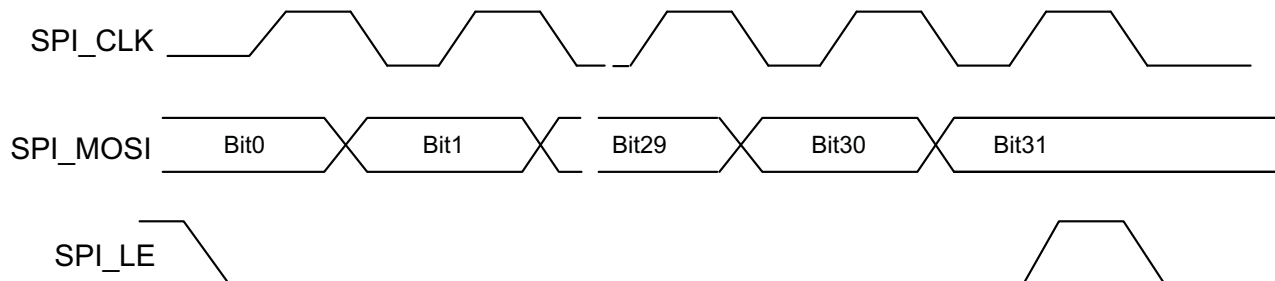
**Figure 17. CDCE62002 SPI Write Operation**

## Reading from the CDCE62002

Figure 18 shows how the CDCE62002 executes a Read Command. The SPI master first issues a Read Command to initiate a data transfer from the CDCE62002 back to the host (see Table 6). This command specifies the address of the register of interest. By transitioning SPI_LE from a low to a high, the CDCE62002 resolves the address specified in the appropriate bits of the data field. The host drives SPI_LE low and the CDCE62002 presents the data present in the register specified in the Read Command on SPI_MISO.
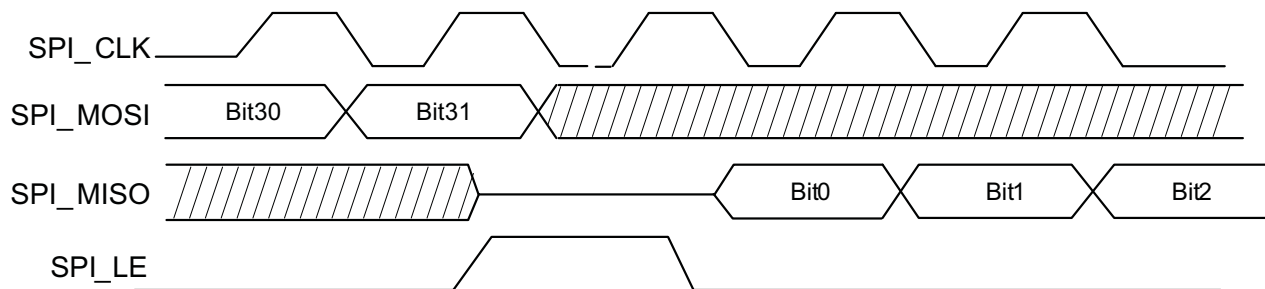
**Figure 18. CDCE62002 Read Operation**

## Writing to EEPROM

After the CDCE62002 detects a power-up and completes a reset cycle, it copies the contents of the on-board EEPROM into the Device Registers. Therefore, the CDCE62002 initializes into a known state predefined by the user. The host issues an EEPROM write command shown in Table 6 to copy the contents of Device Registers 0 through 1 into EERPOM.

After an EEPROM write command is initiated, power must remain stable and the host must not access the CDCE62002 for at least 50 ms to allow the EEPROM to complete the write cycle and to avoid the possibility of EEPROM corruption.

## Device Registers: Register 0

### Table 7. CDCE62002 Register 0 Bit Definitions

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION / FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 0 |
| 1 | | A1 | | Address 1 | 0 |
| 2 | | A2 | | Address 2 | 0 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | INBUFSELX | INBUFSELX | Input Buffer Select (LVPECL,LVDS or LVCMOS) | EEPROM |
| 5 | 1 | INBUFSELY | INBUFSELY | XY(00 ) Disabled, (01) LVPECL, (10) LVDS, (11) LVCMOS<br>The VBB internal Biasing will be determined from this setting | EEPROM |
| 6 | 2 | REFSEL | Smart MUX Bits(2,3) | *See specific section for more detailed description and configuration setup.* | EEPROM |
| 7 | 3 | AUXSEL | | 00 – RESERVED<br>10 – REF_IN Select<br>01– AUX_IN Select<br>11 – Auto Select ( Reference then AUX) | EEPROM |
| 8 | 4 | ACDCSEL | Input Buffers | If Set to "1" DC Termination, If set to "0" AC Termination | EEPROM |
| 9 | 5 | TERMSEL | Input Buffers | If Set to "0" Input Buffer Internal Termination Enabled | EEPROM |
| 10 | 6 | REFDIVIDE 0 | | Reference Divider Settings.<br>*See specific section for more detailed description and configuration setup.* | EEPROM |
| 11 | 7 | REFDIVIDE 1 | | | EEPROM |
| 12 | 8 | REFDIVIDE 2 | | | EEPROM |
| 13 | 9 | REFDIVIDE 3 | | | EEPROM |
| 14 | 10 | RESERVED | | Always Set to "0" | EEPROM |
| 15 | 11 | *I70TEST* | *TEST* | *Set to "0" for Normal Operation.* | EEPROM |
| 16 | 12 | *ATETEST* | *TEST* | *Set to "0" for Normal Operation.* | EEPROM |
| 17 | 13 | LOCKW(0) | PLL Lock | Lock-detect window Bit 0 | EEPROM |
| 18 | 14 | LOCKW(1) | PLL Lock | Lock-detect window Bit 1 | EEPROM |
| 19 | 15 | OUT0DIVRSEL0 | Output 0 | Output 0 Divider Settings.<br>*See specific section for more detailed description and configuration setup.* | EEPROM |
| 20 | 16 | OUT0DIVRSEL1 | Output 0 | | EEPROM |
| 21 | 17 | OUT0DIVRSEL2 | Output 0 | | EEPROM |
| 22 | 18 | OUT0DIVRSEL3 | Output 0 | | EEPROM |
| 23 | 19 | OUT1DIVRSEL0 | Output 1 | Output 1 Divider Settings.<br>*See specific section for more detailed description and configuration setup.* | EEPROM |
| 24 | 20 | OUT1DIVRSEL1 | Output 1 | | EEPROM |
| 25 | 21 | OUT1DIVRSEL2 | Output 1 | | EEPROM |
| 26 | 22 | OUT1DIVRSEL3 | Output 1 | | EEPROM |
| 27 | 23 | HIPERORMANCE | Output 0 & 1 | High Performance, If this Bit is set to "1":<br>– Increase the Bias in the device to achieve Best Phase Noise on the Output Divider<br>– It changes the LVPECL Buffer to Hi Swing in LVPECL.<br>– It increases the current consumption by 20mA (Typical) | EEPROM |
| 28 | 24 | OUTBUFSEL0X | Output 0 | Output Buffer mode select for OUTPUT "0 ".<br>(X,Y)=00:Disabled, 01:LVCMOS, 10:LVDS, 11:LVPECL | EEPROM |
| 29 | 25 | OUTBUFSEL0Y | Output 0 | | EEPROM |
| 30 | 26 | OUTBUFSEL1X | Output 1 | Output Buffer mode select for OUTPUT "1 ".<br>(X,Y)=00:Disabled, 01:LVCMOS, 10:LVDS, 11:LVPECL | EEPROM |
| 31 | 27 | OUTBUFSEL1Y | Output 1 | | EEPROM |

Product Folder Link(s): *CDCE62002*

**Table 8. Reference Input AC/DC Input Termination Table**

| REFERENCE INPUT | RAM BITS | | | | VBB VOLTAGE | REF+ TERMINATION | REF– TERMINATION |
|---|---|---|---|---|---|---|---|
| **INTERNAL TERMINATION** | 0 | 1 | 4 | 5 | GENERATOR | 5kΩ to VBB | 5kΩ to VBB |
| External Termination | X | X | X | 1 | OFF | OPEN | OPEN |
| Disabled | 0 | 0 | X | X | OFF | OPEN | OPEN |
| LVCMOS | 1 | 1 | X | 0 | OFF | OPEN | OPEN |
| LVPECL-AC | 0 | 1 | 0 | 0 | 1.9V | CLOSED | CLOSED |
| LVPECL-DC | 0 | 1 | 1 | 0 | 1.0V | CLOSED | CLOSED |
| LVDS-AC | 1 | 0 | 0 | 0 | 1.2V | CLOSED | CLOSED |
| LVDS-DC | 1 | 0 | 1 | 0 | 1.2V | CLOSED | CLOSED |

Product Folder Link(s): *CDCE62002*

## Device Registers: Register 1

### Table 9. CDCE62002 Register 1 Bit Definitions

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION / FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 1 |
| 1 | | A1 | | Address 1 | 0 |
| 2 | | A2 | | Address 2 | 0 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | SELVCO | VCO Core | VCO Select | EEPROM |
| 5 | 1 | SELINDIV0 | VCO Core | Input Divider Settings. *See specific section for more detailed description and configuration setup.* | EEPROM |
| 6 | 2 | SELINDIV1 | VCO Core | | EEPROM |
| 7 | 3 | SELINDIV2 | VCO Core | | EEPROM |
| 8 | 4 | SELINDIV3 | VCO Core | | EEPROM |
| 9 | 5 | SELINDIV4 | VCO Core | | EEPROM |
| 10 | 6 | SELINDIV5 | VCO Core | | EEPROM |
| 11 | 7 | SELINDIV6 | VCO Core | | EEPROM |
| 12 | 8 | SELINDIV7 | VCO Core | | EEPROM |
| 13 | 9 | SELPRESCA | VCO Core | PRESCALER Setting. *See specific section for more detailed description and configuration setup.* | EEPROM |
| 14 | 10 | SELPRESCB | VCO Core | | EEPROM |
| 15 | 11 | SELFBDIV0 | VCO Core | FEEDBACK DIVIDER Setting *See specific section for more detailed description and configuration setup.* | EEPROM |
| 16 | 12 | SELFBDIV1 | VCO Core | | EEPROM |
| 17 | 13 | SELFBDIV2 | VCO Core | | EEPROM |
| 18 | 14 | SELFBDIV3 | VCO Core | | EEPROM |
| 19 | 15 | SELFBDIV4 | VCO Core | | EEPROM |
| 20 | 16 | SELFBDIV5 | VCO Core | | EEPROM |
| 21 | 17 | SELFBDIV6 | VCO Core | | EEPROM |
| 22 | 18 | SELFBDIV7 | VCO Core | | EEPROM |
| 23 | 19 | SELBPDIV0 | VCO Core | BYPASS DIVIDER Setting ( 6 settings + Disable + Enable) *See specific section for more detailed description and configuration setup.* | EEPROM |
| 24 | 20 | SELBPDIV1 | VCO Core | | EEPROM |
| 25 | 21 | SELBPDIV2 | VCO Core | | EEPROM |
| 26 | 22 | LFRCSEL0 | VCO Core | Loop Filter & Charge Pump Control Setting *See specific section for more detailed description and configuration setup.* | EEPROM |
| 27 | 23 | LFRCSEL1 | VCO Core | | EEPROM |
| 28 | 24 | LFRCSEL2 | VCO Core | | EEPROM |
| 29 | 25 | LFRCSEL3 | VCO Core | | EEPROM |
| 30 | 26 | RESERVED | Status | TI Use Only | EEPROM |
| 31 | 27 | RESERVED | Status | Read Only always reads "1" | EEPROM |

## Device Registers: Register 2

### Table 10. CDCE62002 Register 2 Bit Definitions

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION / FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 0 |
| 1 | | A1 | | Address 1 | 1 |
| 2 | | A2 | | Address 2 | 0 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 5 | 1 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 6 | 2 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 7 | 3 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 8 | 4 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 9 | 5 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 10 | 6 | PLLLOCKPIN | Status | Read Only: Status of the PLL Lock Pin Driven by the device. PLL Lock = 1 | RAM |
| 11 | 7 | $\overline{PD}$ | Control | Power Down mode "On" when set to "0", Off when set to "1" is normal operation ($\overline{PD}$ bit does not load the EEPROM into RAM when set to "1"). | RAM |
| 12 | 8 | $\overline{SYNC}$ | Control | If toggled "1-0-1" this bit forces "$\overline{SYNC}$" resynchronize the Output Dividers. | RAM |
| 13 | 9 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 14 | 10 | VERSION0 | Read Only | | RAM |
| 15 | 11 | VERSION1 | Read Only | | RAM |
| 16 | 12 | VERSION2 | Read Only | | RAM |
| 17 | 13 | PLLRESET | VCO Core | If toggled "0-1-0" it Resets PLL to start calibration. "0" is normal operation. | RAM |
| 18 | 14 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 19 | 15 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 20 | 16 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 21 | 17 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 22 | 18 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 23 | 19 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 24 | 20 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 25 | 21 | *TITSTCFG0* | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 26 | 22 | *TITSTCFG1* | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 27 | 23 | *TITSTCFG2* | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 28 | 24 | *TITSTCFG3* | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 29 | 25 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 30 | 26 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |
| 31 | 27 | RESERVED | Diagnostics | *TI Test Registers. For TI Use Only* | RAM |

## Device Control

Figure 19 provides a conceptual explanation of the CDCE62002 Device operation. Table 11 defines how the device behaves in each of the operational states.
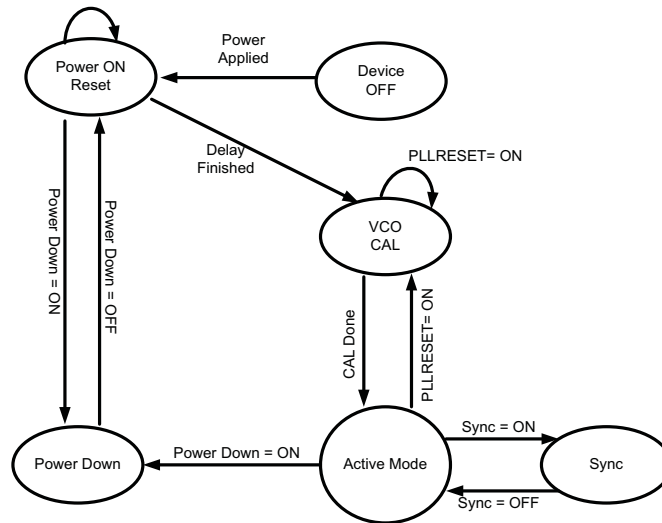


**Figure 19. CDCE62002 Device State Control Diagram**

**Table 11. CDCE62002 Device State Definitions**

| State | Device Behavior | Entered Via | Exited Via | SPI Port Status | PLL Status | Output Divider Status | Output Buffer Status |
|---|---|---|---|---|---|---|---|
| Power-On Reset | After device power supply reaches approximately 2.35V, the contents of EEPROM are copied into the Device Registers, thereby initializing the device hardware . | Power applied to the device or upon exit from Power Down State via the $\overline{PD}$ pin set HIGH. | Power On Reset and EEPROM loading delays are finished OR the $\overline{PD}$ pin is set LOW. | OFF | Disabled | Disabled | OFF |
| VCO CAL | The voltage controlled oscillator is calibrated based on the PLL settings and the incoming reference clock. After the VCO has been calibrated, the device enters Active Mode automatically. | Delay process in the Power-On Reset State is finished or PLLRESET=ON | Calibration Process in completed | ON | Enabled | Disabled | OFF |
| Active Mode | Normal Operation | CAL Done (VCO calibration process finished) or Sync = OFF (from Sync State). | Power Down or PLLRESET=ON | ON | Enabled | Disabled or Enabled | Disabled or Enabled |
| Power Down | Used to shut down all hardware and Resets the device after exiting the Power Down State. Therefore, the EEPROM contents will eventually be copied into RAM after the Power Down State is exited. | $\overline{PD}$ pin is pulled LOW. | $\overline{PD}$ pin is pulled HIGH. | ON | Disabled | Disabled | Disabled |
| Sync | Sync synchronizes both outputs dividers so that they begin counting at the same time | $\overline{Sync}$ Bit in device register 2 bit 8 is set LOW | $\overline{Sync}$ bit in device register 2 bit 8 is set HIGH | ON | Enabled | Disabled | Disabled |

## External Control Pins

### Power Down ($\overline{PD}$)

When pulled LOW, $\overline{PD}$ activates the Power Down state which shuts down all hardware and resets the device. Restoring $\overline{PD}$ high will cause the CDCE62002 to exit the Power Down State. This causes the device to behave as if it has been powered up including copying the EEPROM contents into RAM. $\overline{PD}$ pin also has a shadowed $\overline{PD}$ bit residing in Register 2 Bit 7. When asserted Low it puts the device in Power Down Mode, but it does not load the EEPROM when the bits is disserted.

Product Folder Link(s): *CDCE62002*

---

**NOTE**

The SPI_LE signal has to be high in order for the EEPROM to load correctly into RAM on the Rising edge of $\overline{PD}$ Pin.

---

## FACTORY DEFAULT PROGRAMMING

The CDCE62002 is factory pre-programmed to work with 25 MHz input from the reference input or from the auxiliary input with auto switching enabled. An internal PFD of 6.25 MHz and about 400 KHz loop bandwidth. Output 0 is pre-programmed as an LCPECL driver to output 156.25 MHz and output 1 is pre-programmed as LVDS driver to output 125 MHz.
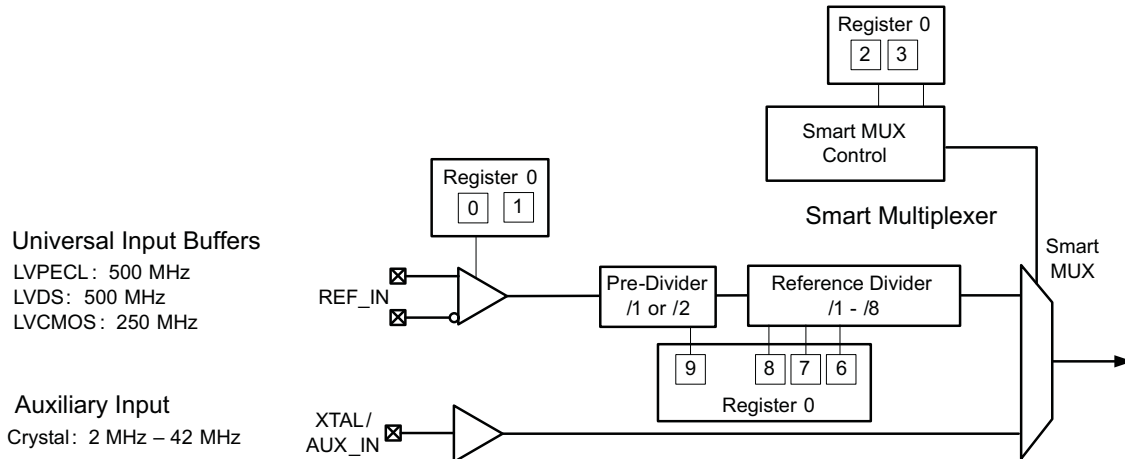


| EEPROM | Register Content |
|---|---|
| Register 0 | 72A000E0 |
| Register 1 | 8389A061 |
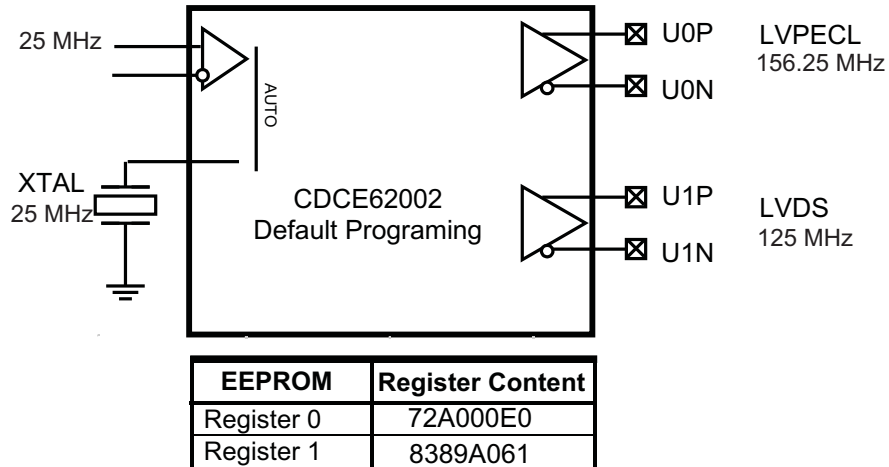
**Figure 20. CDCE62002 Default Factory Programming**

Product Folder Link(s): *CDCE62002*

## INPUT BLOCK

The Input Block includes one Universal Input Buffers, an Auxiliary Input, and a Smart Multiplexer.



**Figure 21. CDCE62002 Input Block With References to Registers**

The CDCE62002 provides a Reference Divider that divides the clock exiting Reference (REF_IN) input buffer.

**Table 12. CDCE62002 Reference Divider Settings**

| BIT NAME → | REFERENCE DIVIDER | | | | TOTAL DIVIDE RATIO |
|---|---|---|---|---|---|
| | REFDIVIDE3 | REFDIVIDE2 | REFDIVIDE1 | REFDIVIDE0 | |
| REGISTER BIT → | 0.9 | 0.8 | 0.7 | 0.6 | |
| | 0 | 0 | 0 | 0 | /1 |
| | 0 | 0 | 0 | 1 | /2 |
| | 0 | 0 | 1 | 0 | /3 |
| | 0 | 0 | 1 | 1 | /4 |
| | 0 | 1 | 0 | 0 | /5 |
| | 0 | 1 | 0 | 1 | /6 |
| | 0 | 1 | 1 | 0 | /7 |
| | 0 | 1 | 1 | 1 | /8 |
| | 1 | 0 | 0 | 0 | /2 |
| | 1 | 0 | 0 | 1 | /4 |
| | 1 | 0 | 1 | 0 | /6 |
| | 1 | 0 | 1 | 1 | /8 |
| | 1 | 1 | 0 | 0 | /10 |
| | 1 | 1 | 0 | 1 | /12 |
| | 1 | 1 | 1 | 0 | /14 |
| | 1 | 1 | 1 | 1 | /16 |

### Reference Input Buffer

Figure 22 shows the key elements of a Universal Input Buffer (UIB). A UIB supports multiple formats along with different termination and coupling schemes. The CDCE62002 implements the UIB by including on board switched termination, a programmable bias voltage generator, and a multiplexer. The CDCE62002 provides a high degree of configurability on the UIB to facilitate most existing clock input formats.
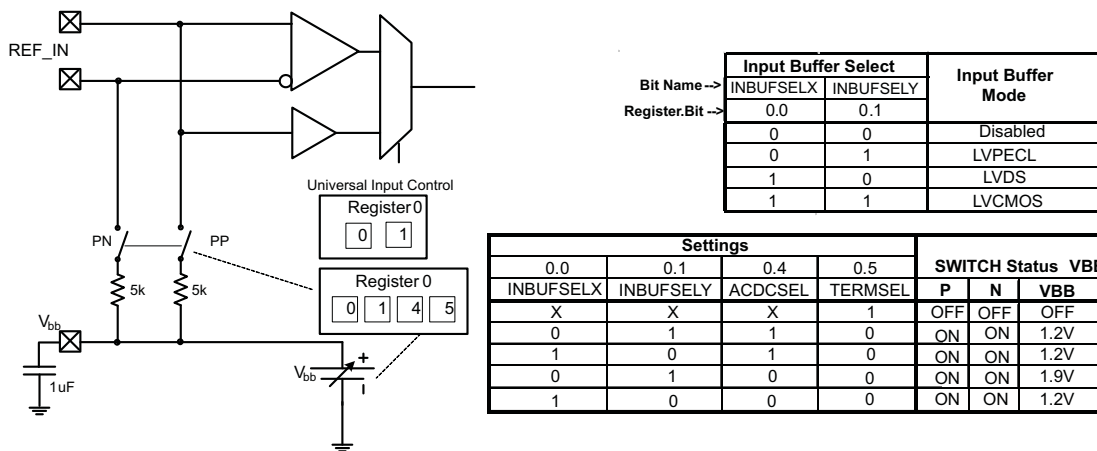


| Bit Name --> | Input Buffer Select | | Input Buffer Mode |
|---|---|---|---|
| | INBUFSELX | INBUFSELY | |
| Register.Bit --> | 0.0 | 0.1 | |
| | 0 | 0 | Disabled |
| | 0 | 1 | LVPECL |
| | 1 | 0 | LVDS |
| | 1 | 1 | LVCMOS |

| Settings | | | | SWITCH Status  VBB | | |
|---|---|---|---|---|---|---|
| 0.0 | 0.1 | 0.4 | 0.5 | | | |
| INBUFSELX | INBUFSELY | ACDCSEL | TERMSEL | P | N | VBB |
| X | X | X | 1 | OFF | OFF | OFF |
| 0 | 1 | 1 | 0 | ON | ON | 1.2V |
| 1 | 0 | 1 | 0 | ON | ON | 1.2V |
| 0 | 1 | 0 | 0 | ON | ON | 1.9V |
| 1 | 0 | 0 | 0 | ON | ON | 1.2V |

**Figure 22.  CDCE62002 Universal Input Buffer**

### Smart Multiplexer Dividers



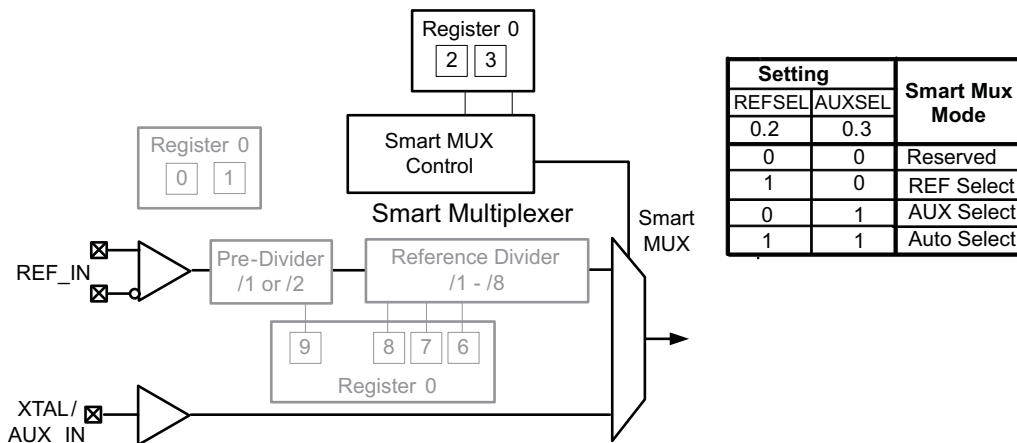| Setting | | Smart Mux Mode |
|---|---|---|
| REFSEL | AUXSEL | |
| 0.2 | 0.3 | |
| 0 | 0 | Reserved |
| 1 | 0 | REF Select |
| 0 | 1 | AUX Select |
| 1 | 1 | Auto Select |

**Figure 23.  CDCE62002 Smart Multiplexer**

In Auto Select Mode the Smart Mux switches automatically between Reference input and Auxiliary input with a preference to the Reference input. In order for the Smart Mux to function correctly the frequency after the reference divider and the Auxiliary Input signal frequency should be within 20% of each other or one of them should be zero or ground. In This mode a valid frequency needs to be present on AUX_IN before the /PD is deasserted or power is applied.

**Auxiliary Input Port**

The auxiliary input on the CDCE62002 is designed to connect to an AT-Cut Crystal with a total load capacitance of 8 pF to 10pF. One side of the crystal connects to Ground while the other side connects to the Auxiliary input of the device. The circuit accepts crystals from 2 to 42 MHz.
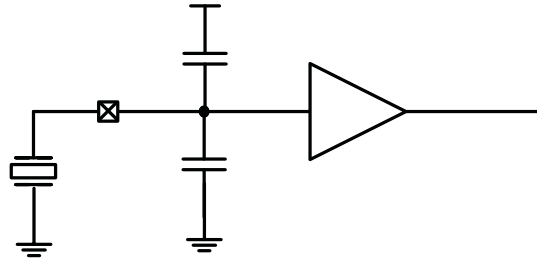


**Figure 24. CDCE62002 Auxiliary Input Port**

Product Folder Link(s): *CDCE62002*

## OUTPUT BLOCK

The output block includes two identical output channels. Each output channel comprises of a clock divider module, and a universal output buffer as shown in Figure 25.
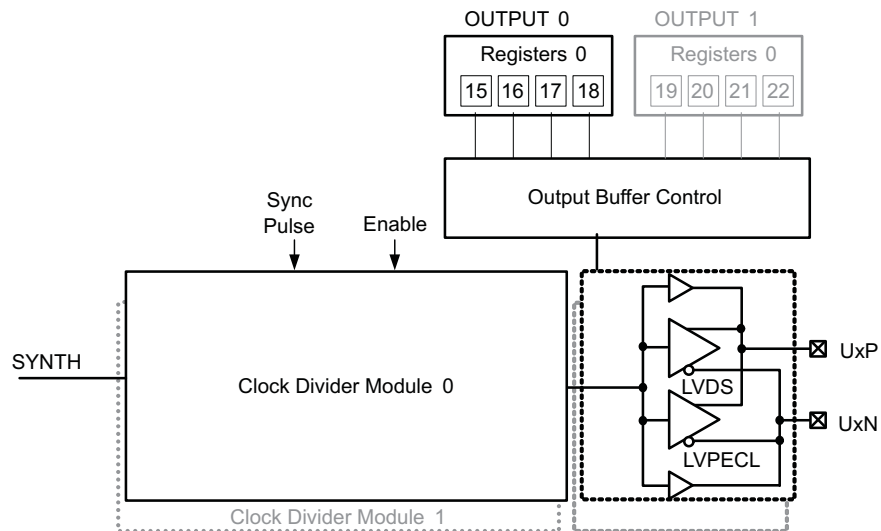


**Figure 25. CDCE62002 Output Channel**

**Table 13. CDCE62002 Output Divider Settings**

| OUTPUT DIVIDERS SETTING | | | | DIVIDE RATIO |
|---|---|---|---|---|
| DIVIDER 0 → 0.18 | 0.17 | 0.16 | 0.15 | |
| DIVIDER 1 → 0.22 | 0.21 | 0.20 | 0.19 | |
| 0 | 0 | 0 | 0 | Disabled |
| 0 | 0 | 0 | 1 | /1 |
| 0 | 0 | 1 | 0 | /2 |
| 0 | 0 | 1 | 1 | /3 |
| 0 | 1 | 0 | 0 | /4 |
| 0 | 1 | 0 | 1 | /5 |
| 0 | 1 | 1 | 0 | /6 |
| 0 | 1 | 1 | 1 | Disabled |
| 1 | 0 | 0 | 0 | /8 |
| 1 | 0 | 0 | 1 | Disabled |
| 1 | 0 | 1 | 0 | /10 |
| 1 | 0 | 1 | 1 | /20 |
| 1 | 1 | 0 | 0 | /12 |
| 1 | 1 | 0 | 1 | /24 |
| 1 | 1 | 1 | 0 | /16 |
| 1 | 1 | 1 | 1 | /32 |

## SYNTHESIZER BLOCK

Figure 26 provides an overview of the CDCE62002 synthesizer block. The Synthesizer Block provides a Phase Locked Loop, a partially integrated programmable loop filter, and two Voltage Controlled Oscillators (VCO). The synthesizer block generates an output clock called "SYNTH" and drives it onto the Internal Clock Distribution Bus.
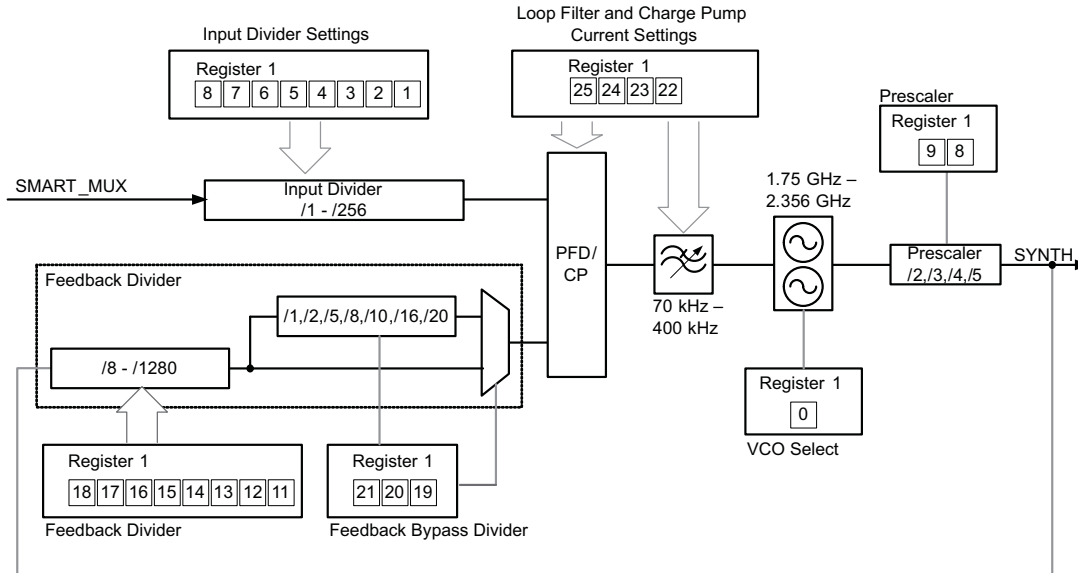


**Figure 26. CDCE62002 Synthesizer Block**

### Input Divider

The Input Divider divides the clock signal selected by the Smart Multiplexer and presents the divided signal to the Phase Frequency Detector / Charge Pump of the frequency synthesizer.

**Table 14. CDCE62002 Input Divider Settings**

| INPUT DIVIDER SETTINGS | | | | | | | | DIVIDE RATIO |
|---|---|---|---|---|---|---|---|---|
| SELINDIV7 | SELINDIV6 | SELINDIV5 | SELINDIV4 | SELINDIV3 | SELINDIV2 | SELINDIV1 | SELINDIV0 | |
| 1.8 | 1.7 | 1.6 | 1.5 | 1.4 | 1.3 | 1.2 | 1.1 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 6 |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 256 |

Product Folder Link(s): *CDCE62002*

## Feedback and Feedback Bypass Divider

Table 15 shows how to configure the Feedback divider for various divide values:

**Table 15. CDCE62002 Feedback Divider Settings**

| FEEDBACK DIVIDER | | | | | | | | DIVIDE RATIO |
|---|---|---|---|---|---|---|---|---|
| SELFBDIV7 | SELFBDIV6 | SELFBDIV5 | SELFBDIV4 | SELFBDIV3 | SELFBDIV2 | SELFBDIV1 | SELFBDIV0 | |
| 1.18 | 1.17 | 1.16 | 1.15 | 1.14 | 1.13 | 1.12 | 1.11 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 12 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 20 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 24 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 32 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 36 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 40 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 48 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 56 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 60 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 64 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 72 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 80 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 84 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 96 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 100 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 108 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 112 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 120 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 128 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 140 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 144 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 160 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 168 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 180 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 192 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 200 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 216 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 224 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 240 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 252 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 256 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 280 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 288 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 300 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 320 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 336 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 360 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 384 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 392 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 400 |

Submit Documentation Feedback 33

Product Folder Link(s): CDCE62002

**Table 15. CDCE62002 Feedback Divider Settings (continued)**

| FEEDBACK DIVIDER | | | | | | | | DIVIDE RATIO |
|---|---|---|---|---|---|---|---|---|
| SELFBDIV7 | SELFBDIV6 | SELFBDIV5 | SELFBDIV4 | SELFBDIV3 | SELFBDIV2 | SELFBDIV1 | SELFBDIV0 | |
| 1.18 | 1.17 | 1.16 | 1.15 | 1.14 | 1.13 | 1.12 | 1.11 | |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 420 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 432 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 448 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 480 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 500 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 504 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 512 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 560 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 576 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 588 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 600 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 640 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 672 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 700 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 720 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 768 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 784 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 800 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 840 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 896 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 960 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 980 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1024 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1120 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1280 |

Table 16 shows how to configure the Feedback Bypass Divider.

Product Folder Link(s): *CDCE62002*

**Table 16. CDCE62002 Feedback Bypass Divider Settings**

| FEEDBACK BYPASS DIVIDER | | | DIVIDE RATIO |
|---|---|---|---|
| **SELBPDIV2** | **SELBPDIV1** | **SELBPDIV0** | |
| **1.21** | **1.20** | **1.19** | |
| 0 | 0 | 0 | 2 |
| 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 8 |
| 0 | 1 | 1 | 10 |
| 1 | 0 | 0 | 16 |
| 1 | 0 | 1 | 20 |
| 1 | 1 | 0 | RESERVED |
| 1 | 1 | 1 | 1(bypass) |

**VCO Select**

Table 17 illustrates how to control the dual voltage controlled oscillators.

**Table 17. CDCE62002 VCO Select**

| BIT NAME → | VCO SELECT SELVCO | VCO CHARACTERISTICS | | |
|---|---|---|---|---|
| **REGISTER NAME →** | **1.0** | **VCO RANGE** | **Fmin (MHz)** | **Fmax (MHz)** |
| | 0 | Low | 1750 | 2046 |
| | 1 | High | 2040 | 2356 |

**Prescaler**

Table 18 shows how to configure the prescaler.

**Table 18. CDCE62002 Prescaler Settings**

| SETTINGS | | DIVIDE RATIO |
|---|---|---|
| **SELPRESCB** | **SELPRESCA** | |
| **1.10** | **1.9** | |
| 0 | 0 | 5 |
| 1 | 0 | 4 |
| 0 | 1 | 3 |
| 1 | 1 | 2 |

CDCE62002

## Loop Filter

Figure 27 depicts the loop filter topology of the CDCE62002. It facilitates both internal and external implementations providing optimal flexibility.
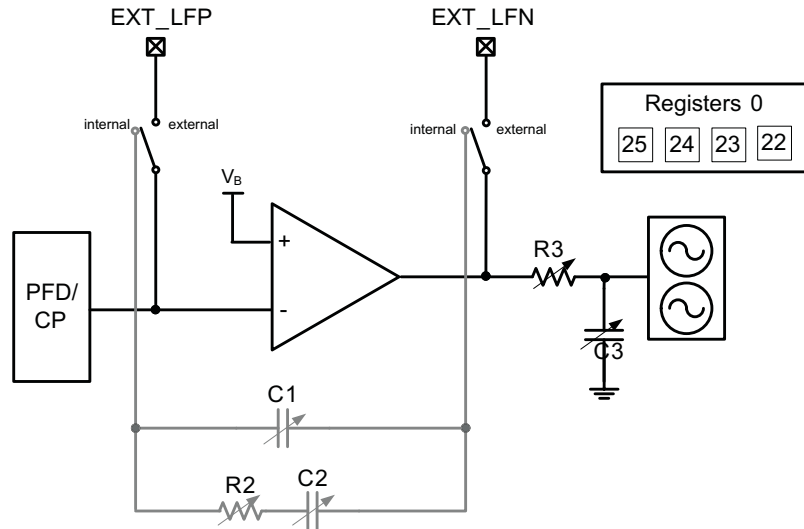


**Figure 27. CDCE62002 Loop Filter Topology**

### *Internal Loop Filter Component Configuration*

Figure 27 illustrates the switching between four fixed internal loop filter settings and the external loop filter setting. Table 19 shows that the CDCE62002 has 16 settings different settings for the loop filter. Four of the settings are internal and twelve are external.

**Table 19. CDCE62002 Loop Filter Settings**

| LFRCSEL | | | | | | | | | | 3 db Corner | Charge Pump |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 2 | 1 | 0 | Loop Filter | C1 | C2 | R2 | R3 | C3 | C3R3 | Current |
| 0 | 0 | 0 | 0 | Internal | 1.5 pF | 473.5 pF | 4.0k | 5k | 2.5 pF | 12 MHz | 1.5 mA |
| 0 | 0 | 0 | 1 | Internal | 1.5 pF | 473.5 pF | 4.0k | 5k | 2.5 pF | 12 MHz | 400 μA |
| 0 | 0 | 1 | 0 | Internal | 1.5 pF | 473.5 pF | 2.7k | 5k | 2.5 pF | 12 MHz | 250 μA |
| 0 | 0 | 1 | 1 | Internal | 1.5 pF | 473.5 pF | 2.7k | 5k | 2.5 pF | 12 MHz | 150 μA |
| 0 | 1 | 0 | 0 | External | X | X | X | 20k | 112 pF | 70 kHz | 1.0 mA |
| 0 | 1 | 0 | 1 | External | X | X | X | 20k | 112 pF | 70 kHz | 2.0 mA |
| 0 | 1 | 1 | 0 | External | X | X | X | 20k | 112 pF | 70 kHz | 3.0 mA |
| 0 | 1 | 1 | 1 | External | X | X | X | 20k | 112 pF | 70 kHz | 3.75 mA |
| 1 | 0 | 0 | 0 | External | X | X | X | 10k | 100 pF | 150 kHz | 1.0 mA |
| 1 | 0 | 0 | 1 | External | X | X | X | 10k | 100 pF | 150 kHz | 2.0 mA |
| 1 | 0 | 1 | 0 | External | X | X | X | 10k | 100 pF | 150 kHz | 3.0 mA |
| 1 | 0 | 1 | 1 | External | X | X | X | 10k | 100 pF | 150 kHz | 3.75 mA |
| 1 | 1 | 0 | 0 | External | X | X | X | 5k | 100 pF | 300 kHz | 1.0 mA |
| 1 | 1 | 0 | 1 | External | X | X | X | 5k | 64 pF | 500 kHz | 2.0 mA |
| 1 | 1 | 1 | 0 | External | X | X | X | 5k | 48 pF | 700 kHz | 3.0 mA |
| 1 | 1 | 1 | 1 | External | X | X | X | 5k | 38 pF | 800 kHz | 3.75 mA |

Product Folder Link(s): *CDCE62002*

**Lock Detect**

The CDCE62002 provides a lock detect indicator circuit that can be detected on an external Pin PLL_LOCK (Pin 32) and internally by reading PLLLOCKPIN bit (6) in Register 2.

Two signals whose phase difference is less than a prescribed amount are 'locked' otherwise they are 'unlocked'. The phase frequency detector / charge pump compares the clock provided by the input divider and the feedback divider; using the input divider as the phase reference. The lock detect circuit implements a programmable lock detect window. Table 20 shows an overview of how to configure the lock detect feature. The PLL_LOCK pin will possibly jitter several times between lock and out of lock until the PLL achieves a stable lock. If desired, choosing a wide loop bandwidth and a high number of successive clock cycles virtually eliminates this characteristic. PLL_LOCK will return to out of lock, if just one cycle is outside the lock detect window or if a cycle slip occurs.
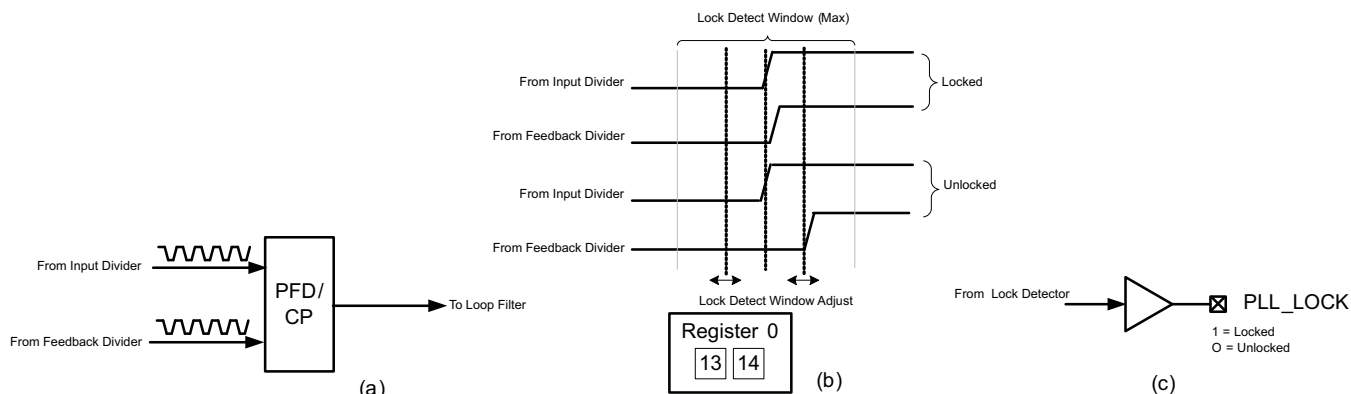


**Figure 28. CDCE62002 Lock Detect**

**Table 20. CDCE62002 Lock Detect Control**

| | LOCK DETECT | | LOCK DETECT WINDOW |
|---|---|---|---|
| BIT NAME → | LOCKW(1) | LOCKW(0) | |
| REGISTER NAME → | 0.13 | 0.14 | |
| | 0 | 0 | 2.1 ns |
| | 0 | 1 | 4.6 ns |
| | 1 | 0 | 7.2 ns |
| | 1 | 1 | 19.9 ns |

Product Folder Link(s): CDCE62002

## Device Power Calculation and Thermal Management

The CDCE62002 is a high performance device; therefore careful attention must be paid to device configuration and printed circuit board layout with respect to power consumption. Table 21 provides the power consumption for the individual blocks within the CDCE62002. To estimate total power consumption, calculate the sum of the products of the number of blocks used and the power dissipated of each corresponding block.

**Table 21. CDCE62002 Power Consumption**

| INTERNAL BLOCK (Power at 3.3V) | POWER DISSIPATED PER BLOCK | NUMBER OF BLOCKS PER DEVICE |
|---|---|---|
| Input Circuit | 32 | 1 |
| PLL and VCO Core | 333 | 1 |
| Output Divider | 92 | 2 |
| Output Buffer ( LVPECL) | 150 | 2 |
| Output Buffer (LVDS) | 95 | 2 |
| Output Buffer (LVCMOS) | 62 | 4 |

This power estimate determines the degree of thermal management required for a specific design. Observing good thermal layout practices enables the thermal pad on the backside of the QFN-32 package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.
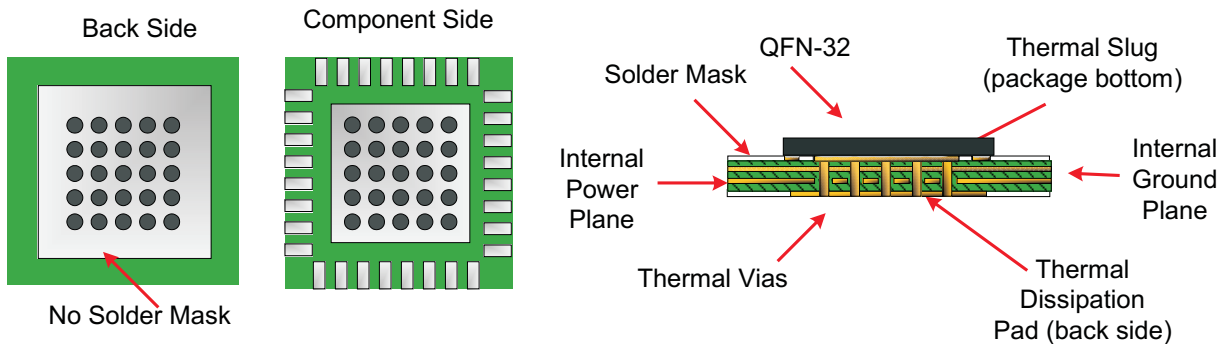


**Figure 29.  CDCE62002 Recommended PCB Layout**

## CDCE62002 Power Supply Bypassing – Recommended Layout

Figure 30 shows a conceptual layout focusing on power supply bypass capacitor placement. If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the Thermal Dissipation Pad can be difficult. If the capacitors are mounted on the component side, 0201 components must be used to facilitate signal routing. In either case, the connections between the capacitor and the power supply terminal on the device must be kept as short as possible.
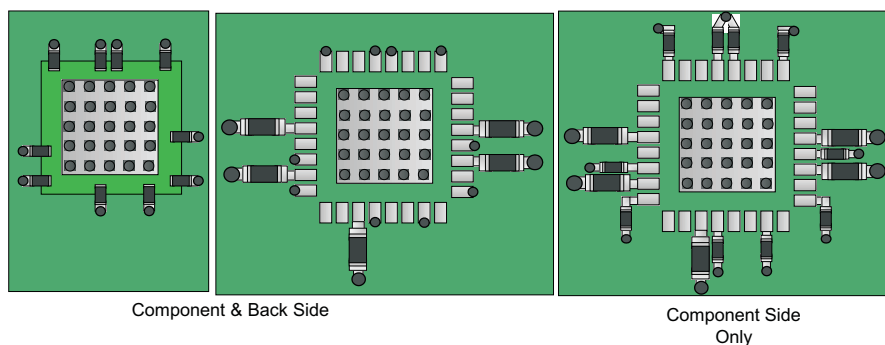


**Figure 30.  CDCE62002 Power Supply Bypassing**

Product Folder Link(s): *CDCE62002*

## APPLICATION INFORMATION AND GENERAL USAGE HINTS

### Clock Generator

The CDCE62002 can generate 1 to 4 low noise clocks from a single crystal or crystal oscillator as follows:
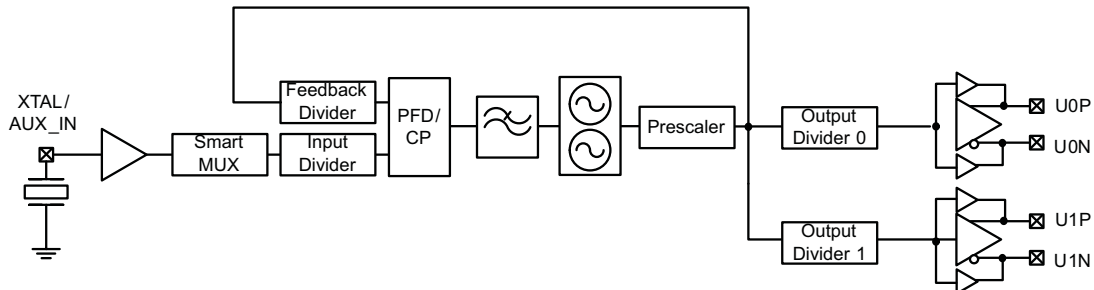


**Figure 31. CDCE62002 as a Clock Generator**

### SERDES Startup and Clock Cleaner

The CDCE62002 can serve as a SERDES device companion by providing a crystal based reference for the SERDES device to lock to receive data stream and when the SERDES locks to the data and outputs the recovered clock the CDCE62002 can switch and use the recovered clock and serve as a jitter cleaner.
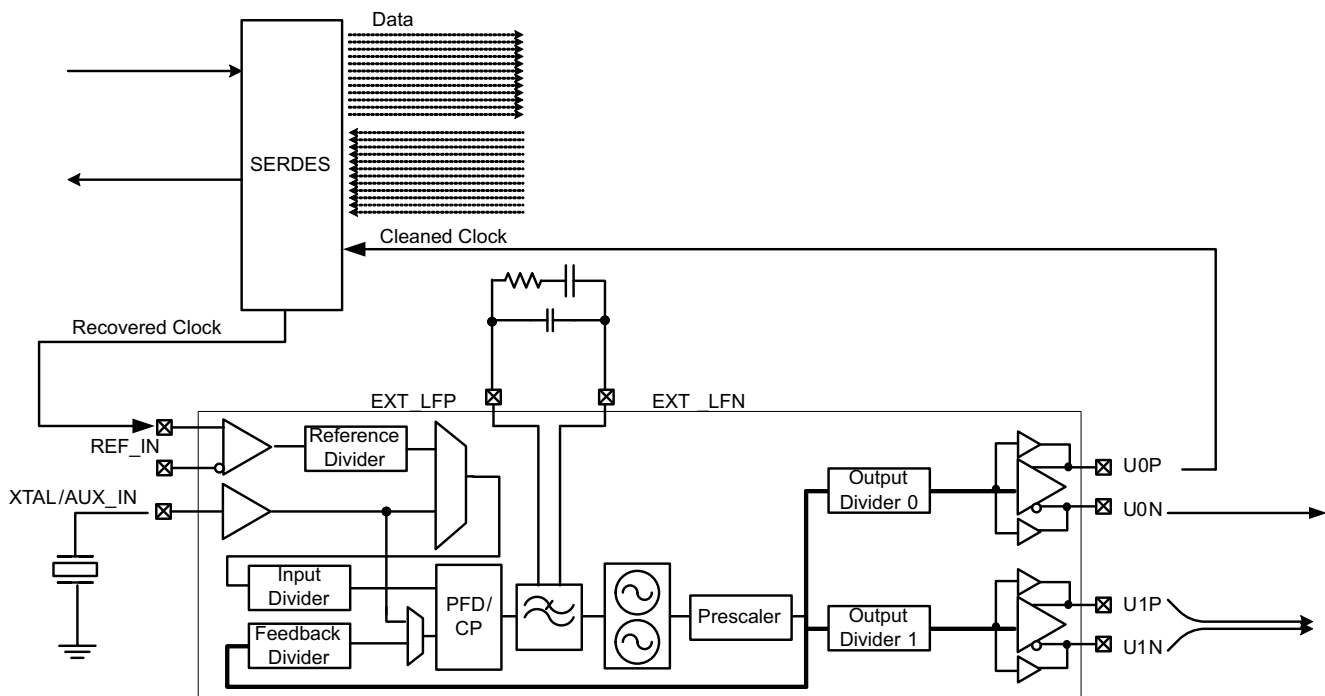


**Figure 32. CDCE62002 Clocking SERDES**

Since the jitter of the recovered clock can be above 100 ps (RMS) the output jitter from CDCE62002 can be as low and 6 ps (RMS) depending on the external loop filter configuration.

## CLOCKING ADCS WITH THE CDCE62002

High-speed analog to digital converters incorporate high input bandwidth on both the analog port and the sample clock port. Often the input bandwidth far exceeds the sample rate of the converter. Engineers regularly implement receiver chains that take advantage of the characteristics of bandpass sampling. This implementation trend often causes engineers working in communications system design to encounter the term "clock limited performance". Therefore, it is important to understand the impact of clock jitter on ADC performance. The following equation shows the relationship of data converter signal to noise ratio (SNR) to total jitter:

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi \, f_{in} \, jitter_{total}}\right]$$
(4)

Total jitter comprises two components: the intrinsic aperture jitter of the converter and the jitter of the sample clock:

$$jitter_{total} = \sqrt{\left(jitter_{ADC}\right)^2 + \left(jitter_{CLK}\right)^2}$$
(5)

With respect to an ADC with N-bits of resolution, ignoring total jitter, ADC quantization error, and input noise, the following equation shows the relationship between resolution and SNR:

$$SNR_{ADC} = 6.02N + 1.76$$
(6)

Figure 33 plots Equation 4 and Equation 6 for constant values of total jitter. When used in conjunction with most ADCs, the CDCE62002 supports a total jitter performance value of <1ps.

**Data Converter Jitter Requirements**
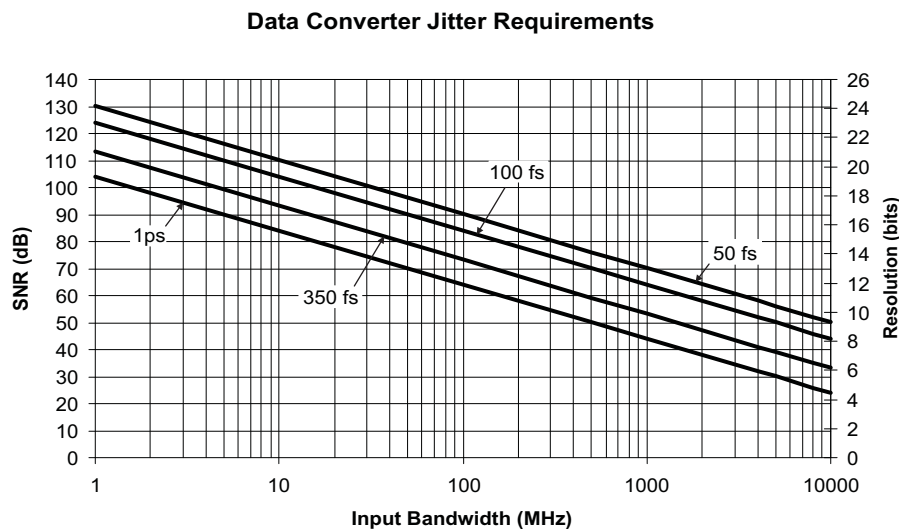


Figure 33. Data Converter Jitter Requirements

Product Folder Link(s): *CDCE62002*

# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Product Folder Link(s): CDCE62002

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| CDCE62002RHBR | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CDCE62002RHBT | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
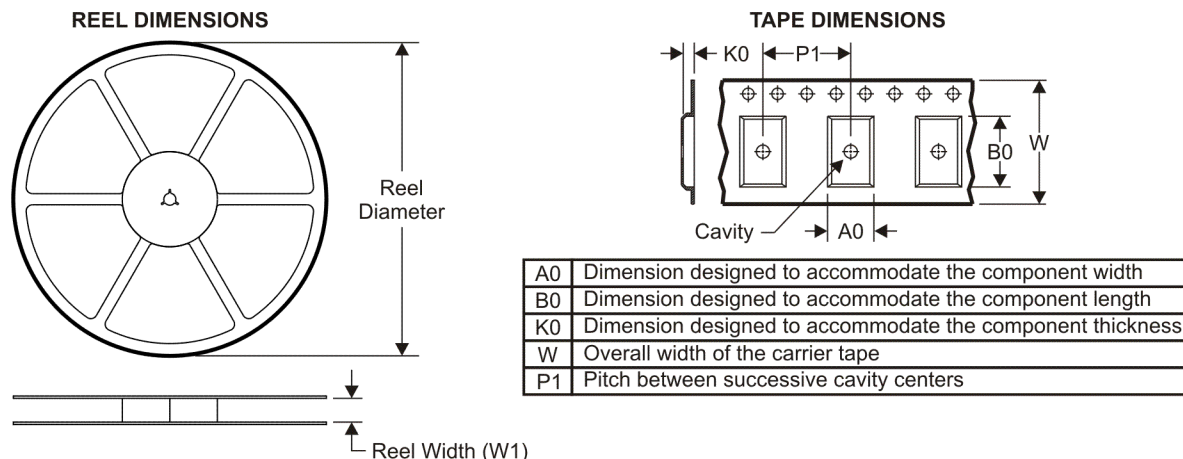**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
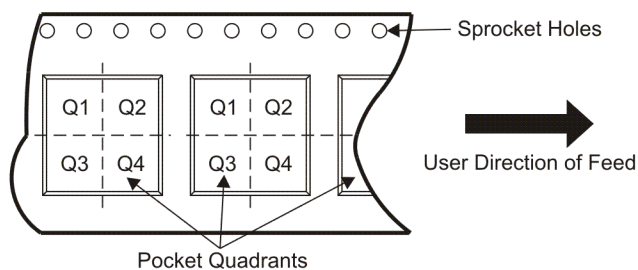
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCE62002RHBR | QFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| CDCE62002RHBT | QFN | RHB | 32 | 250 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| CDCE62002RHBR | QFN | RHB | 32 | 3000 | 340.5 | 333.0 | 20.6 |
| CDCE62002RHBT | QFN | RHB | 32 | 250 | 340.5 | 333.0 | 20.6 |

"CDCE62002"

# RHB (S−PQFP−N32)                    PLASTIC QUAD FLATPACK
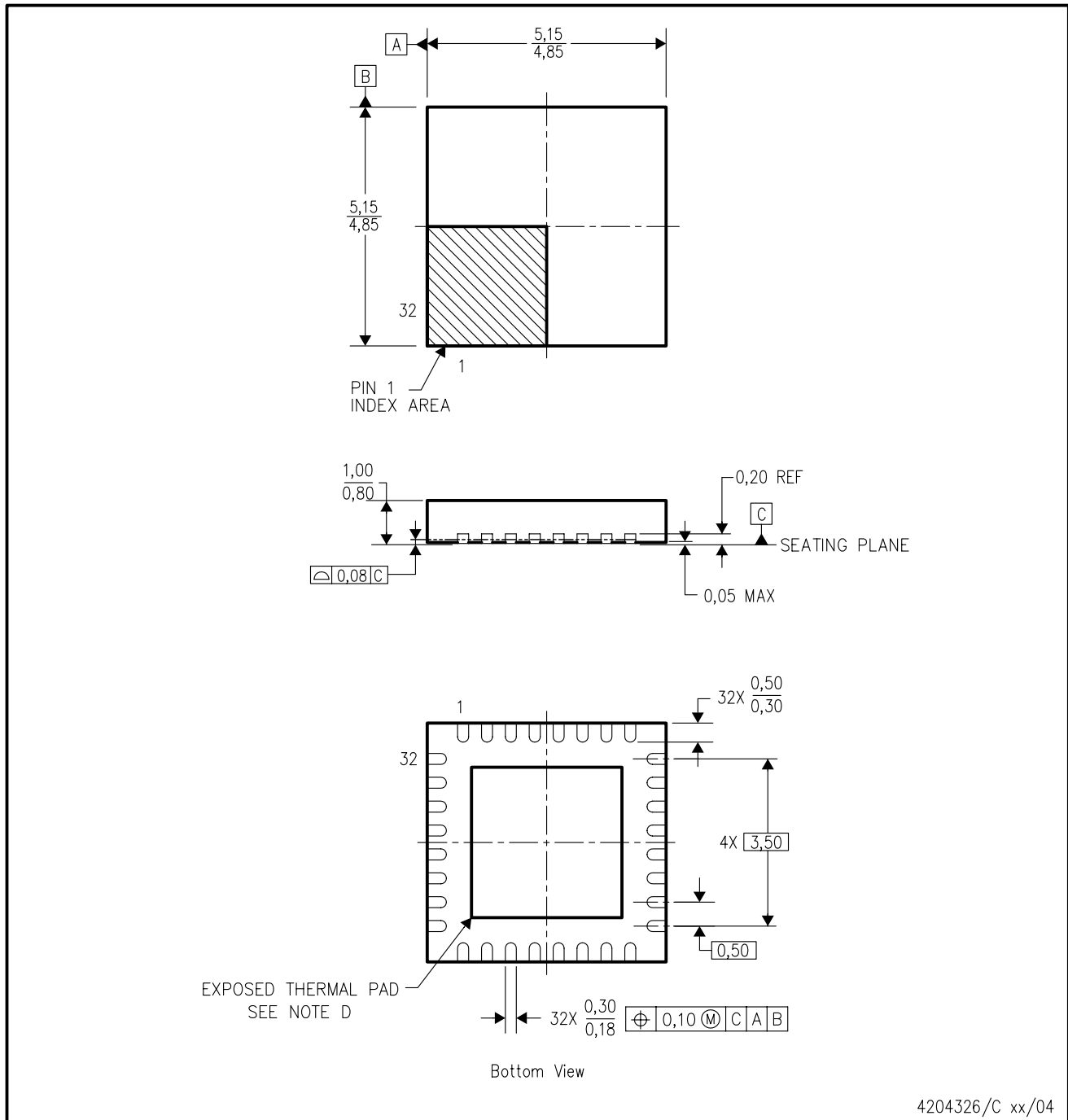
A ← 5,15 / 4,85 →

B

5,15 / 4,85

32

1

PIN 1
INDEX AREA

1,00 / 0,80

0,20 REF

C

SEATING PLANE

△ 0,08 C

0,05 MAX

1

32

32X 0,50 / 0,30

4X 3,50

0,50

EXPOSED THERMAL PAD
SEE NOTE D

32X 0,30 / 0,18          ⊕ 0,10 Ⓜ C A B

Bottom View

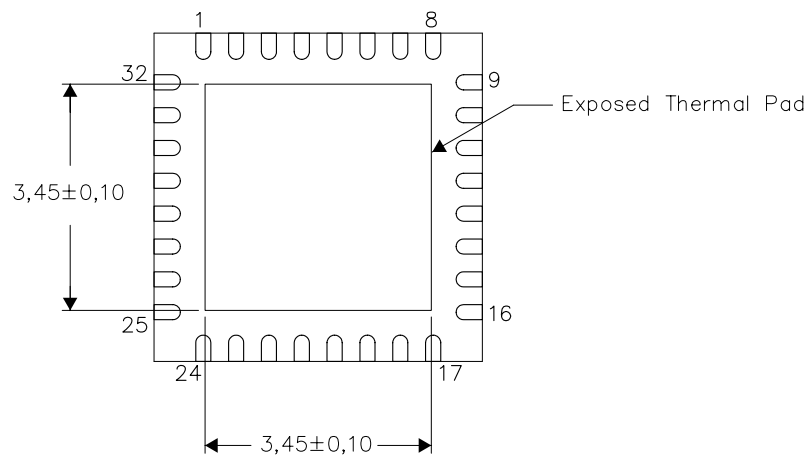4204326/C xx/04

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−Lead) Package configuration.
         D    The Package thermal pad must be soldered to the board for thermal and mechanical performance.
              See product data sheet for details regarding the exposed thermal pad dimensions.
         E.   Falls within JEDEC MO−220.

"CDCE62002"

RHB (S−PVQFN−N32)                    PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

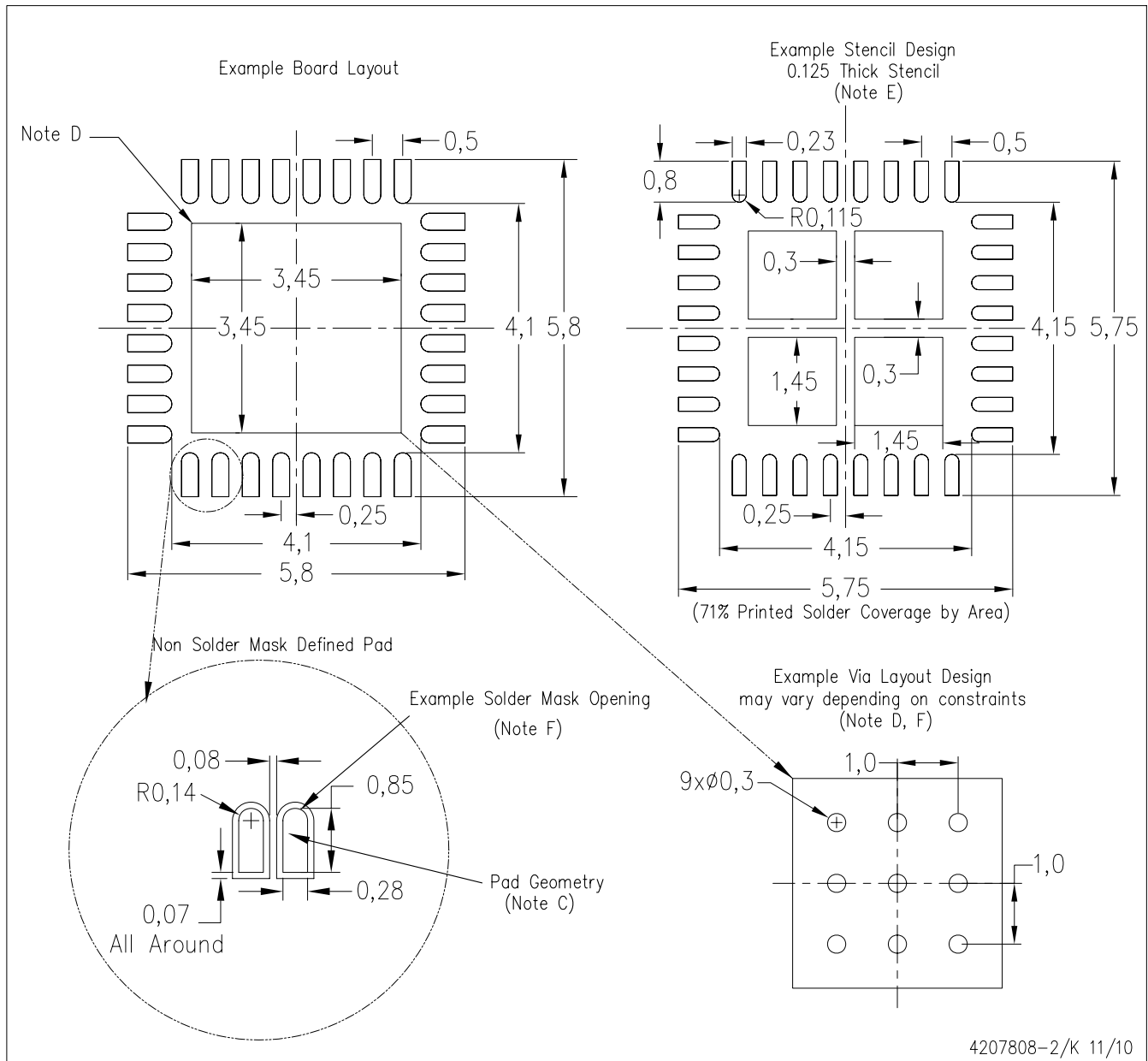Exposed Thermal Pad

3,45±0,10

3,45±0,10

Bottom View

Exposed Thermal Pad Dimensions

4206356−2/Q  11/10

NOTE:   A. All linear dimensions are in millimeters

RHB (S−PVQFN−N32)        PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Note D

0,5

3,45

3,45

4,1 5,8

0,25

4,1

5,8

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,28

0,07

All Around

Pad Geometry
(Note C)

Example Stencil Design
0.125 Thick Stencil
(Note E)

0,23

0,5

0,8

R0,115

0,3

1,45

0,3

4,15 5,75

1,45

0,25

4,15

5,75

(71% Printed Solder Coverage by Area)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

9xØ0,3

1,0

1,0

4207808−2/K 11/10

NOTES:    A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC−7351 is recommended for alternate designs.
          D.   This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat−Pack
               Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
               for specific thermal information, via requirements, and recommended board layout.  These documents are available at
               www.ti.com <http://www.ti.com>.
          E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
               contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
          F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
               recommendations for vias placed in the thermal pad.

**"CDCE62002"**

# IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DLP® Products | www.dlp.com | Communications and Telecom | www.ti.com/communications |
| DSP | dsp.ti.com | Computers and Peripherals | www.ti.com/computers |
| Clocks and Timers | www.ti.com/clocks | Consumer Electronics | www.ti.com/consumer-apps |
| Interface | interface.ti.com | Energy | www.ti.com/energy |
| Logic | logic.ti.com | Industrial | www.ti.com/industrial |
| Power Mgmt | power.ti.com | Medical | www.ti.com/medical |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Space, Avionics & Defense | www.ti.com/space-avionics-defense |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video and Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless-apps |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2010, Texas Instruments Incorporated