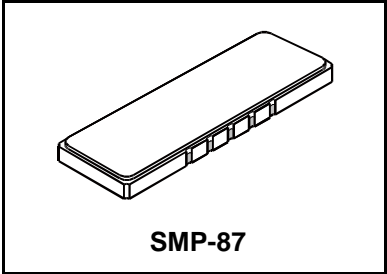


SF1081A-1

**71.00 MHz
SAW Filter**



- **Designed for GSM BTS Receiver IF Applications**
- **Simple External Impedance Matching**
- **Hermetic SMP-87 Surface-Mount Case**
- **Unbalanced Input and Output**
- **Wider Temperature Version of SF1081A**
- **Complies with Directive 2002/95/EC (RoHS)**



Absolute Maximum Ratings

Rating	Value	Units
Maximum Incident Power in Passband	+10	dBm
Max. DC voltage between any 2 terminals	30	VDC
Storage Temperature Range	-40 to +85	°C
Suitable for lead-free soldering - Max Soldering Profile	260°C for 30 s	

Electrical Characteristics


Characteristic	Sym	Notes	Min	Typ	Max	Units	
Nominal Center Frequency	f_c	1	71.000			MHz	
Passband	Insertion Loss at f_c	1, 2		6	8.0	dB	
	3 dB Passband		BW_3	± 100	± 140	± 200	kHz
	Amplitude Ripple over $f_c \pm 80$ kHz					1.5	dB _{p-p}
	Group Delay Variation over $f_c \pm 50$ kHz		GDV		300	1000	ns _{p-p}
	Absolute Group Delay	GD		2.8		μ s	
Rejection	$f_c - 600$ to $f_c - 400$ and $f_c + 400$ to $f_c + 600$ MHz	1, 2, 3	25	26		dB	
	$f_c - 1.0$ to $f_c - 0.6$ and $f_c + 0.6$ to $f_c + 1.8$ MHz		35	40			
	69.6 to 70.0 MHz		40	45			
	31 to 69.6 and 71.8 to 111 MHz		35	50			
Operating Temperature Range	T_A	1	-40		+85	°C	

Impedance Matching to 50 Ω unbalanced	External L-C
Case Style	SMP-87 22.1 X 8 mm Nominal Footprint
Lid Symbolization (YY=year, WW=week)	RFM SF1081A-1 YYWW

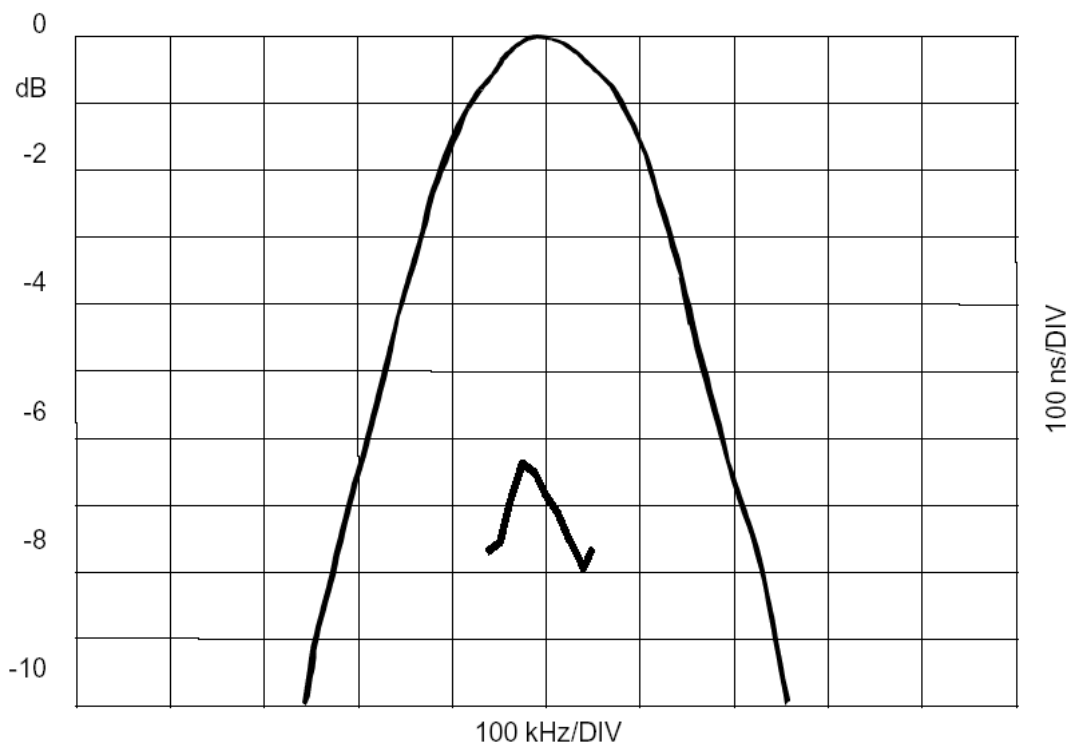
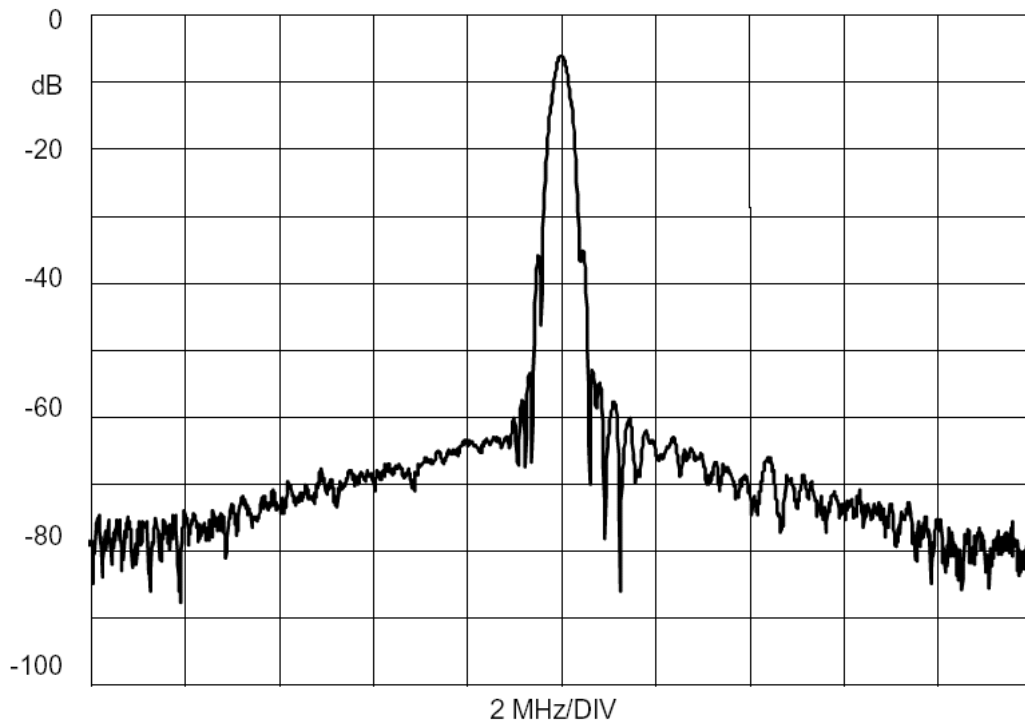
Electrical Connections

Connection	Terminals
Port 1 Hot	1
Port 1 Gnd Return	10
Port 2 Hot	6
Port 2 Gnd Return	5
Case Ground	All Others

Notes:

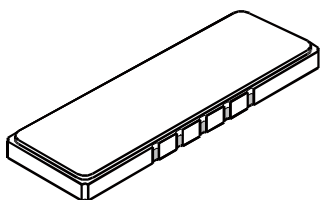
1. Unless noted otherwise, all specifications apply over the operating temperature range with filter soldered to the specified demonstration board with impedance matching to 50 Ω and measured with 50 Ω network analyzer.
2. Unless noted otherwise, all frequency specifications are referenced to the nominal center frequency, f_c .
3. Rejection is measured as attenuation below the minimum IL point in the passband. Rejection in final user application is dependent on PCB layout and external impedance matching design. See Application Note No. 42 for details.
4. "LRIP" or "L" after the part number indicates "low rate initial production" and "ENG" or "E" indicates "engineering prototypes."
5. The design, manufacturing process, and specifications of this filter are subject to change.
6. Either Port 1 or Port 2 may be used for either input or output in the design. However, impedances and impedance matching may vary between Port 1 and Port 2, so that the filter must always be installed in one direction per the circuit design.
7. US and international patents may apply.
8. RFM, stylized RFM logo, and RF Monolithics, Inc. are registered trademarks of RF Monolithics, Inc.
9. ©Copyright 1999, RF Monolithics Inc.
10. Electrostatic Sensitive Device. Observe precautions for handling 

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SMP-87 Case

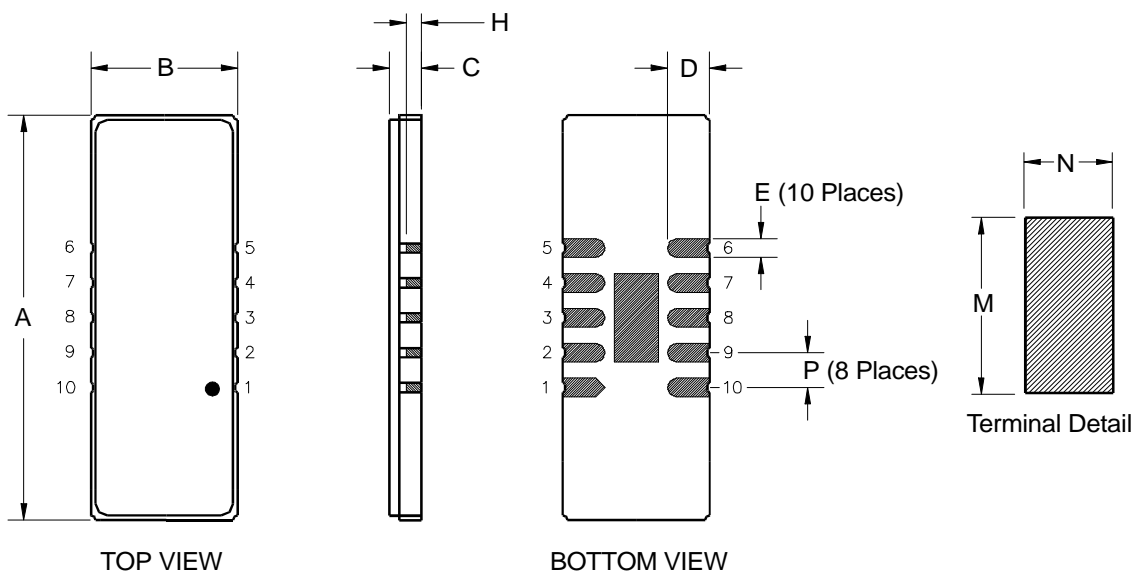
10-Terminal Ceramic Surface-Mount Case 22.1 x 8 mm Nominal Footprint



Case Dimensions						
Dimension	mm			Inches		
	Min	Nom	Max	Min	Nom	Max
A	21.90	22.10	22.40	0.862	0.870	0.882
B	7.80	8.00	8.30	0.307	0.315	0.327
C		1.78	2.00		0.070	0.079
D		2.29			0.090	
E		1.02			0.040	
H		1.0			0.039	
M		4.83			0.190	
N		2.41			0.095	
P		1.905			0.075	

Materials	
Solder Pad Termination	Au plating 30 - 60 μinches (76.2-152 μm) over 80-200 μinches (203-508 μm) Ni.
Lid	Fe-Ni-Co Alloy Electroless Nickel Plate (8-11% Phosphorus) 100-200 μinches Thick
Body	Al ₂ O ₃ Ceramic
Pb Free	

Electrical Connections		
Connection		Terminals
Port 1	Input or Return	10
	Return or Input	1
Port 2	Output or Return	5
	Return or Output	6
Ground		All others
Single Ended Operation		Return is ground
Differential Operation		Return is hot

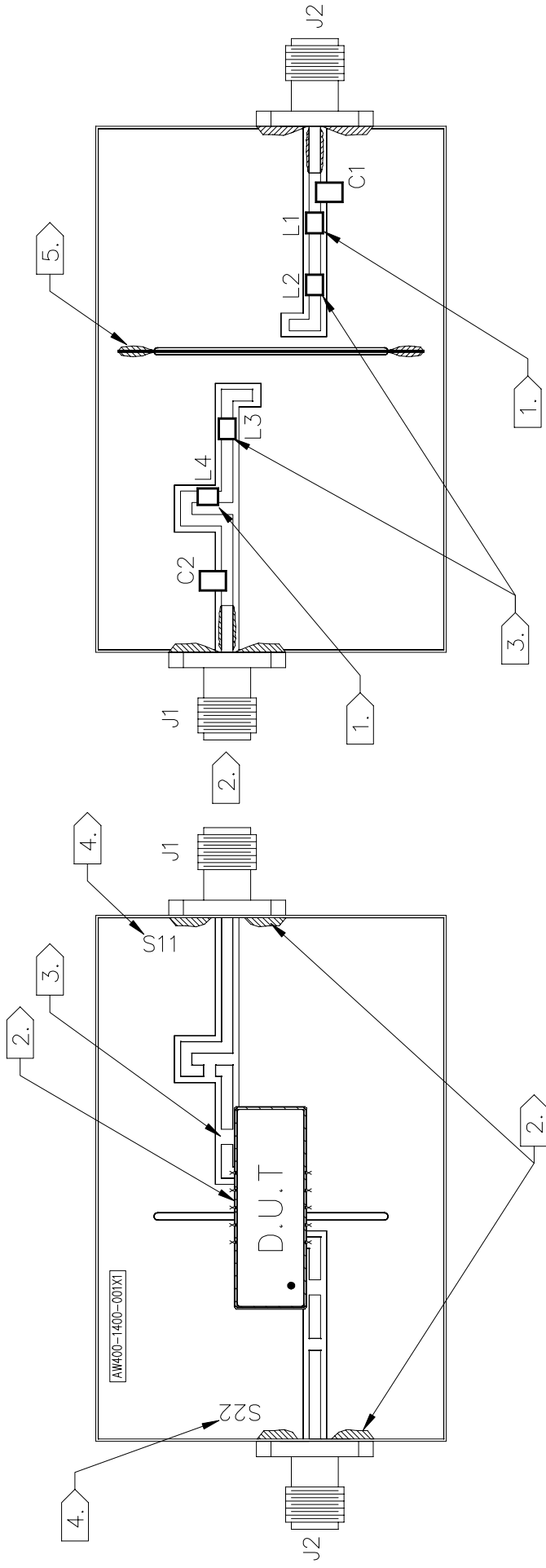


REV	ECN NO.	DESCRIPTION	DATE
A	7160	INITIAL RELEASE	9 NOV 98

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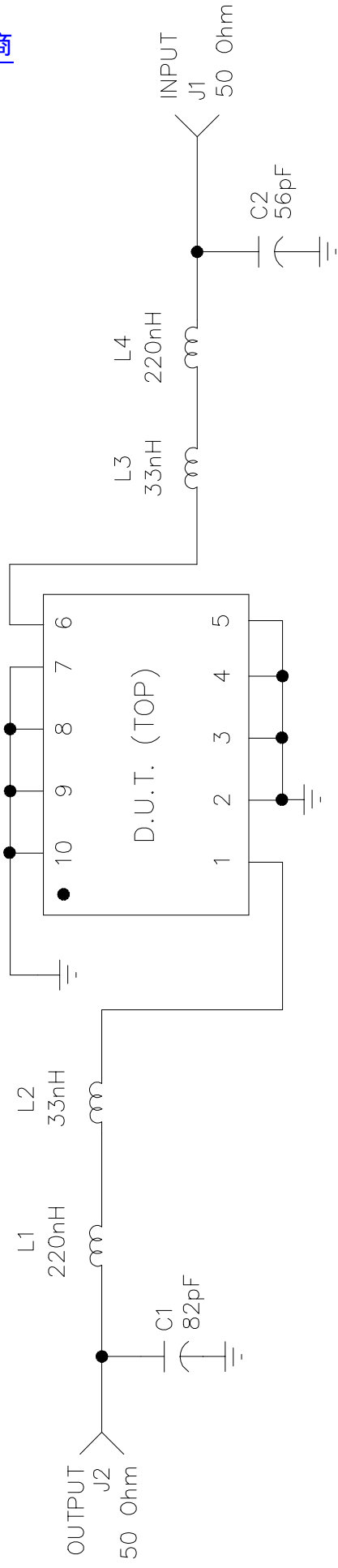
NOTES:

1. NOTE PROPER ORIENTATION OF INDUCTORS L1 & L4. THEY ARE TO BE POSITIONED 90° TO EACH OTHER.
2. SOLDER SURFACE MOUNT PACKAGE TO TEST SIDE OF PCB. SOLDER 10 PLACES AND CONNECTORS AS SHOWN.
3. CUT TRACES ON BOTH SIDES OF THE PCB BETWEEN THE SAME HOLES TO PROVIDE GAP FOR L2 & L3.
4. LABEL BOARD USING ELECTRONIC METHOD.
5. CUT SHIELD TAB SO THAT IT IS EVEN WITH TEST SIDE. SOLDER AS SHOWN.



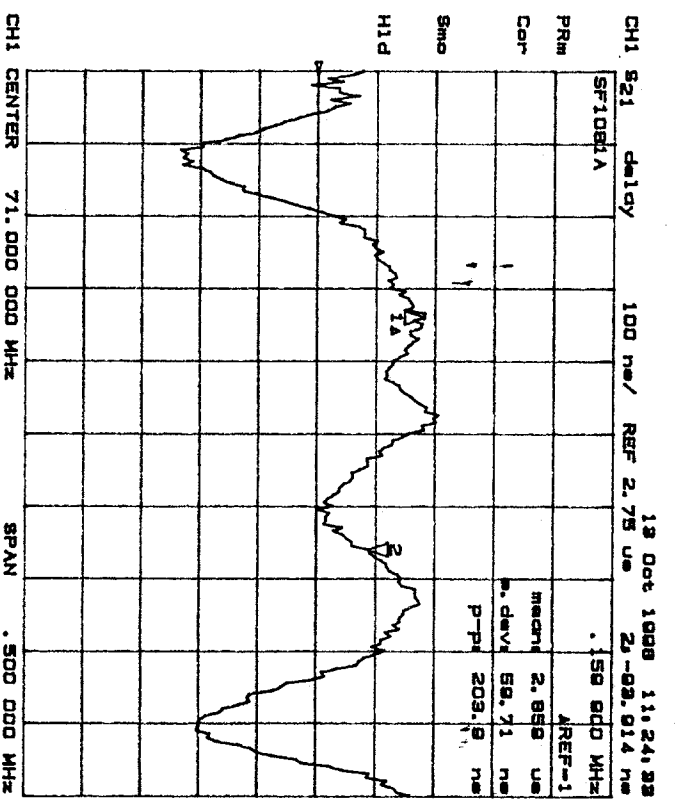
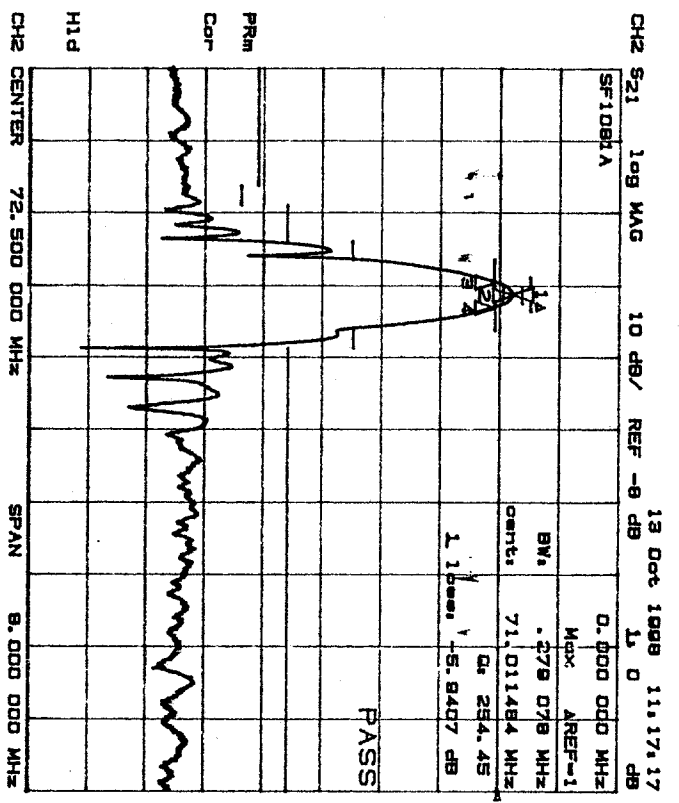
DRAWN BY/DATE:	L. ASHMORE 9 NOV98	TITLE:	ASSEMBLY, SF1081A-1-DEMO
RF Monolithics, Inc.	CHECKED/APPROVED	SIZE	CODE IDENT
DALLAS, TEXAS 75244		A	2U874
		DWG. NO.	SF1081A-1-000
		REV	A
		SHEET	1/3

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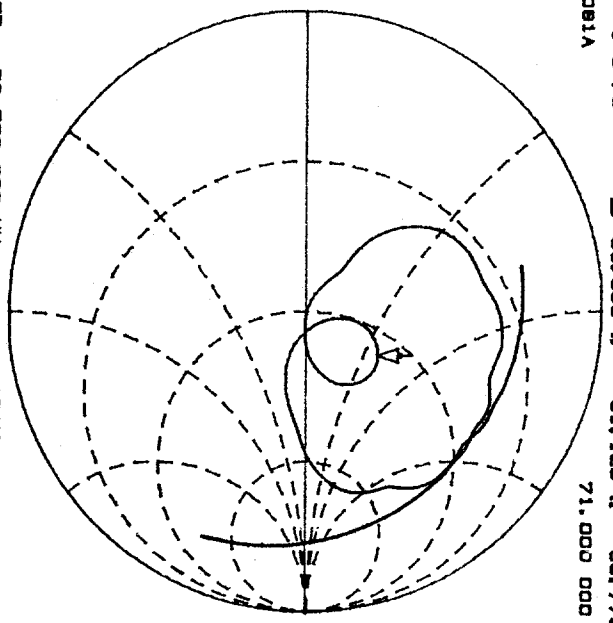
DemO

B.C
 10/13/98

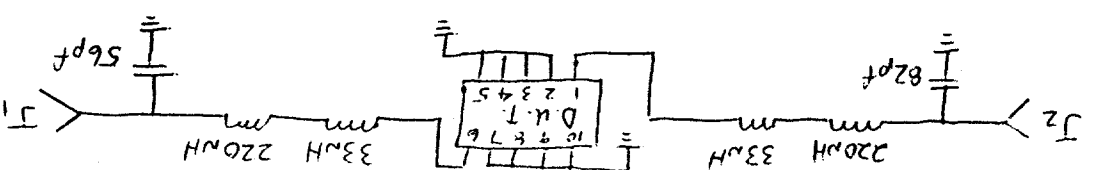
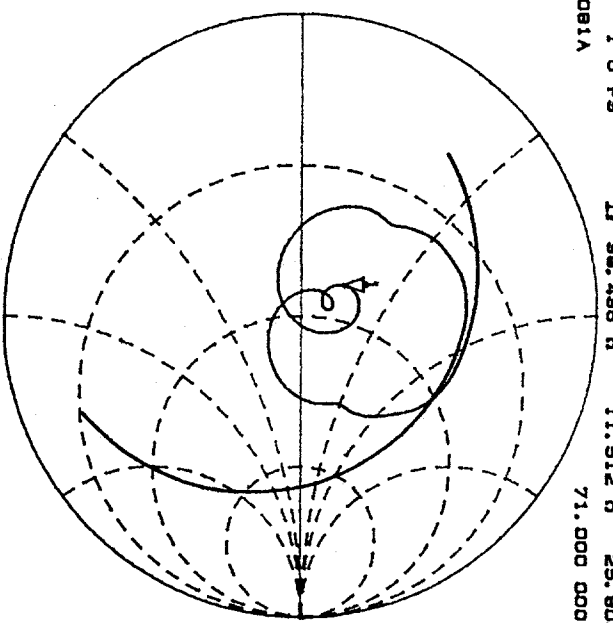


查询"SF1081A-1"供应商

CH2 S11 1 U FS 13 Oct 1998 11:20:28
 SF1081A 1 58.888 0 31.128 0 89.779 MHz
 71.000 000 MHz



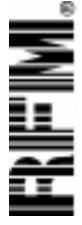
CH2 S22 1 U FS 13 Oct 1998 11:21:35
 SF1081A 1 39.488 0 11.912 0 25.805 MHz
 71.000 000 MHz



BILL OF MATERIALS

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<u>PART IDENTIFIER</u>	<u>DESCRIPTION 1</u>	<u>DESCRIPTION 2</u>	<u>QTY/ASSY</u>	<u>REFERENCE DESCRIPTION</u>
SF1081A-1-DEMO	DEMO BOARD,SF1081A-1			
400-1400-001	PCB,DEMO BOARD,SF1081A		1.0000	
400-0533-001	SHIELD,TO-39 TEST FIXTURE		1.0000	
500-0319-001	TAPE,COPPER FOIL,SCOTCH	TYPE 1181,44F3260,1/2"	0	
SF1081A-1-LRIP	FILTER,SM,71.000MHZ		1.0000	
SF1081A-1-000	ASSY DIAGRAM,DEMO BOARD,	SF1081A-1	0	
500-0003-820	CAP,CHIP,NPO,82(J),STD		1.0000	C 1
500-0003-560	CAP,CHIP,NPO,56(J),STD		1.0000	C 2
500-0248-001	CONN,COAX,FLANGE MT.JACK	4 HOLE	2.0000	J 1,2
500-0010-221	IND,CHIP;1008CS,220NH,10%		2.0000	L 1,4
500-0010-330	IND,CHIP;1008CS,33NH,10%		2.0000	L 2,3



SIZE **A**

FSCM NO. **2U874**

DWG NO. **SF1081A-1-DEMO**

SCALE **NONE**

W/O or ECN

7160

REV **A**

SHEET **1**

OF **2**

REV HISTORY

REV	ECN	DATE	DESCRIPTION
A	7160	11/02/98	INITIAL RELEASE

[查询"SF1081A-1"供应商](#)



SCALE **NONE**

SIZE **A**
FSCM NO. **2U874**
W/O or ECN **7160**

DWG NO. **SF1081A-1-DEMO**
REV **A** SHEET **2** OF **2**