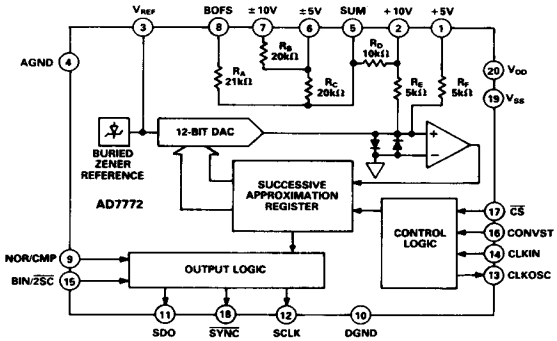
LC²MOS Serial Output 12-Bit ADC

AD7772

FEATURES

12-Bit Resolution and Accuracy
Fast Conversion Time: 10μs
Serial Output
Complete with On-Chip Reference
Low Power
Unipolar or Bipolar Input Ranges
Small 0.3", 20-Pin DIPs and 20-Terminal Surface Mount Package

AD7772 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7772 is a complete 12-bit ADC that offers high speed performance combined with low, CMOS power levels. It uses an accurate, high speed DAC and comparator in a successive approximation loop to achieve a fast conversion time. An on-chip, buried Zener diode provides a stable reference voltage to give low drift performance over the full temperature range, and the specified accuracy is achieved without any user trims. The AD7772 can be configured to have analog input ranges of 0 to +5V, 0 to +10V, ±5V or ±10V.

An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation. Alternatively, the clock input may be driven from an external clock source such as a divided-down microprocessor clock.

The AD7772 serial interface is compatible with digital signal processors such as the TMS32020, μPD7720 and DSP56000. It can also be used with general purpose serial to parallel converters such as shift registers. The device outputs the conversion result with one leading zero and the twelve data bits following. When using the AD7772 at top speed (CLKIN = 1.28MHz) with a 3μs sample-and-hold amplifier like the AD585, it is possible to achieve throughput rates of 76kHz. With this 76kHz sample rate signals with spectral contents up to 38kHz can be digitized.

The AD7772 is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

PRODUCT HIGHLIGHTS

1. Fast, 10μs conversion time makes the AD7772 ideal for a wide range of applications in telecommunications, sonar and radar signal processing and industrial data acquisition systems requiring optical isolation.
2. Where space saving is important, the small package and serial interface of the AD7772 minimize the amount of board space needed to realize 12-bit data acquisition.
3. The versatile serial interface on the AD7772 makes it simple to interface to the serial ports of DSPs as well as other microprocessor systems.
4. On-chip buried Zener reference has temperature coefficient as low as 25ppm/°C, giving low full-scale drift over the operating temperature range.
5. Stable DAC and comparator give excellent linearity and low zero error over the full temperature range.
6. LC²MOS circuitry gives low power drain (135mW) from +5V, −15V supplies.

SPECIFICATIONS (V_{DD} = +5V ±5%, V_{SS} = −15V ±5%, f_{CLK} = 1.28MHz. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	K, B Versions[1]	L Version[1]	C Version[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity @ 25°C	±1	±1/2	±1/2	LSB max	Tested Range: 0 to +5V
T_{min} to T_{max}	±1	±1/2	±3/4		
Differential Nonlinearity	±1	±1	±1	LSB max	No Missing Codes Guaranteed T_{min} to T_{max}
Unipolar Offset Error @ +25°C	±8	±4	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±8	±4	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Full Scale Error[2] @ +25°C	±15	±10	±10	LSB max	Input Range: 0 to 5V or 0 to 10V
Bipolar Zero Error @ +25°C	±9	±5	±5	LSB max	Input Range: ±5V or ±10V
T_{min} to T_{max}	±15	±9	±9	LSB max	
Bipolar Full Scale Error[2] @ +25°C	±10	±7	±7	LSB max	Input Range: ±5V or ±10V
Full Scale TC[3,4]	±45	±35	±35	ppm/°C max	
ANALOG INPUTS					
Input Ranges					
Unipolar	0 to +5	0 to +5	0 to +5	Volts	
	0 to +10	0 to +10	0 to +10	Volts	
Bipolar	−5 to +5	−5 to +5	−5 to +5	Volts	
	−10 to +10	−10 to +10	−10 to +10	Volts	
Input Current					
Unipolar	3	3	3	mA max	Input Range: 0 to 5V or 0 to 10V
Bipolar	±0.4	±0.4	±0.4	mA max	Input Range: ±5V to ±10V
INTERNAL REFERENCE VOLTAGE					
V_{REF} Output @ +25°C	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	V_{min}/V_{max}	−5.25V ±1%
V_{REF} Output TC	±40	±25	±25	ppm/°C typ	
Output Current Sink Capability[5]	550	550	550	µA max	(External Load Should Not Change During Conversion.)
POWER SUPPLY REJECTION					
V_{DD} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{SS} = −15V V_{DD} = +4.75V to +5.25V
V_{SS} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{DD} = +5V V_{SS} = −14.25V to −15.75V
LOGIC INPUTS					
$\overline{CS}$, NOR/CMP, BIN/$\overline{2SC}$					
CONVST, CLKIN					
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	V min	
C_{IN}[5], Input Capacitance	10	10	10	pF max	
$\overline{CS}$, NOR/CMP, BIN/$\overline{2SC}$					
CONVST					
I_{IN}, Input Current	±10	±10	±10	µA max	V_{IN} = 0 to V_{DD}
CLKIN					
I_{IN}, Input Current	±20	±20	±20	µA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS					
SDO, SCLK, CLKOSC, $\overline{SYNC}$					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200µA
Floating State Leakage Current	±10	±10	±10	µA max	
SDO					
Floating State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME	10.2	10.2	10.2	µs max	f_{CLK} = 1.28MHz. See Control Inputs Synchronization.
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	VNOM	±5% for Specified Performance
V_{SS}	−15	−15	−15	VNOM	±5% for Specified Performance
I_{DD}[6]	7	7	7	mA max	$\overline{CS}$ = CONVST = V_{DD}, AIN = 5V
I_{SS}[6]	12	12	12	mA max	$\overline{CS}$ = CONVST = V_{DD}, AIN = 5V
Power Dissipation	135	135	135	mW typ	
	215	215	215	mW max	

NOTES
[1]Temperature range as follows: K, L versions: 0 to +70°C
B, C versions: −25°C to +85°C
[2]Includes internal voltage reference error.
[3]Full Scale TC = $\Delta FS/\Delta T$, where ΔFS is Full Scale change from T_A = +25°C to T_{min} or T_{max}.
[4]Includes internal voltage reference drift.
[5]Sample tested to ensure compliance.
[6]Power supply current is measured when AD7772 is inactive, i.e., $\overline{CS}$ = CONVST = $\overline{SYNC}$ = HIGH.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V, V_{SS} = −15V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Units	Conditions/Comments
t_1[2]	780	780	ns min	CLKIN Cycle Time
t_2	40	50	ns max	Propagation Delay between CLKIN and CLKOSC
t_3	545	560	ns max	Propagation Delay between CLKIN and SCLK
t_4[3]	780	780	ns min	SCLK Cycle Time
t_5	45	45	ns min	$\overline{CS}$ to CONVST Setup Time
t_6[3]	0	0	ns min	$\overline{CS}$ to $\overline{SYNC}$ Hold Time
t_7	40	50	ns min	CONVST Pulse Width
t_8	50	50	ns max	SCLK ↓ to $\overline{SYNC}$ ↑ Delay
t_9	60	65	ns max	SCLK ↓ to $\overline{SYNC}$ ↓ Delay
t_{10}[4]	50	50	ns max	SCLK ↓ to SDO ↑ Delay, C_L = 20pF
	100	125	ns max	SCLK ↓ to SDO ↑ Delay, C_L = 100pF
t_{11}[4]	115	145	ns max	SCLK ↓ to Data Valid, C_L = 20pF
	190	235	ns max	SCLK ↓ to Data Valid, C_L = 100pF
t_{12}[5]	10	10	ns min	SCLK ↓ to SDO High Impedance
	65	80	ns max	

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]CLKIN Mark/Space Ratio Range is 55/45 to 45/55.
[3]SCLK and $\overline{SYNC}$ are loaded with the circuit of Figure 1.
[4]t_{10} and t_{11} are measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.
[5]t_{12} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 3.
Specifications subject to change without notice.

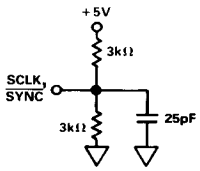
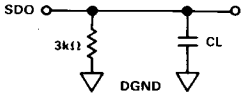
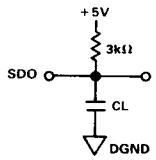


Figure 1. SCLK, $\overline{SYNC}$ Load Circuit

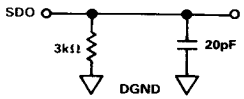


a. To V_{OH} (t_{11})

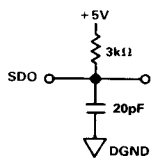


b. To V_{OL} (t_{10}, t_{11})

Figure 2. Load Circuits for t_{10}, t_{11} Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 3. Load Circuits for Bus Relinquish Time Test (t_{12}).

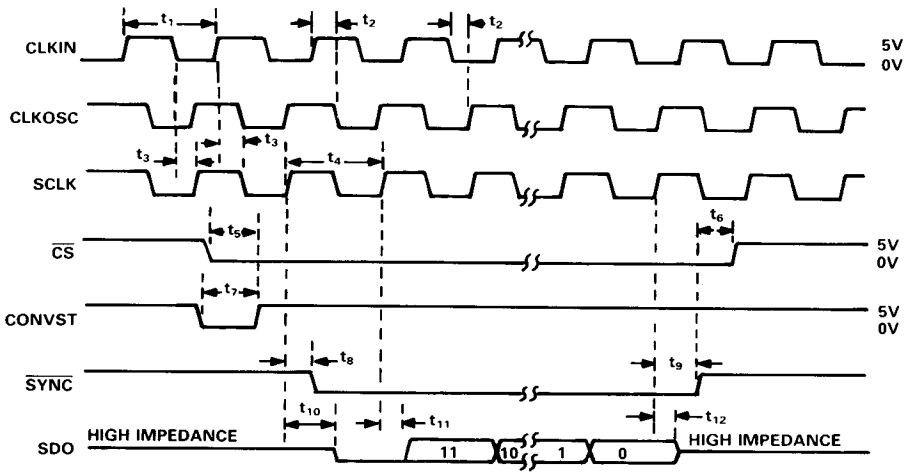


Figure 4. AD7772 Timing Diagram.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3V to +7V
V_{SS} to DGND . . . . . +0.3V to −17V
AGND to DGND . . . . . −0.3V to V_{DD} +0.3V
Analog Input Voltage to AGND
(BOFS, ±10V, ±5V, SUM,
+10V, +5V) . . . . . −15V to +15V
Digital Input Voltage to DGND
(CLK IN, $\overline{CS}$, CONVST, NOR/CMP,
BIN/$\overline{2SC}$) . . . . . −0.3V to V_{DD} +0.3V
Digital Output Voltage to DGND
(SDO, SCLK, $\overline{SYNC}$, CKOSC) . . . −0.3V to V_{DD} +0.3V

Operating Temperature Range
Commercial (K, L Versions) . . . . . 0 to +70°C
Industrial (B, C Versions) . . . . . −25°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

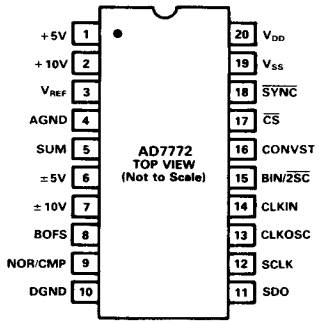
ORDERING INFORMATION[1]

Full Scale TC	Accuracy Grade	0 to +70°C	−25°C to +85°C
		Plastic DIP[2] (N-20)	**Hermetic[2] (Q-20)**
45ppm/°C	±1LSB	AD7772KN	AD7772BQ
35ppm/°C	±1/2LSB	AD7772LN	AD7772CQ
		PLCC (P-20A)[2,3]	
45ppm/°C	±1LSB	AD7772KP	
35ppm/°C	±1/2LSB	AD7772LP	

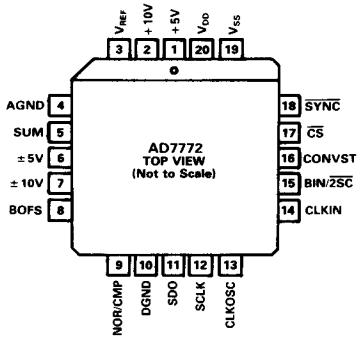
NOTES
[1]Analog Devices reserves the right to ship either ceramic or cerdip hermetic packages.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	+5V	Analog Input Pin. This is connected as in Figure 9 to provide a +5V analog input range.
2	+10V	Analog Input Pin. This is connected as in Figure 11 to provide a +10V analog input range.
3	V_{REF}	Voltage Reference Output. The AD7772 has its own internal −5.25V reference.
4	AGND	Analog Ground
5	SUM	Analog Input Pin. This is connected to the inverting terminal of an op amp for ±5V to ±10V analog input ranges. See Figure 13.
6	±5V	Analog Input Pin. Figure 13 shows how this is connected for a ±5V analog input range.
7	±10V	Analog Input Pin. For ±10V analog input range see Figure 13.
8	BOFS	Bipolar Offset Pin. This is tied to V_{REF} for either of the bipolar analog input ranges. See Figure 13.
9	NOR/CMP	NOR/CMP and BIN/$\overline{2SC}$ determine the format of the output data. See Table I.
10	DGND	Digital Ground
11	SDO	Serial Data Output
12	SCLK	Continuously running Serial Clock Output.
13	CLKOSC	Clock Oscillator Pin. An inverted CLKIN signal appears at CLKOSC when external clock is used. See CLKIN (Pin 14) description for crystal (resonator).
14	CLKIN	Clock Input Pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be applied between CLKIN and CLKOSC. See Figure 7.
15	BIN/$\overline{2SC}$	BIN/$\overline{2SC}$ and NOR/CMP determine the output data format. See Table I.
16	CONVST	Conversion Start Input. This signal starts a conversion on its rising edge when $\overline{CS}$ is low.
17	$\overline{CS}$	Chip Select Input. This active low signal, in conjunction with CONVST, starts a conversion.
18	$\overline{SYNC}$	This is the framing signal for the serial data output. It goes low on the first rising edge of SCLK after conversion begins and goes high when conversion is complete.
19	V_{SS}	Negative Supply, −15V
20	V_{DD}	Positive Supply, +5V

NOR/CMP	BIN/$\overline{2SC}$	Unipolar Data Format	Bipolar Data Format
0	0	2s Complement	Complementary 2s Complement
0	1	Straight Binary	Complementary Offset Binary
1	0	Complementary 2s Complement	2s Complement
1	1	Complementary Binary	Offset Binary

Table I. AD7772 Output Coding

TERMINOLOGY

LEAST SIGNIFICANT BIT
An ADC with 12-bit resolution can resolve one part in 2^{12} (1/4096 of full scale). For the AD7772 operating in the 0 to +5V range, 1LSB is 1.22mV.

NO MISSING CODES
A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For all grades of the AD7772, all 4096 codes are present over the entire operating temperature ranges.

UNIPOLAR OFFSET ERROR
For the unipolar analog input range, the first transition should occur at a level 1/2LSB above AGND. Unipolar offset error is defined as the deviation of the actual transition from that point. This error can be adjusted as explained further on in this data sheet.

BIPOLAR ZERO ERROR
In the bipolar analog input ranges, bipolar zero is defined as the middle of code 2048. Bipolar zero error is the actual deviation from that point. The circuit diagram on page 9 shows how to adjust this.

UNIPOLAR FULL SCALE ERROR
The last transition in the ADC (from 111 . . .110 to 111 . . .111 when using straight binary coding) should occur for an analog value 1 1/2LSB below the nominal full scale (4.99816 for 5.000 volts full scale). The full scale error is the deviation of the actual level at the last transition from the ideal level with unipolar offset error adjusted to zero. This error can be trimmed out as shown in Figure 12. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal −5.25 volts reference.

BIPOLAR FULL SCALE ERROR
In the bipolar mode, the ADC has a positive full scale error and a negative full scale error. Positive full scale error is the deviation of the actual level at the last transition from the ideal level, with bipolar zero error adjusted to zero. Negative full scale error is the deviation of the actual level at the first transition from the ideal level, with bipolar zero error adjusted to zero. Full scale error is defined as either positive full scale error or negative full scale error, whichever is largest.

CIRCUIT INFORMATION

CONVERTER DETAILS

Conversion start on the AD7772 is controlled by the $\overline{CS}$ and CONVST inputs. Figure 5 shows the operating signals of interest. With $\overline{CS}$ held permanently low, a positive-going edge on CONVST starts the conversion cycle. The successive approximation register (SAR) is reset at this stage. On the next rising edge of SCLK, the $\overline{SYNC}$ output goes low and the three-state data output (SDO) is enabled.

During conversion, the internal 12-bit DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output against the analog input. The MSB decision is made and latched to the serial data output 90ns (typically) after the second rising edge of SCLK following the conversion start. Similarly, the succeeding bit decisions are made and latched approximately 90ns after the SCLK rising edges. When conversion is complete, the SDO output is latched to the high impedance state and the $\overline{SYNC}$ output goes high.

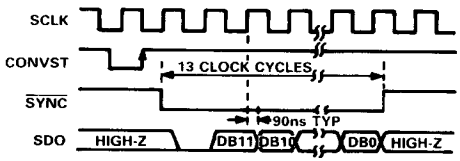


Figure 5. Operating Waveforms Using an External Clock Source for CLKIN

CONTROL INPUTS SYNCHRONIZATION

Conversion time for the AD7772 is defined as the time for which the $\overline{SYNC}$ output is low. This is always 13 clock cycles. However, there is a delay between CONVST going high and $\overline{SYNC}$ going low. Without synchronization this delay can vary from zero to an entire clock period. If a constant delay is required here, then the following approach can be used: when starting a conversion CONVST must go high on either the rising edge of CLKIN or the falling edge of CLKOSC.

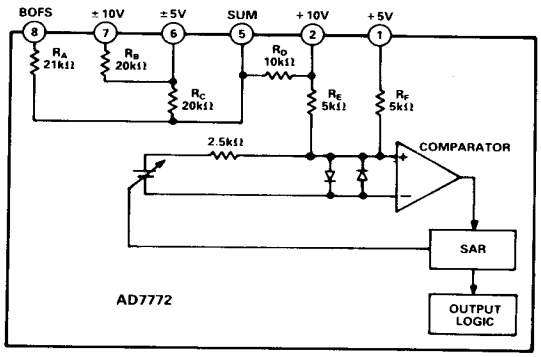


Figure 6. AD7772 Analog Input Stage

DRIVING THE ANALOG INPUT

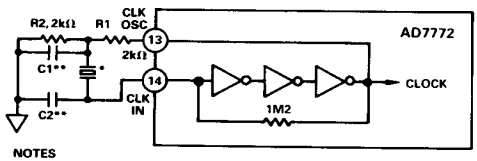
Figure 6 shows the analog input stage for the AD7772. There are four application resistors (R_A, R_B, R_C and R_D). These can be used with one external op amp to implement ±5V and ±10V analog input ranges. R_A is always connected to V_{REF} for these ranges and offsets the input signal by +2.5V. R_C and R_D provide an attenuation of 2 for the ±5V input while R_B, R_C and R_D attenuate the ±10V input by 4. The external op amp is connected as an inverting amplifier with its output driving Pins 1 and 2 and R_D as the feedback resistor. Figure 13 shows the circuit configuration.

The +5V and +10V inputs on the AD7772 connect to the comparator input via the 5kΩ resistors R_E and R_F. The DAC which has 2.5kΩ output impedance also connects to this point. During conversion, current from the analog input is modulated by the DAC output current at a rate equal to the CLKIN frequency (1.28MHz maximum). This causes voltage spikes (glitches) to appear at the analog input. The magnitude and settling time of these glitches depends on the open-loop output impedance and small signal bandwidth of the amplifier or sample-and-hold driving the input. These devices must have sufficient drive to ensure that the glitches have settled within one clock period. An example of a suitable op amp is the AD OP-27. The magnitude of the largest glitch when using this device to drive the analog input is typically 11mV with a 200ns settling time.

Suitable devices capable of driving the AD7772 analog inputs are the AD OP-27 and AD711 op amps and the AD585 sample-and-hold.

INTERNAL CLOCK OSCILLATOR

Figure 7 shows the AD7772 internal clock circuit. A crystal or ceramic resonator may be connected as in Figure 7 to provide a clock oscillator for the ADC timing. Resistors R1 and R2 ensure that the CLKIN mark/space ratio stays between 45/55 and 55/45. Alternatively, the crystal/resonator may be omitted and an external clock source connected to CLKIN. The mark/space ratio of the external clock must be in the range 45/55 to 55/45. An inverted CLKIN signal will appear at the CLKOSC output pin.



NOTES
*1.28MHz CRYSTAL/CERAMIC RESONATOR.
**C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30pF TO 100pF.

Figure 7. AD7772 Internal Clock Circuit

INTERNAL REFERENCE

The AD7772 has an on-chip, buffered, temperature compensated, buried Zener reference, which is factory trimmed to −5.25V ±1%. It is internally connected to the DAC and is also available at Pin 3 to sink up to 550μA current from an external load.

For minimum code transition noise, the reference output should be decoupled with a capacitor to filter out wideband noise from the reference diode (10μF tantalum in parallel with 100nF ceramic). However, large values of decoupling capacitors can affect the dynamic response and stability of the reference amplifier. A 10Ω resistor in series with the decoupling capacitors will eliminate this problem without adversely affecting the filtering effect of the capacitors. A simplified schematic of the reference with its recommended decoupling components is shown in Figure 8.

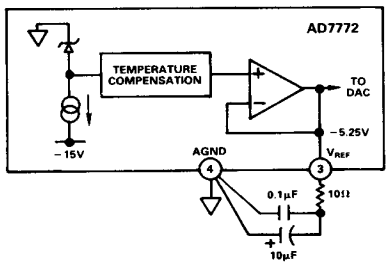


Figure 8. AD7772 Internal −5.25V Reference

APPLYING THE AD7772

The AD7772 has a flexible input stage with application resistors which can be configured for various analog input ranges. The following sections show the AD7772 configured for these ranges.

UNIPOLAR OPERATION

Figure 9 shows the AD7772 connected for the unipolar 0 to +5V input range. The ideal input/output characteristic for this range is given in Figure 10. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, 5/2LSBs . . .FS − 3/2LSBs). The output code is straight binary (see Table I) with an LSB size of FS/4096 = 5/4096V = 1.22mV. To change to complementary binary coding, NOR/CMP should be tied to +5V.

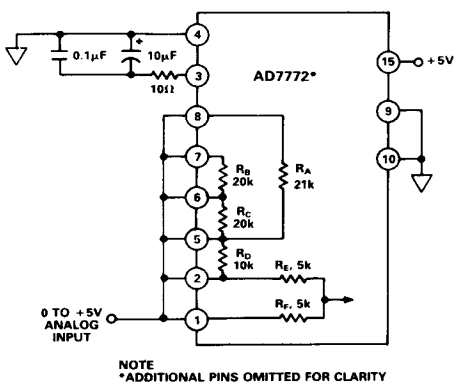


Figure 9. Unipolar 0 to +5V Input Range

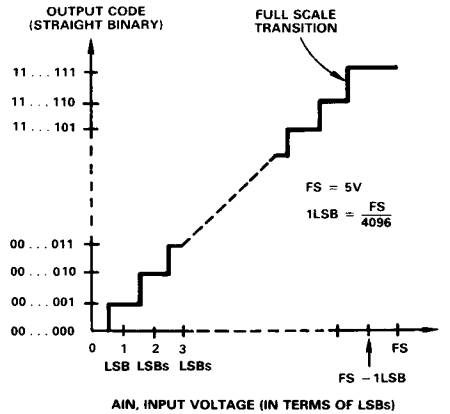


Figure 10. Ideal Input/Output Transfer Characteristic for Figure 9

Figure 11 shows how the AD7772 can be connected for a 0 to +10V input range. The +5V pin is now connected to 0V, thereby attenuating the input by 2 and effectively doubling the analog input range. The analog input is applied to the +10V pin. For this circuit, the LSB size is FS/4096 = 10/4096V = 2.44mV and the coding is straight binary.

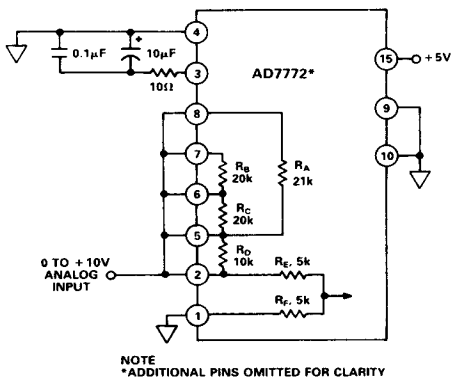


Figure 11. AD7772 in 0 to +10V Analog Input Range

UNIPOLAR OFFSET AND FULL SCALE ERROR ADJUSTMENT

If absolute accuracy is an application requirement, then offset and full scale error can be adjusted to zero. Offset error must be adjusted before full scale error. Figure 12 shows the extra components required for full scale error adjustment. The analog input range is 0 to +5V and the coding is straight binary. Zero offset is achieved by adjusting the offset of the op amp driving the analog input (i.e., A1 in Figure 12). For zero offset error apply 0.61mV (+1/2LSB) to V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 . . . 0000 and 000 . . . 0001.

To adjust the full scale error, apply an analog input of 4.99817V (FS − 3/2LSBs) to V_{IN} and adjust R1 until the ADC output code flickers between 1111 . . . 1110 and 1111 . . . 1111.

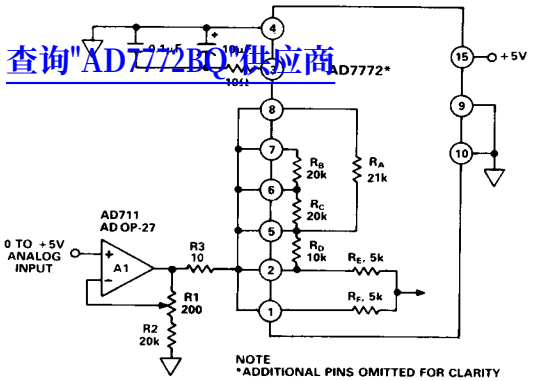


Figure 12. Unipolar 0 to +5V Operation with Full-Scale Error Adjust

BIPOLAR OPERATION

Figure 13 shows the circuit configuration for implementing ±5V and ±10V analog input voltages on the AD7772. R_A and R_D offset the input signal by a constant +2.5V while R_C and R_D provide attenuation for the ±5V input. R_B, R_C and R_D provide attenuation for the ±10V input. If a ±5V input range is needed, the input signal should be applied to Pin 6 (±5V) and Pin 7 left unconnected. For a ±10V input range, apply the signal to Pin 7 (±10V) and leave Pin 6 open circuit. The output code format is offset binary. Figure 14 shows the ideal input/output characteristic for the ±5V input range.

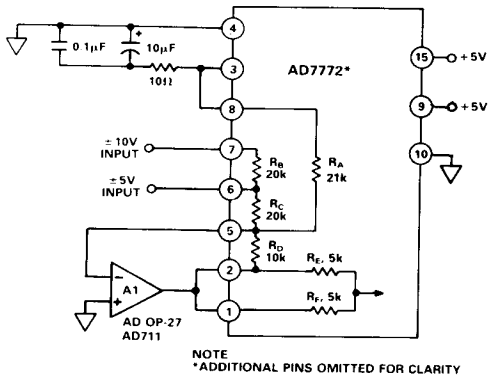


Figure 13. AD7772 Connected for ±5V/±10V Input Range

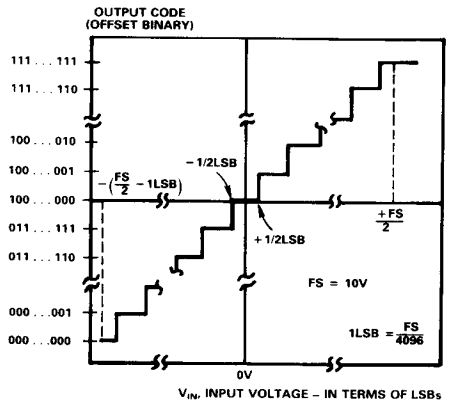


Figure 14. Ideal Input/Output Transfer Characteristic for the Bipolar Circuit of Figure 13

BIPOLAR OFFSET AND FULL SCALE ERROR ADJUSTMENT

In measurement applications where absolute accuracy is required, offset and full scale error can be adjusted to zero. Figure 15 shows how the ±5V input range circuit is modified to do this. By placing R3 in parallel with the op amp feedback resistance R_D and the R1, R2 combination in parallel with R_C, an adjustment range of ±16LSBs is possible.

Bipolar zero error must be adjusted before full scale error. This is achieved by applying an analog input of +1.22mV (+1/2LSB) at the ±5V input pin and adjusting the op amp offset until the ADC output code flickers between 1000 . . . 0000 and 1000 . . . 0001.

For full scale error adjustment, the analog input must be at 4.99878 volts (i.e., FS/2 – 1/2LSB or last transition point). Then R1 is adjusted until the output code flickers between 1111 . . . 1110 and 1111 . . . 1111.

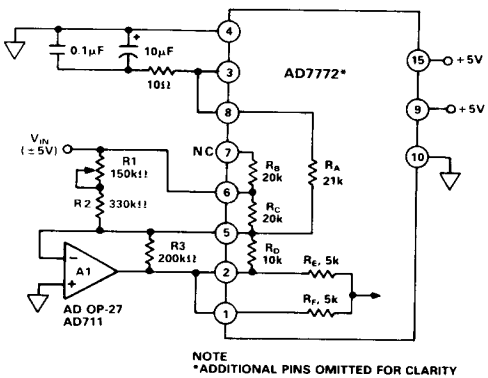


Figure 15. AD7772 Connected for ±5V Input Range with Full-Scale Error Adjust

INTERFACING

The AD7772 is a serial output device, making it suitable for use with digital signal processors which have a serial port (TMS32020, DSP56000, etc.) as well as microcontrollers (8051, 6803) and shift registers. See Figure 4 for the timing diagram. The serial data is placed on the SDO pin as conversion is taking place. Each data bit is valid on the falling edge of SCLK, and the complete word is framed by the SYNC pulse.

TMS32020/TMS320C25 INTERFACE

Figure 16 shows the circuit for interfacing the AD7772 to the TMS32020/TMS320C25 Serial Port. The AD7772 has CS tied permanently low. In a sampling system, the SAMPLE TIMER would control the start of conversion. When the system is non-sampling, this CONVST pulse could be software-controlled by the processor. When conversion begins, the SYNC output goes low. This enables the serial input of the TMS32020/TMS320C25 which now accepts the data appearing at DR on each negative-going edge of CLKR. After sixteen CLKR pulses the internal interrupt (RINT) is automatically set. The service routine for this interrupt then reads the conversion result from the DRR (data receive register) into the accumulator or memory. Note that the word in the DRR must be shifted right three times in order to get the

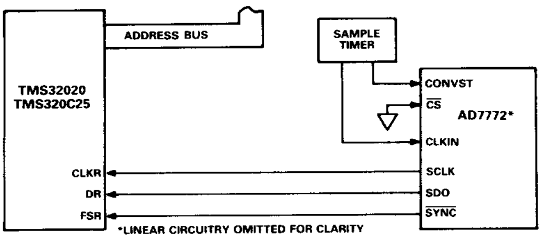


Figure 16. AD7772 to TMS32020/TMS320C25 Interface

standard right-justified data format. This is also the case in the other processor interfaces which follow.

NEC µPD7720/µPD77230 INTERFACE

Figure 17 shows an interface circuit for the NEC µPD7720 digital signal processor. Unlike the FSR input on the TMS320 processors, the SIEN input on the µPD7720/µPD77230 is level sensitive rather than edge sensitive. Because the processor can only be configured for either 8-bit or 16-bit data transfers, the SIEN input to the µPD7720/µPD77230 must be at least 16 clock pulses wide to receive the 12-bit conversion result from the AD7772. The circuitry of Figure 17 accomplishes this by using the CONVST and SYNC signals as the set and reset controls on an S-R flip-flop.

In Figure 17 the processor controls the start of conversion. CS is tied low, and the output of the address decoder drives CONVST.

Data bits are shifted into the µPD7720 on the rising edge of SCK when SIEN is asserted. This means that SCLK from the AD7772 must be inverted before connecting to the SCK input. The internal shift register converts the serial data to parallel and transfers it to the SI register when 16 bits have been received. The internal acknowledge flag, SIACK, is also set at this time. When the parallel data is read from the SI register, this SIACK flag is reset. It is important to read the data from the SI register before the next conversion is complete and the data bits transferred; otherwise the original data will be lost.

When interfacing to the µPD77230, the inverter for SCLK shown in Figure 17 is not needed, since data on SI is synchronized with the falling edge of SICK (the serial input clock). Thus, SCLK from the AD7772 is connected directly to SICK on the µPD77230. All other connections are as in Figure 17.

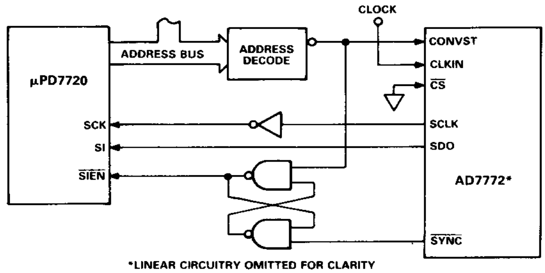


Figure 17. AD7772 to NEC µPD7720 Interface

DSP56000 INTERFACE

The DSP56000 has a very versatile serial interface which can be configured to suit various applications. Figure 18 shows an interface circuit for the AD7772 to DSP56000. The DSP56000 is configured for normal mode, asynchronous operation. This means that the DSP56000 serial transmitter and receiver have their own separate clock and synchronization signals. The processor is set up for 16-bit word and continuous clock with SCO and SCI configured as inputs. The FSL control bit, which selects the type of frame synchronization to be recognized, should be set to 0. All of these conditions are programmable in the DSP56000.

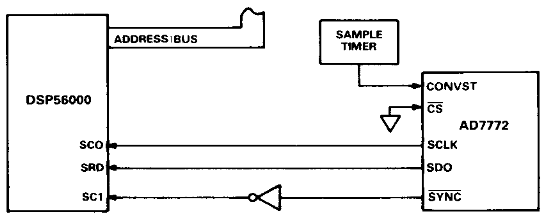


Figure 18. AD7772 to DSP56000 Interface

When the receiver is enabled, a 16-bit data word will be clocked in each time the frame synchronization signal is detected. Once received, the data word will be transferred from the SSI receive shift register to the receive data register (RX). The RDF flag (receive data register full flag) will be set to indicate that the receiver is full and the receive interrupt will occur if it has been enabled. The DSP program should read the data from RX before a new data word is transferred from the receive shift register, otherwise the receive overrun error (ROE) will be set.

AD7772 IN REMOTE CONTROL APPLICATIONS

Figure 19 shows a serial interface between the AD7772 and a remote controller. The digital signals are transmitted differentially along twisted pairs while optocouplers sense the signals at the receiving end. The DS8830 is a dual differential line driver, designed to drive long lengths of coaxial cable, strip line or twisted pair transmission lines. The optocouplers used are HCPL-2601s, which have sufficient speed (1000V/μs slew rate) to handle the maximum data transfer rate of 1.28M bits/sec.

The AD7772 is set up so that only one signal (CONVST) is needed to start conversion. Three twisted pairs are needed to transfer the data back to the controller. These take the SCLK, SDO and $\overline{\text{SYNC}}$ signals.

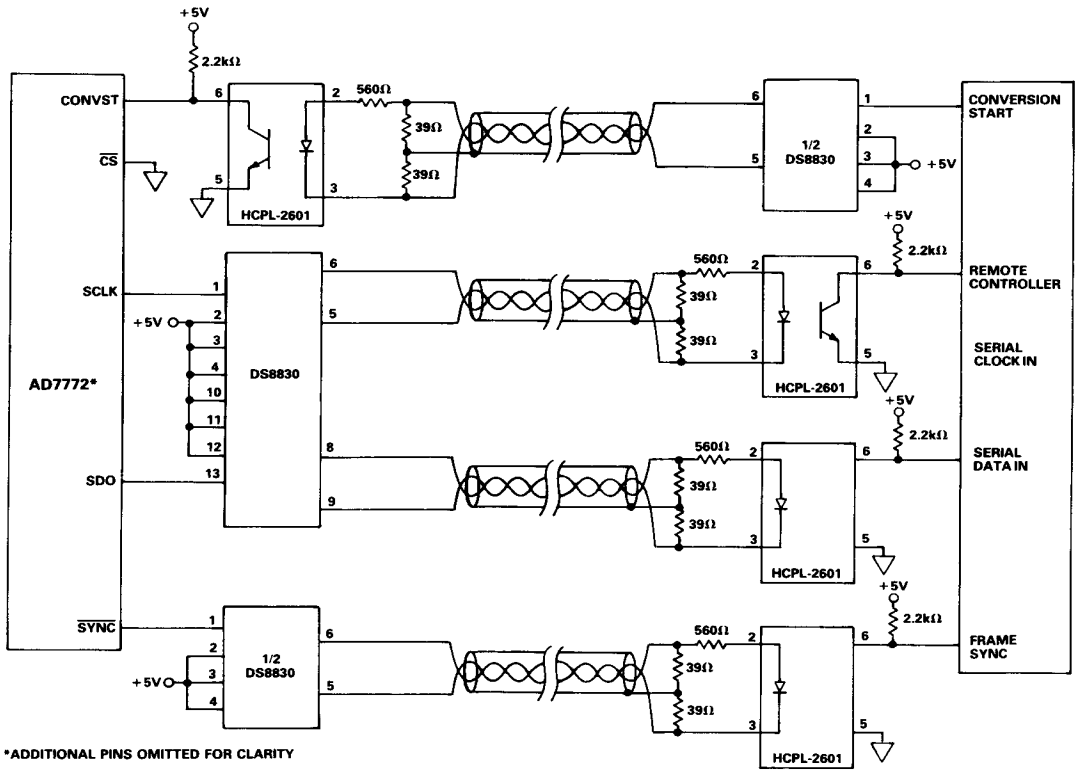


Figure 19. Using Optocouplers with the AD7772

AD7772 – AD585 SAMPLE-HOLD INTERFACE

Figure 20 shows a typical sampling application for the AD7772 with an AD585 sample-and-hold amplifier driving the ADC analog input. The AD585 is configured as a unity gain buffer. The ±10V input signal is successively sampled and held and this signal is then fed to Pin 7 of the AD7772 which is connected for an analog input range of ±10V.

For the circuit of Figure 20 to function properly, it is necessary to have the CONVST signal for the ADC synchronized with CLKIN as discussed previously. This ensures that the analog input is always held at a fixed point in time after the CONVST signal goes high and equal interval sampling is achieved. Without this synchronization, the holding point would not be exactly defined and the data acquisition system performance would suffer accordingly.

The maximum throughput rate of the system shown in Figure 20 is 76kHz. 10μs is required for conversion while a further 3μs must be allowed for the AD585 to acquire the signal. This yields a total time of 13μs. Thus, the maximum sampling rate is 76kHz and the analog input bandwidth is 38kHz.

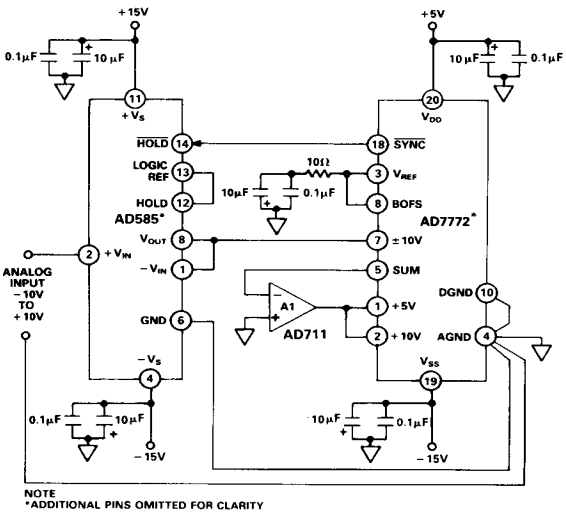


Figure 20. AD7772 Sample-and-Hold Interface

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7772's comparator is required to make bit decisions on an LSB size of 1.22mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 4 (AGND) or as close as possible to the AD7772 as shown in Figure 21. Connect all other grounds and Pin 10 (AD7772 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths while guarding the analog circuitry from digital noise. The circuit layout of Figures 24 and 25 have both analog and digital ground planes which are kept separate and only joined together at the AD7772 AGND pin.

NOISE: Keep the input signal leads to the analog input and signal return leads from AGND (Pin 4) as short as possible to minimize input noise coupling. In applications where this is not possible use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

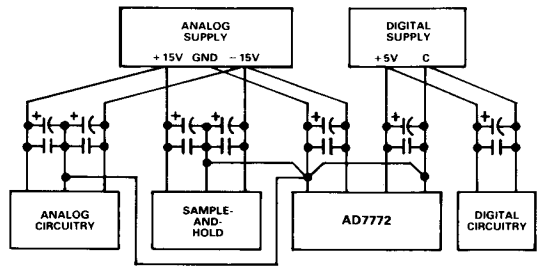


Figure 21. Power Supply Grounding Practice

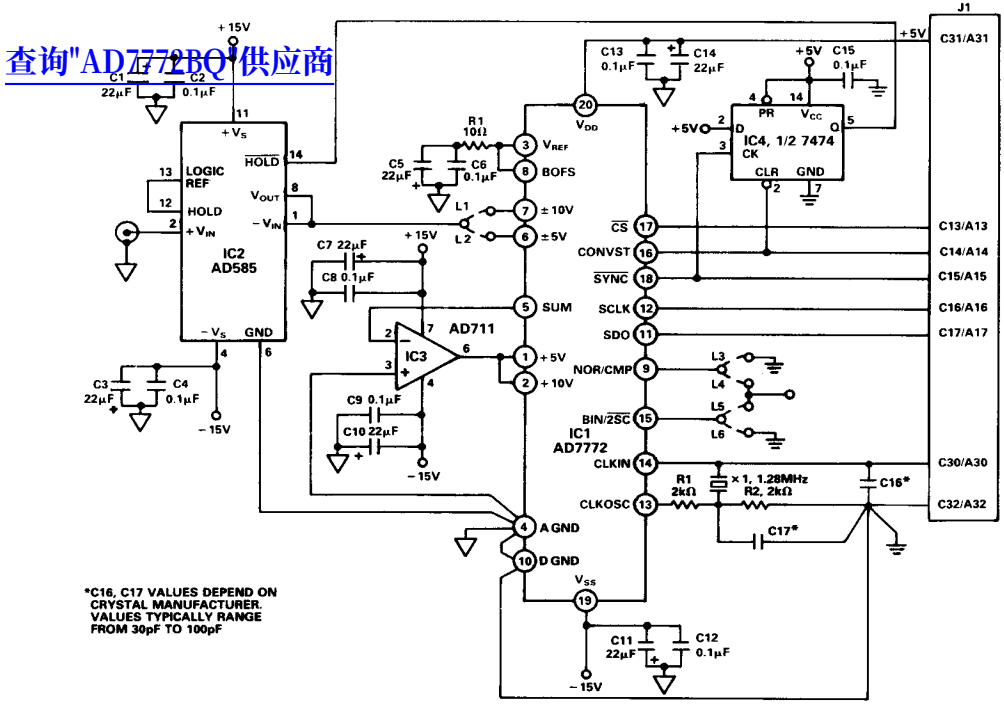


Figure 22. Schematic for AD7772 Board

PRINTED CIRCUIT BOARD LAYOUT

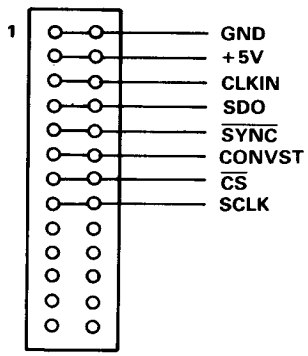
Figure 22 is a circuit diagram showing the AD7772 being used to digitize an analog signal. The circuit board contains the ADC, sample-and-hold and extra op amp necessary to sample a bipolar input signal. Links L1 and L2 allow the user to choose a ±5V or ±10V analog input range. With L1 inserted the range will be ±10V, and with L2 inserted it will be ±5V.

The AD585 is the input sample-and-hold. Its $\overline{\text{HOLD}}$ input is driven from IC4 (1/2 7474 D-type flip-flop). The input signal is sampled at the end of conversion, when $\overline{\text{SYNC}}$ goes high and is held when the CONVST signal goes low. To make sure that the sample-and-hold has enough time to acquire the input signal, the time from sample-and-hold should be at least 3µs. Links L3, L4, L5 and L6 allow the user to choose the output code format for the device. See Table I for the output code truth table.

The PCB layout is designed so that all external connections except the V_{DD} and V_{SS} power supplies can be made in any of three ways:

1. 32-way single-sided edge connector.
2. Eurocard connector, J1.
3. 26-pin plug, J2.

The pinout for the 26-way connector is shown in Figure 23, and the other pinouts are shown in Figure 22. The V_{DD} and V_{SS} power supplies are connected at the top of the board (see Figure 26).



J2: 26-WAY IDC PLUG

Figure 23. J2 Pin Configuration

The printed circuit board layout is shown in Figure 24 and 25. Figure 24 is the component side layout and Figure 25 is the solder side layout. The component overlay is shown in Figure 26. In the layout, the STAR ground point is located at Pin 4 (AGND). Pin 10 (DGND), the AD585 ground, AD711 ground and the ground plane are connected directly to this point.

To ensure optimum performance, the AD7772 power supplies are decoupled as shown. The V_{REF} pin is decoupled with R1, C5 and C6. All ADC decoupling capacitors are placed as close as possible to the device.

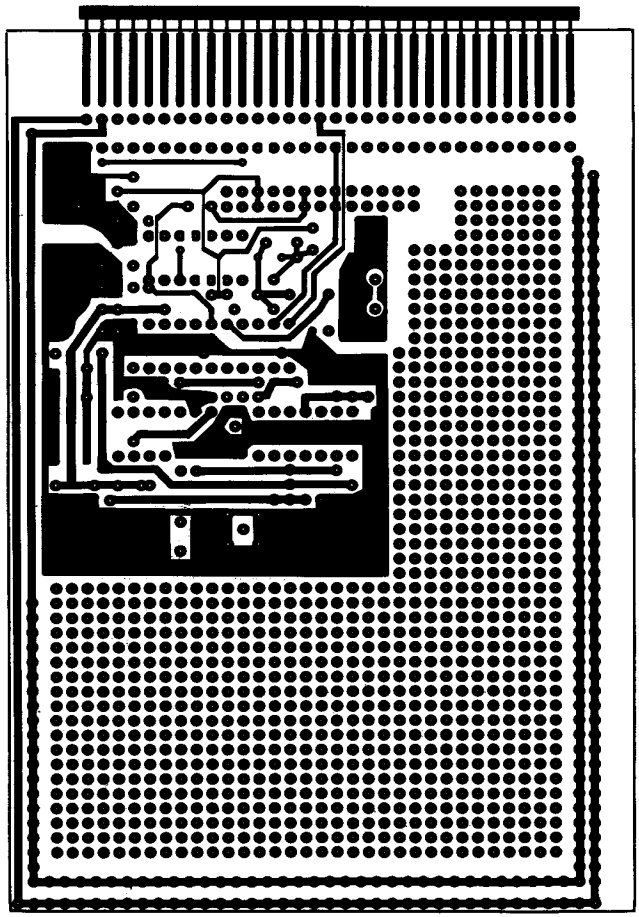


Figure 24. PCB Component Side Layout for Figure 22

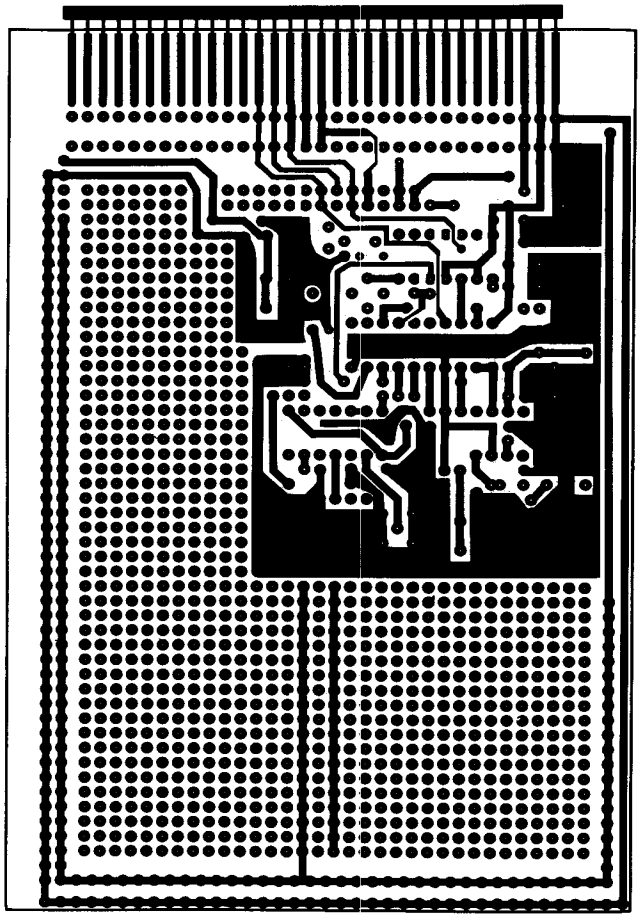


Figure 25. PCB Solder Side Layout for Figure 22

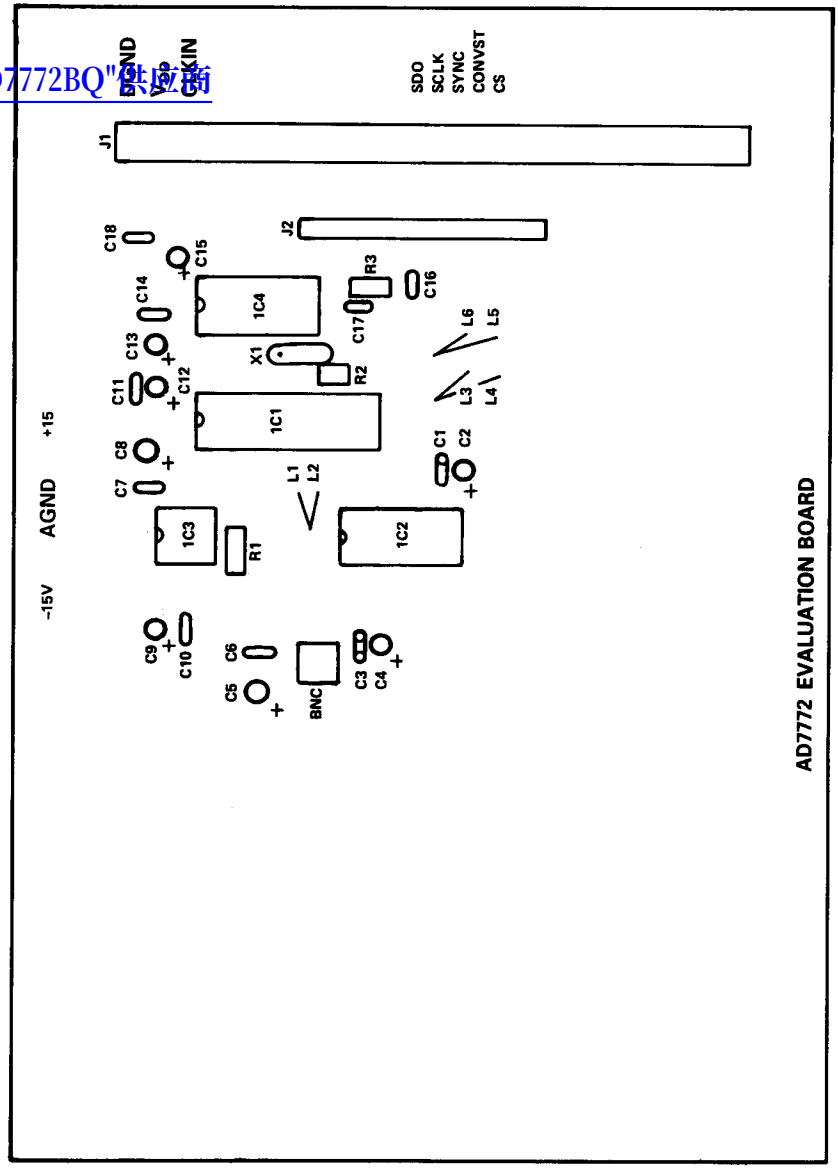


Figure 26. Component Overlay for Circuit of Figure 22